

I4T: 45V / 70V

Process Technology

I4T: 0.18 μm CMOS Process Technology - 45 V/70 V



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Overview

The I4T process from ON Semiconductor is an industry compatible 0.18 μm CMOS technology manufactured in the United States. This full featured process includes 1.8 V/3.3 V dual gate I/Os, nominal and high value MIM capacitors, resistors, and six levels of metal. A comprehensive design kit offers an expansive core, I/O, and memory library. Specialty services including stitching,

planarized passivation, shuttle prototyping are available. The I4T process is the only 180 nm process available with deep trench isolation (DTI), which makes it uniquely suitable for high-voltage automotive applications. I4T also serves as a platform for highly integrated high voltage mixed-signal processes ideal for many automotive, industrial, medical, and military applications.

Features

- 4 to 6 Metal Layers
- 1.0 fF/ μm^2 Metal-insulator-metal (MIM) Capacitor
- 2.0 fF/ μm^2 Metal-insulator-metal (MIM) Capacitors (design dependent)
- 4.0 fF/ μm^2 Metal-insulator-metal (MIM) Stacked Capacitors (design dependent)
- Salicide Process with Optional Blocking
- 1.8 V, 3.3 V Core Voltage and 3.3 V I/O Voltage with 5 V Tolerant Input
- Poly, Diffusion, and Well Resistors
- Deep Trench Isolation
- Bipolar Transistors: HV and LV Parasitic
- Extended Temperature Range -40 to $+200^\circ\text{C}$
- Die Stitching
- Specialty Devices
 - ◆ 5 V Zener Diode
 - ◆ Schottky Diode
 - ◆ HV Schottky Diode
 - ◆ Deep N-Well (Triple Well/Noise Isolation)

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PROCESS CHARACTERISTICS

Operating Voltage	1.8 V, 3.3 V
Substrate Material	P-Type
Drawn Transistor Length	0.18 μm
Gate Oxide Thickness	2.9 nm/6.5 nm
Contact/Via Size	0.22 μm /0.26 μm
Metal Thickness	M1-MTop-1 – 0.56 μm MT(0.8 μm) – 0.94 μm MT(3.0 μm) – 3.14 μm
Contacted Metal Pitch	
Metal 1	0.46 μm
Metal 2-Top-1	0.56 μm
Metal Top (0.8 μm)	0.9 μm
Metal Top (3.0 μm)	6 μm
Metal Composition	Al-0.5%Cu/TiN

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TEMPERATURE RANGE

Minimum	-40°C	-40°C	-40°C	-40°C		
Maximum	200°C	135°C	135°C	135°C		

CMOS (Isat [$\mu\text{A}/\mu\text{ width}$] shown)

1.8V NMOS – Generic Threshold	600	600	600	600	N	
1.8V PMOS – Generic Threshold	-260	-260	-260	-260	N	
1.8V Native NMOS	365	365	365	365	N	
1.8V Low Vt NMOS	350	350	350	350	1	
1.8V NMOS – High Threshold ~ 0.65V	410	410	410	410	2	
1.8V PMOS – High Threshold ~ -0.65V	-175	-175	-175	-175	2	
3.3V NMOS – Generic Threshold	550	NA	NA	550	N	
3.3V PMOS – Generic Threshold	-285	NA	NA	-285	N	
3.3V Native NMOS	540	NA	NA	540	N	
3.3V Low Vt NMOS	370	NA	NA	370	1	
5.0V NMOS – Generic Threshold (SVt)	NA	570	570	NA	N	
5.0V PMOS – Generic Threshold (SVt)	NA	-258	-258	NA	N	
5.0V NMOS – Medium Threshold (XVt)	NA	420	420	NA	1	
5.0V PMOS – Medium Threshold (XVt)	NA	-158	-158	NA	1	
5.0V NMOS – Low Threshold (LVt)	NA	390	390	NA	1	
5.0V PMOS – Low Threshold (LVt)	NA	-124	-124	NA	1	
5.0V Native NMOS	NA	14	14	NA	N	

CAPACITORS (BV [V] shown)

MiM Capacitor – 1 fF/ μm^2	>20 V	>20 V	>20V	>20 V	1	
High Capacitance MIM – 2 fF/ μm^2	>10 V	>10 V	>10V	>10 V	1	
Stacked MiM Capacitor – 4 fF/ μm^2	>10 V	>10 V	>10V	>10 V	2	
Linear MOSCAP (Thick) – ~4 fF/ μm^2	>5 V	NA	NA	>5 V	1	
Linear MOSCAP (Thin) – ~8 fF/ μm^2	>2.5 V	>2.5 V	>2.5 V	>2.5 V	1	
Metal Finger Capacitor – 0.5 & 0.7 fF/ μm^2	>20 V	>20 V	>20 V	>20 V	N	
HV Metal Finger Cap – 0.23 fF/ μm^2 (>0.45 μm Space)	>100 V	>100 V	>100 V	>100 V	N	>0.45 μm Spacing required.

RESISTORS (Rsheet [Ω/sq] shown)

N+ w/ Salicide	7	7	7	7	N	
N+ w/o Salicide	60	60	60	60	N	
P+ w/ Salicide	7	7	7	7	N	
P+ w/o Salicide	127	127	127	127	N	
N+ Poly w/ Salicide	7	7	7	7	N	
N+ Poly w/o Salicide	290	290	290	290	N	
P+ Poly w/ Salicide	7	7	7	7	N	
P+ Poly w/o Salicide	311	311	311	311	N	
N-Well under STI	910	910	910	910	N	
"Low" TC Resistor	295	295	295	295	1	

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RESISTORS (Rsheet [Ω /sq] shown)

High Value Resistor	1035	1035	1035	1035	1	
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RESISTORS (Rsheet [Ω /sq] shown)

Deep Trench Isolation (DTI)	✓					
3.3V Gate / 15V Drain Analog NLD MOS	NA	NA	NA	41	N	
3.3V Gate / 15V Drain NLD MOS Switch	NA	NA	NA	8.5	N	
3.3V Gate / 15V Drain PLD MOS	NA	NA	NA	34.5	N	
5.0V Gate / 18V Drain NLD MOS	NA	17	17	NA	4	5 V 30 V Flow
5.0V Gate / 18V Drain PLD MOS	NA	45	45	NA	4	5 V 30 V Flow
5.0V Gate / 24V Drain NLD MOS	NA	21.5	21.5	NA	4	5 V 30 V Flow
5.0V Gate / 24V Drain PLD MOS	NA	60	60	NA	4	5 V 30 V Flow
5.0V Gate / 30V Drain NLD MOS	NA	24.5	24.5	NA	4	5 V 30 V Flow
5.0V Gate / 30V Drain PLD MOS	NA	68	68	NA	4	5 V 30 V Flow
18V Gate / 18V Drain Symetrical isolated NLD MOS	NA	NA	58	NA	11	18 V 18 V Flow
18V Gate / 18V Drain Symetrical,isolated, analog NLD MOS	NA	NA	60	NA	11	18 V 18 V Flow
18V Gate / 18V Drain Asymetrical, isolated NLD MOS	NA	NA	23	NA	11	18 V 18 V Flow
18V Gate / 18V Drain Asymetrical PLD-MOS	NA	NA	49.5	NA	11	18 V 18 V Flow
18V Gate / 18V Drain Symetrical PLD MOS	NA	NA	87	NA	11	18 V 18 V Flow
18V Gate / 18V Drain Symetrical, analog PLD MOS	NA	NA	180	NA	11	18 V 18 V Flow
3.3V Gate / 30V Drain NLD MOS Switch / Analog	32 / 48.5	NA	NA	NA	7	45 V or 70 V Flow
3.3V Gate / 30V Drain PLD MOS Switch / Analog	75 / 112	NA	NA	NA	7	45 V or 70 V Flow
3.3V Gate / 45V Drain NLD MOS Switch / Analog	49 / 78	NA	NA	NA	7	45 V or 70 V Flow
3.3V Gate / 45V Drain PLD MOS Switch / Analog	132 / 183	NA	NA	NA	7	45 V or 70 V Flow
3.3V Gate / 70V Drain NLD MOS Switch / Analog	97 / 173	NA	NA	NA	9	70 V Flow
3.3V Gate / 70V Drain PLD MOS Switch / Analog	231 / 280	NA	NA	NA	9	70 V Flow

BIPOLAR TRANSISTORS

LV Parasitic Bipolars	✓	✓	✓	✓	N	
HV Parasitic Bipolars	✓	✓	✓		N	

NON-VOLATILE MEMORY

CMOS LogicEE Trim	✓			✓	N	
High Temperature CMOS LogicEE Trim	R&D				N	
Poly Fuse OTP	✓	✓	✓		N	
LogicEE MTP		R&D	R&D		N	
OTP (Sidense Oxide Rupture OTP)	✓			✓	N	

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SPECIALTY DEVICES

5V Zener Diode	✓	✓	✓	✓	1	
5.5V Zener Diode		✓	✓		1	
Free Zener Diode (5.5 to 6.5 V)		✓	✓		N	
Schottky Diode	✓	✓	✓	✓	1	
HV Schottky Diode	✓	✓	✓		N	
Deep N-well (Triple Well / Noise Isolation)	✓	✓	✓	✓	1	

LIBRARIES

(All values typical at 1.8 V, 25°C)

Front-End Digital Design
Digital
Synthesis Libraries
Simulation Libraries
Analog
Design Rules
Spice Models

Standard Core Cell	Density (gates/ mm ²)	Operating Voltage	Leakage (nW)	Propagation Delay (ps)	Dynamic Power (mW/MHz/gate)
1.8 V Standard Core Cell	99.6 k	1 V, 1.5 V, 1.8 V	0.136	137 with 0.015 pF L	0.000031
1.8 V Low Leakage Core Cell	99.6 k	1.5 V, 1.8 V	0.008	171 with 0.0148 pF L	0.000021
3.3 V High Voltage Core Cell	70.8 k	3.3 V	0.00097	112 with 0.0194 pF L	0.00016
Level Shifter	n/a	1.8 V, 3.3 V	n/a	n/a	n/a

*All the data derived from 2nand cell under nominal voltage and 25°C.

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IO Library Description	CUP Support	DTI Support	N-well Option	5 V Process Support	Operating Voltage (±10%)	5 V Tolerant	3 V Tolerant	~ Pad Height (µm)	~ Inline / (Staggered) Pad Pitch (µm)	Max Output Strength per Pad (mA)	Top Metal Option	
1.8 V	Yes	Yes	Regular	Y	1.0 V, 1.8 V	N	Y	117	84	12	4, 5, 6	
3.3 V w/level-shift				N	2.5 V, 3.3 V	Y	N	130/146	84/96	12	4, 5, 6	
3.3 V				N	1.8 V, 3.3 V	Y	N	121/135	84/96	12	4, 5, 6	
1.8 V		No	No	Deep	Y	1.0 V, 1.8 V	N	Y	136	84	12	4, 5, 6
3.3 V w/level-shift					N	3.3 V	Y	N	152	84	12	4, 5, 6
3.3 V					N	1.8 V, 3.3 V	Y	N	132	84	12	4, 5, 6
5.0 V					Y	1.8 V, 2.5 V, 3.3 V, 5.0 V	Y	N	132	84	12	4, 5, 6
3.3 V	N				1.8 V, 3.3 V	Y	N	221	84	12	4, 5, 6	
1.8 V	Y				1.0 V, 1.8 V	N	Y	226	84	12	4, 5, 6	
5.0 V	Y				1.8 V, 2.5 V, 3.3 V, 5.0 V	Y	N	222	84	12	4, 5, 6	
3.3 V w/level-shift	No	Yes	Regular	N	2.5 V, 3.3 V	Y	N	220	84	12	4, 5, 6	
1.8 V pad limited				Y	1.8 V	N	N	235	60 / (40)	24	5, 6	
2.5 V pad limited w/1.8V level-shift				N	2.5 V	N	Y	235	60 / (40)	16	5, 6	
3.3 V pad limited w/1.8V level-shift				N	3.3 V	Y	N	235	60 / (40)	24	5, 6	
3.3 V pad limited w/o level-shift				N	3.3 V	Y	N	235	60 / (40)	16	5, 6	

MEMORY OPTIONS

Compiled Memory Description	MEM-Type	Max Capacity per Instance	Bit Density (eq. bits/mm ²) (Note 1)	Operating Voltage (V)	Max Frequency (MHz) (Note 2)	Leakage Current (µA) (Note 2)	Dynamic Power (nW/MHz) (Note 2)
ONC18 HVT Single port SRAM	SRAM	589 kbits	160k	1.0, 1.5 V, 1.8 V	200	2	311
ONC18 HVT Dual port SRAM	DPRAM	294 kbits	80k	1.0, 1.5 V, 1.8 V	200	3	285
ONC18 HVT ROM	ROM	1.1 kbits	900k	1.0, 1.5 V, 1.8 V	150	0.5	183
ONC18 SVT Single port SRAM	SRAM	589 kbits	160k	1.0, 1.2 V 1.5 V, 1.8 V	300	50	310
ONC18 SVT Dual port SRAM	DPRAM	294 kbits	80k	1.0, 1.2 V 1.5 V, 1.8 V	300	70	300
ONC18 SVT ROM	ROM	1.1 Mbits	900k	1.0, 1.2 V 1.5 V, 1.8 V	200	40	141
ONC18 3.3 V Signal port SRAM (Note 3)	SRAM	589 kbits	110k	1.8 V, 3.3 V	100	0.5	n/a
ONC18 3.3 V Dual port SRAM (Note 3)	DPRAM	589 kbits	75k	1.8 V, 3.3 V	100	0.5	n/a
ONC18 3.3 V ROM (Note 3)	ROM	589 kbits	850k	1.8 V, 3.3 V	100	0.1	n/a

1. All the data derived from 256 kb instance.
2. Max frequency and leakage current evaluated based on 256 kbit configuration (4kx64), at PwcsV162T125.
3. This Memory Compiler is under development .

NON-VOLATILE MEMORY

OTP – One Time Programmable (Sidense Oxide Rupture OTP)

1k-bit array and 256 kbit array
In field programming capable

CAD TOOL COMPATIBILITY

Digital Design	Cadence Design Kit	Mentor Design Kit	Other
Digital Symbols	Virtuoso	Pyxis Schematic and Language Editor Interface	
RTL Synthesis	Cadence RTL	Mentor Leonardo	Synopsys Design Compiler Explorer
Scan Insertion		Mentor DFT advisor	Synopsys Design DFT Compiler
Static and Timing Analysis			Synopsys Primitime
Power Analysis			Synopsys Primepower
Digital Simulation	Cadence Incisive	Mentor Questa	
Formal Verification	Cadence Conformal	Mentor Formal Pro	Synopsys Formality
P&R	Encounter	Olympus-SOC	Synopsys IC Compiler
Test ATE	Cadence Encounter Test	Tessent	Synopsys Tetramax

ANALOG/MIXED-SIGNAL DESIGN


Schematic View and Sizing	Virtuoso	Pyxis Schematic Editor	
	ADE L-XL-GXL	Pyxis Simulation	
Analog Simulation	Spectre-AP-UltraSim	IC Analyst	HSPICE
		Eldo-Eldo Premier-Adit	
Analog Layout	Virtuoso-XL	Pyxis DLA	
Routing	VSR (CCAR, VCR)	iroute-Pyxis Custom Router	

TOP-LEVEL

Symbol Editor	Virtuoso	Pyxis Schematic and Language Editor Interface	
Top-level Simulation	Cadence AMS	Mentor Questa - ASMS	
Top-level Router		Pyxis Custom Router	

VERIFICATION

DRC		Calibre	
LVS		Calibre	
Robustness		Calibre PERC	
Analog Parasitic Extraction		Calibre xRC-PEX	
Digital Parasitic Extraction			Synopsys StarRC

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