

## Process Technology C3/D3: 0.35 $\mu\text{m}$ Process Technology



ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)

### Overview

The C3/D3 process family from ON Semiconductor is an ideal 0.35  $\mu\text{m}$  low cost solution to mixed-signal designs requiring a moderate amount of digital logic (up to 250 k gates). Optimized for 3.3 V operation with added devices for 5 V capability, high-performance, low-power, and mixed-signal digital libraries, and mixed-signal features such as poly-poly capacitors, Schottky diodes, and high resistivity poly. C3/D3 provides the flexibility to implement a variety of mixed-signal applications.

### Features

- 3 to 5 Metal Layers
- Poly to Poly Capacitors
- Schottky Diodes
- High-resistance Poly
- Salicide Process with Optional Blocking
- 5 V Devices (Thick Gate Oxide)
- 5 V Tolerant I/O in Normal Process

### PROCESS CHARACTERISTICS

Operating Voltage	3.3 V, 5 V
Substrate Material	P-Type, EPI
Drawn Transistor Length	0.35 $\mu\text{m}$
Gate Oxide Thickness	7.0 nm / 11.0 nm
Contact/Via Size	0.4 $\mu\text{m}$ / 0.5 $\mu\text{m}$
Top Metal Thickness	675 nm
Contacted Metal Pitch	
Metal 1	1.1 $\mu\text{m}$
Metal 2-5	1.2 $\mu\text{m}$
Metal Composition	Al/TiN

### SAMPLE PROCESS OPTIONS

	Mask Layers
1 Poly, 3 Metal	16
1 Poly, 5 Metal	20
2 Poly, 3 Metal. Hi-R Poly	20
2 Poly, 5 Metal. Hi-R Poly	24

### DEVICE CHARACTERISTICS

All Values Typical at 25°C

#### TRANSISTORS

N-Channel	Typical Value	Units
$V_t$	0.5	V
$I_{dsat}$	510	$\mu\text{A}/\mu\text{m}$
P-Channel	Typical Value	Units
$V_t$	-0.554	V
$I_{dsat}$	-259	$\mu\text{A}/\mu\text{m}$

#### THICK GATE TRANSISTORS

N-Channel	Typical Value	Units
$V_t$	0.76	V
$I_{dsat}$	470	$\mu\text{A}/\mu\text{m}$
P-Channel	Typical Value	Units
$V_t$	-0.95	V
$I_{dsat}$	-240	$\mu\text{A}/\mu\text{m}$

#### RESISTORS

	Typical Value	Units
Poly	10	$\Omega/\text{square}$
Hi-R Poly	1000	$\Omega/\text{square}$
N-Diffusion	10	$\Omega/\text{square}$
P-Diffusion	10	$\Omega/\text{square}$
N-Well	1250	$\Omega/\text{square}$

#### CAPACITORS

	Typical Value	Units
Poly-Poly	0.9	fF/ $\mu\text{m}^2$

#### DIODES

Schottky Diode	Typical Value	Units
Area	5.1	$\mu\text{m}^2$
$I_d$ ( $V_f = 0.1$ V)	0.05	$\mu\text{A}$
$I_d$ ( $V_f = 0.3$ V)	2	$\mu\text{A}$
$I_d$ ( $V_f = 0.6$ V)	175	$\mu\text{A}$

## LIBRARIES

Standard Cell	
<b>Ultra High Density Core Cell</b>	pn sum: 2.0
	Area of 2-input nand (na21): 38.88 $\mu\text{m}^2$
	Gate density (na21 @ 100% utilization): 25.72 k gates/mm <sup>2</sup>
	Scan Flop density (scan flops @ 100% utilization): 3.215 k ff/mm <sup>2</sup>
	Average power (@ 3.3 V): 0.604852 $\mu\text{W}/\text{MHz}/\text{gate}$
<b>Mixed-Signal Core Cell – Separate substrate for reduced noise</b>	pn sum: 4.5
	Area of 2-input nand (na21): 74.88 $\mu\text{m}^2$
	Gate density (na21 @ 100% utilization): 13.35 k gates/mm <sup>2</sup>
	Scan Flop density (scan flops @ 100% utilization): 1.842 k ff/mm <sup>2</sup>
	Average power (@ 3.3 V): 0.6074 $\mu\text{W}/\text{MHz}/\text{gate}$
<b>5 V Capable Core Cell – Thick gate logic design</b>	pn sum: 5.0
	Area of 2-input nand (na21): 108 $\mu\text{m}^2$
	Gate density (na21 @ 100% utilization): 9.259 k gates/mm <sup>2</sup>
	Scan Flop density (scan flops @ 100% utilization): 1.187 k ff/mm <sup>2</sup>
	Average power (@ 5.0 V): 3.0553 $\mu\text{W}/\text{MHz}/\text{gate}$
<b>Core Cell Level Shifters</b>	Bidirectional: 2 cells, pad high to core low, or pad low to core high
	Unidirectional: 1 cell optimized for speed, pad high to core low
Standard I/O	
<b>Fat Pad I/O Library (for core limited designs)</b>	135 $\mu\text{m}$ max in-line pad pitch
	459.15 $\mu\text{m}$ pad height
<b>Tall Pad I/O Library (for pad limited designs)</b>	86 $\mu\text{m}$ max in-line pad pitch
	730 $\mu\text{m}$ pad height

<b>5 V Capable I/O Library – Thick gate logic design</b>	140.40 $\mu\text{m}$ max in-line pad pitch
	274.05 $\mu\text{m}$ pad height

## MEMORY OPTIONS

RAM	
<b>Asynchronous Single Port SRAM*</b>	35 $\mu\text{m}^2/\text{bit}$ (64 k bit memory)
<b>Asynchronous Dual Port SRAM*</b>	64 $\mu\text{m}^2/\text{bit}$ (64 k bit memory)
ROM	
<b>Asynchronous Diffusion ROM*</b>	5.4 $\mu\text{m}^2/\text{bit}$ (64 k bit memory)
Non-Volatile Memory	
<b>EEPROM</b>	Differential Bit Cell (Redundancy for High Reliability)
	2 ms Write
	Array: up to 1 k Bits (32x32), Vector: up to 32 bits (1x32)
	Internal Charge Pump provided

\*Compiled

## CAD TOOL COMPATIBILITY

<b>Digital Design</b>	Synopsys Design Compiler
	Cadence Verilog
<b>Analog Design</b>	Cadence DFII (4.4.6)
	Spectre
<b>Place and Route</b>	Synopsys Apollo, Astro
	Cadence Silicon Ensemble
<b>Physical Verification</b>	Mentor Calibre

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

## LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
 19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
 USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
 Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
 Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative