25 kW fast EV DC Charger power stage

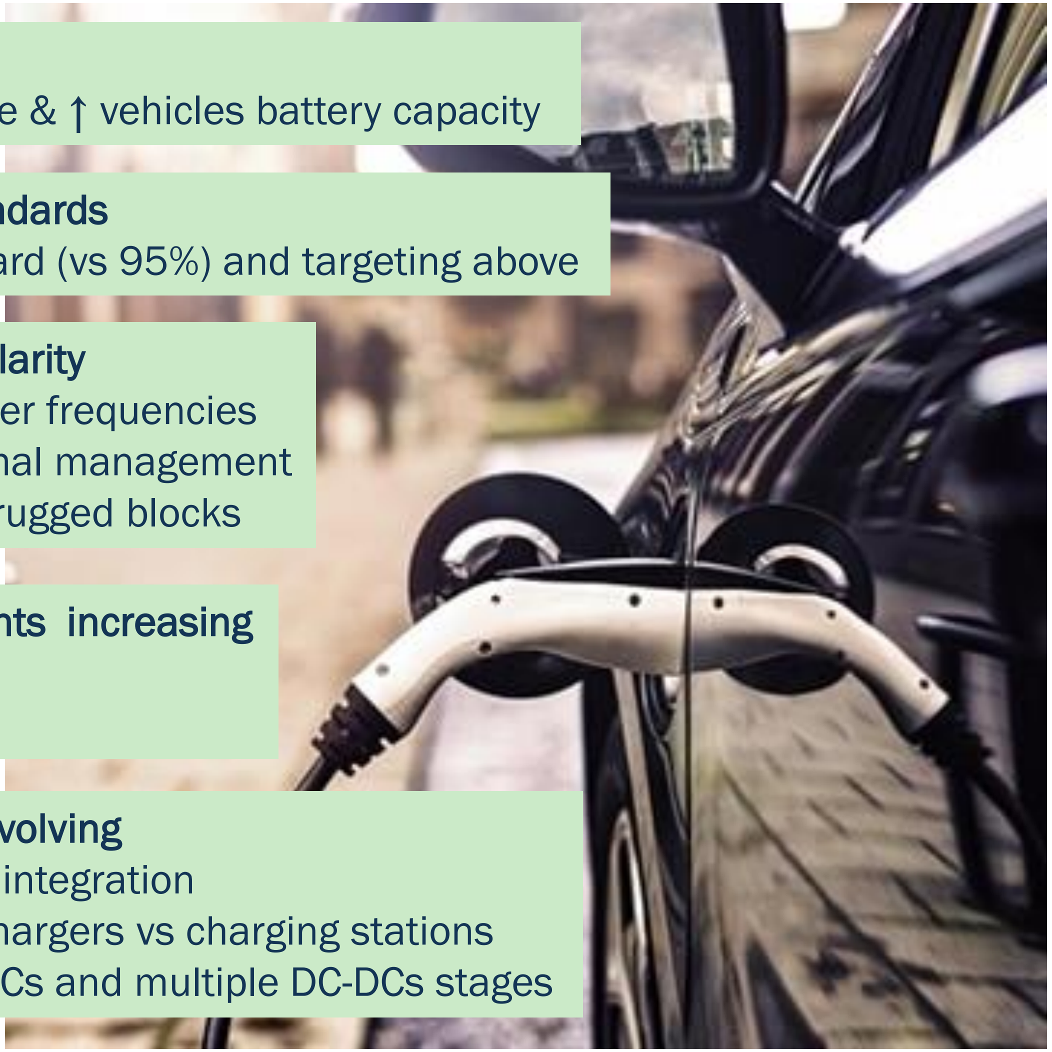
SiC Module, 2-PACK Half Bridge Topology, 1200 V, 10 mohm SiC MOSFET

May 2021

Your value-added partner for EV charging solutions

EV charging market outlook

Requirements are rapidly evolving in several directions



Peak powers increasing
- ↓ charging time & ↑ vehicles battery capacity

Increasing efficiency standards
- 96% as standard (vs 95%) and targeting above

Size reduction and modularity
- Requiring higher frequencies
- Superior thermal management
- Compact and rugged blocks

Cost-focused developments increasing
- ↑ #of competitors
- Commoditization

Multiple use cases and evolving
- ESS and solar integration
- Stand-alone chargers vs charging stations
- Centralized PFCs and multiple DC-DCs stages

Handling such a broad and fluid scope of demanding requirements takes …

- High-level application expertise
- A variety of solutions to fit different cases
- Realiable and robust power conversion technologies

Public Information

ON Semiconductor is your value-added partner for Fast DC EV Charging solutions

System solution expertise and long experience

+ 5 years focus on EV Charging
Dedicated expert application teams
An array of reference design developments
Developements on SiC driver optimization

Development tools and support

Thermal and electrical simuation models
Physical scalable models (Learn more)
Evaluation boards and reference desings

Leading power modules and SiC technologies with a comprehensive overall portfolio

Continuous investment in enhanced packaging technology
Superior SiC features with patented termination for ruggedness
Power devices, analog ICs, auxiliary power, sensing protections and connectivity portfolio

Fully integrated supply value chain

In-house raw wafers
Wafer manufacturing and assembly

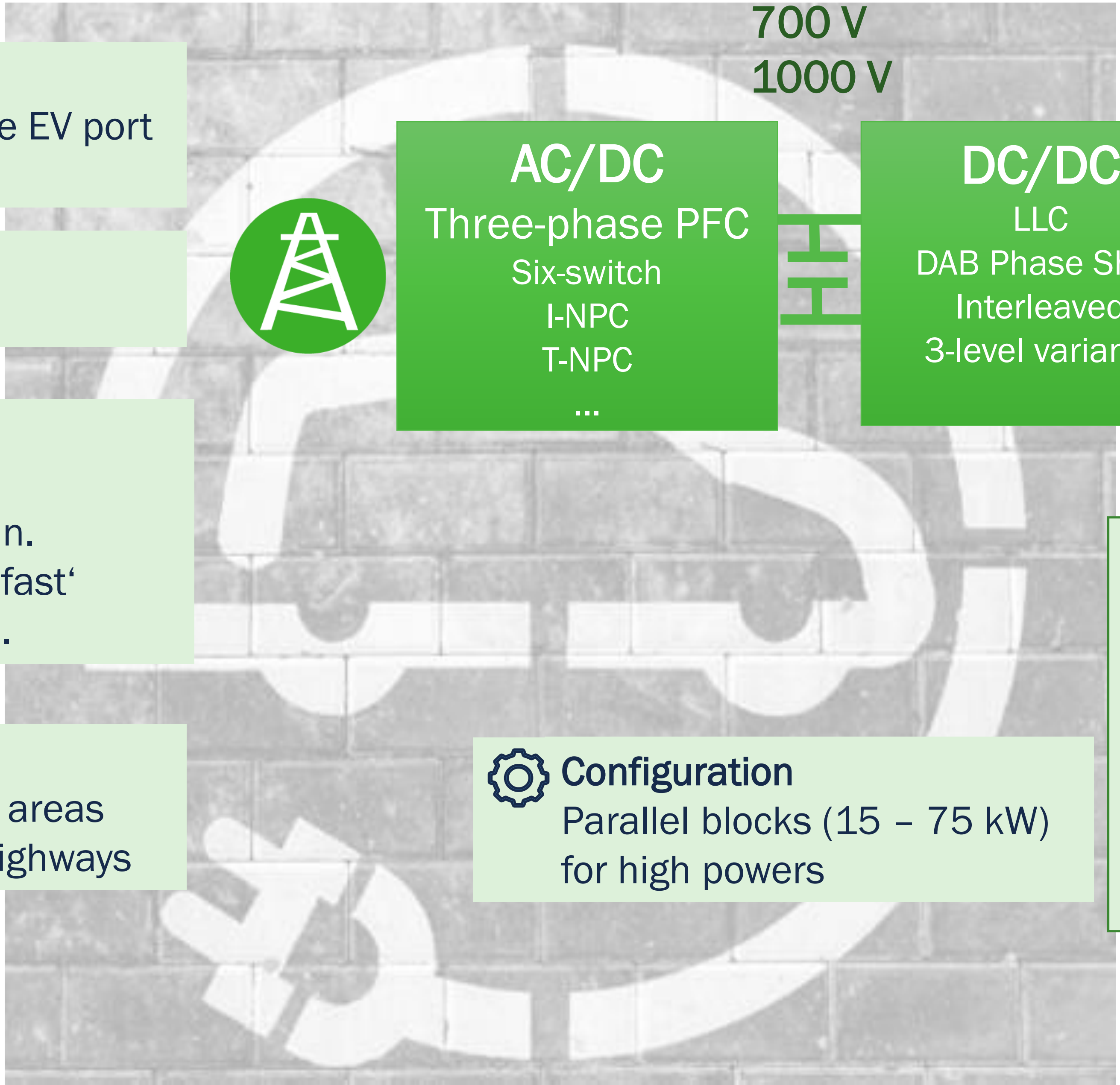
Fast and Ultrafast DC Charging ~ 50 kW – > 350 kW

'Off-board' conversion
Deliver a DC voltage to the EV port

Growth ~ 25 % CAGR
for the next 5 years

Power ratings
~ 50 kW to 100 kW ‚Fast'
100 km < 15 min.
~ 100 kW > 350 kW ‚Ultrafast'
100 km < 2 min.

Deployment locations
‚Fast' inside cities/urban areas
‚Ultrafast' mostly along highways



700 V
1000 V

AC/DC
Three-phase PFC
Six-switch
I-NPC
T-NPC
...

DC/DC
LLC
DAB Phase Shift
Interleaved
3-level variants

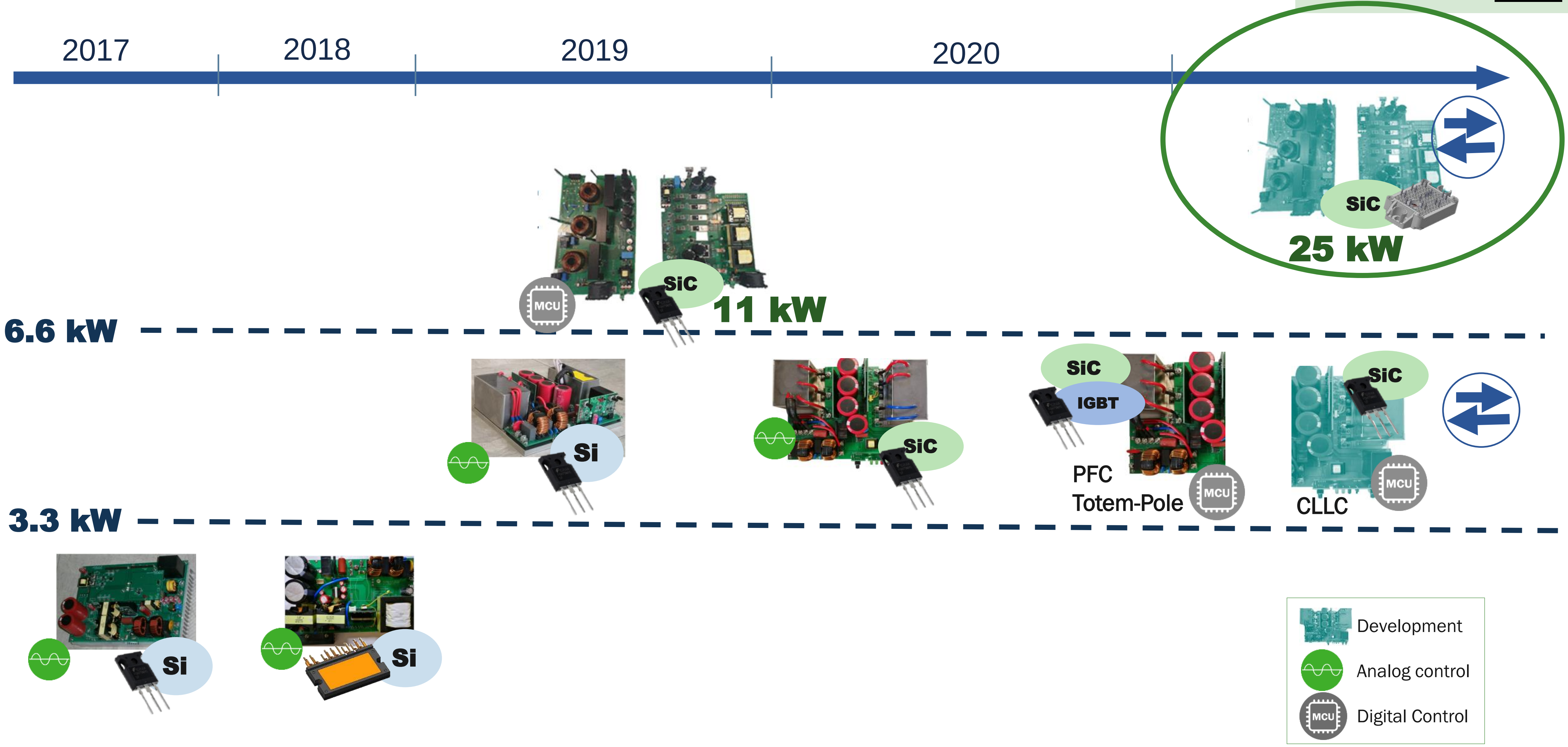
500 V
1000 V

Configuration
Parallel blocks (15 – 75 kW)
for high powers

15 – 75 kW #1
15 – 75 kW #2
15 – 75 kW #3
15 – 75 kW #4

EV Charging - Fostering system expertise since 2016

Find all boards



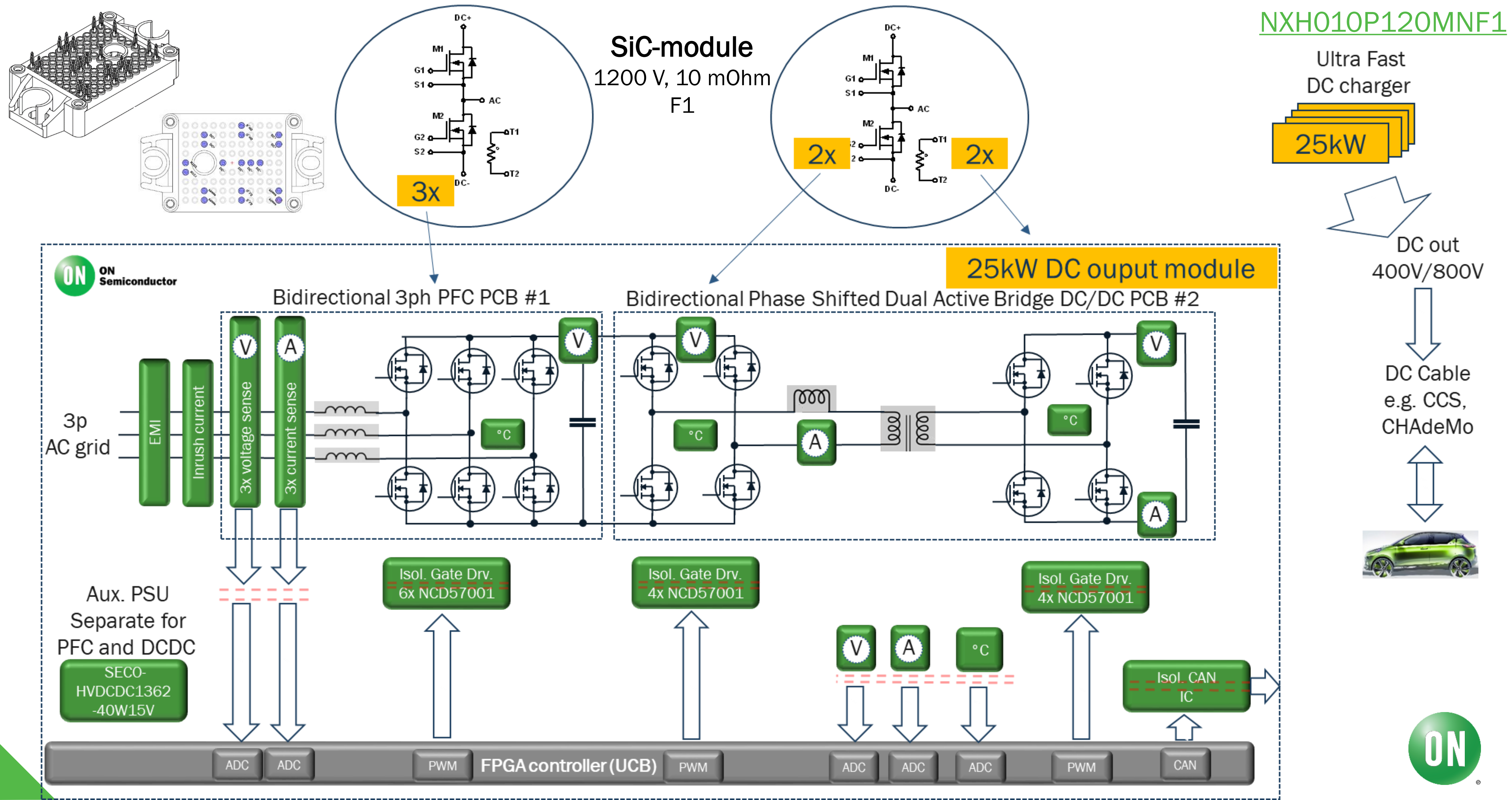
Public Information

25 kW fast EV DC Charger power stage

Taking advantage of 1200 V 10 mOhm

2-PACK SiC-modules

Reference design - 25 kW fast DC Charger power stage



Specification and Key Features

AC input	
Voltage	3-phase 400 V AC (EU) / 480 V AC (US)
Max. Current	37 A
Power Factor	> 0.99
Efficiency	> 96 %

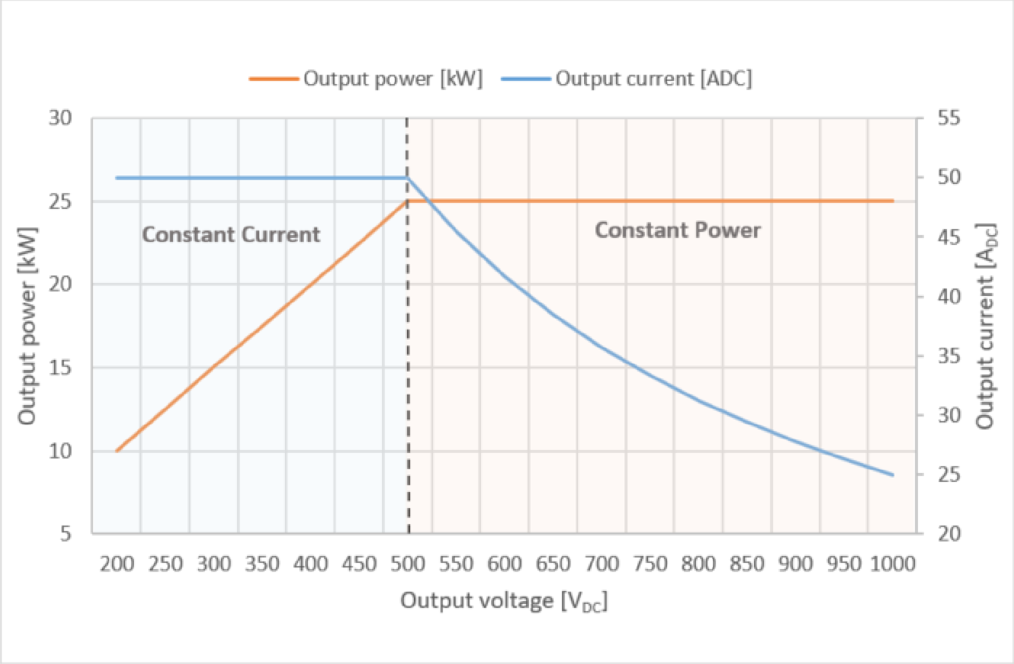
DC Output	
Voltage	800 VDC (optimized) / (200 VDC – 1000 VDC) supported
Max. Power	25 kW
Max. Current	50 A

Protections	
Output	OVP, OCP, SC
Input	UVP, OVP, inrush current limitation
Internal	DESAT (driver), Thermal (NTC on PIM)

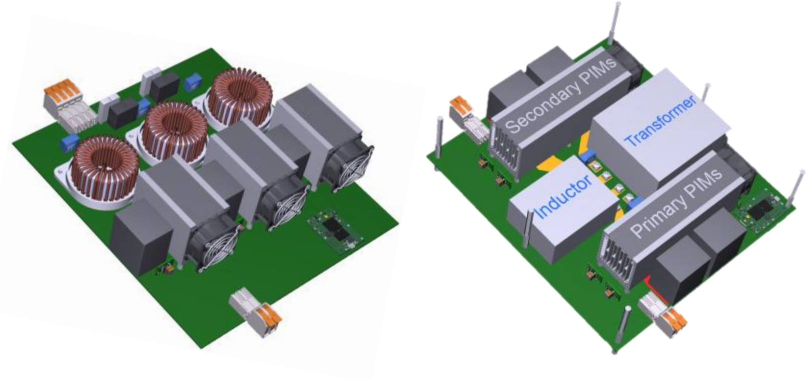
Communications	
Internal	SPI, I2C
External	Isolated CAN, USB, UART

Standards / Norms	
Standard/Norm EV Charging	IEC – 61851 (used as guideline)
Regulation	EN55011 Class A (used as guideline)

Load profile



Dimensions	
Total size (PFC+DCDC)	380 x 345 x (200-270*) mm (stacked PFC and DC-DC)



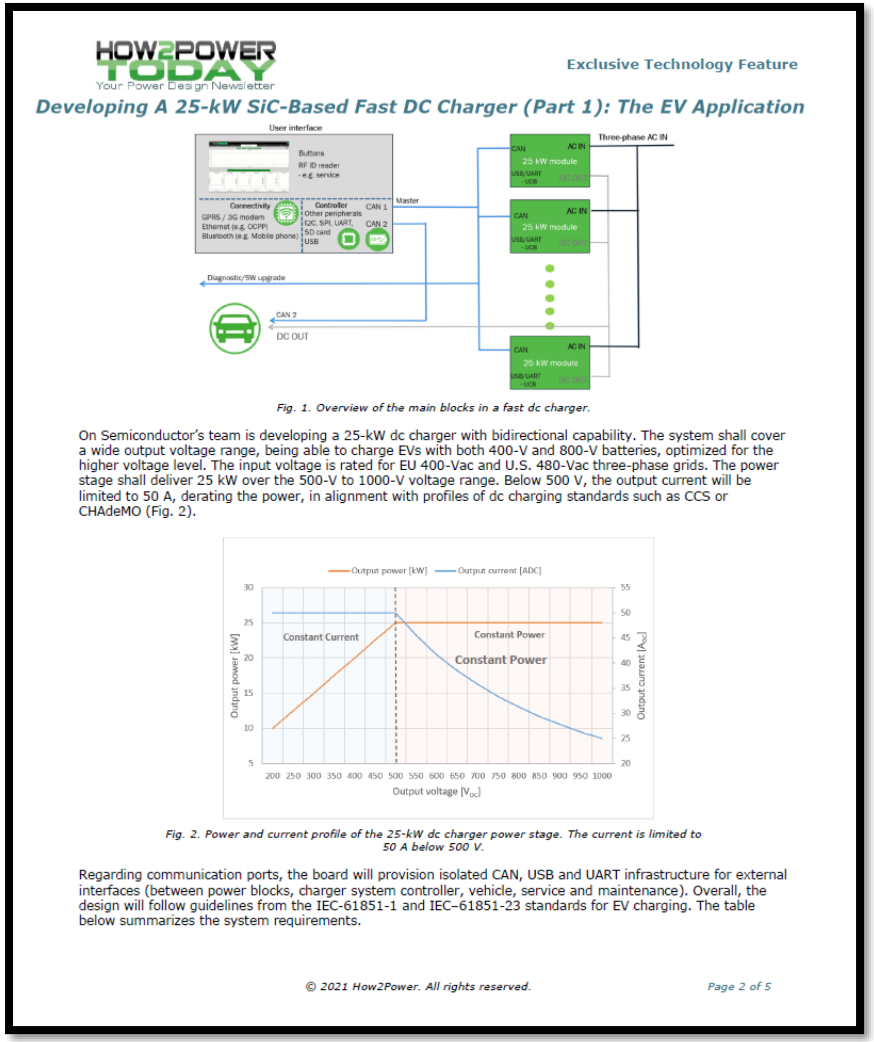
*TBD

Key BOM parts

Functional Block	Description	WPN
Power modules	Half Bridge SiC – Module 2-PACK 1200 V / 10 mOhm	NXH010P120MNF1PTG
SiC driver system	Galvanic isolated high current and high efficiency	NCD57000
	Isolated driver supply	Based on **SECO-LVDCDC-3064-SIC-GEVB** using **NCV3064** buck/boost
Auxiliary Power	Auxiliary Power supply	Based on **SECO-HVDCDC1362-40W15V** using **NCV1362** PSR quasi-resonant flyback / **NVH4L0160N120SC1** 160mOhm SiC
Sensing	12-Bit Low Power SAR ADC Signed Output	NCD9801x
	High Speed Dual-Channel, Bi-Directional Ceramic Digital Isolator	NCID9211
	CSA, 26V, Bidirectional Current Shunt Monitor	NCS21x

Join us in our development journey! Blog series

Learn how to develop a 25 kW fast EV charger stage with ON Semiconductor



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Developing A 25-kW SiC-Based Fast DC Charger (Part 1): The EV Application

Fig. 1. Overview of the main blocks in a fast dc charger.

On Semiconductor's team is developing a 25-kW dc charger with bidirectional capability. The system shall cover a wide output voltage range, being able to charge EVs with both 400-V and 800-V batteries, optimized for the higher voltage level. The input voltage is rated for EU 400-Vac and U.S. 480-Vac three-phase grids. The power stage shall deliver 25 kW over the 500-V to 1000-V voltage range. Below 500 V, the output current will be limited to 50 A, derating the power, in alignment with profiles of dc charging standards such as CCS or CHAdeMO (Fig. 2).

Fig. 2. Power and current profile of the 25-kW dc charger power stage. The current is limited to 50 A below 500 V.

Regarding communication ports, the board will provision isolated CAN, USB and UART infrastructure for external interfaces (between power blocks, charger system controller, vehicle, service and maintenance). Overall, the design will follow guidelines from the IEC-61851-1 and IEC–61851-23 standards for EV charging. The table below summarizes the system requirements.

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Examples of topics

Developing the Power Factor Correction (PFC) rectification stage
Developing the Dual Active Full Bridge DC/DC stage
A closer look to modulation schemes
The driving systems for silicon-carbide (SiC) power modules
Auxiliary power units from 800 V bus

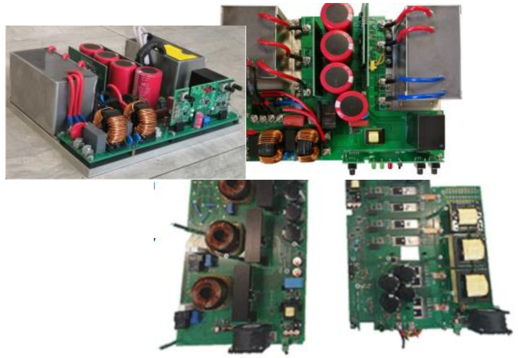
Timeline

Launch April and monthly until October.

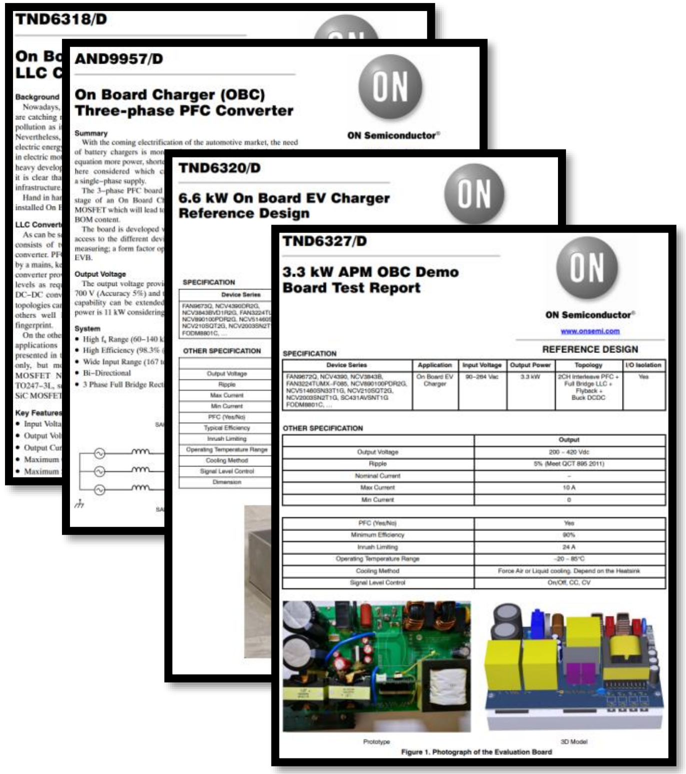
Stay tuned at ‚How2Power‘ and Fast EV Charging site

Support program for reference designs

Get your hands on our design boards

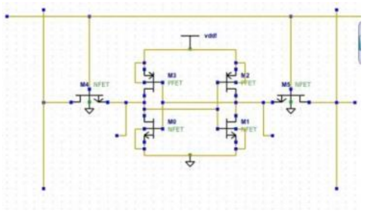


Application & design notes & blogs

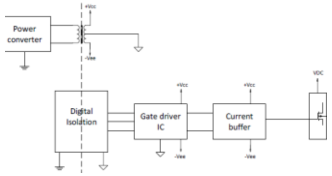


Development results as we go

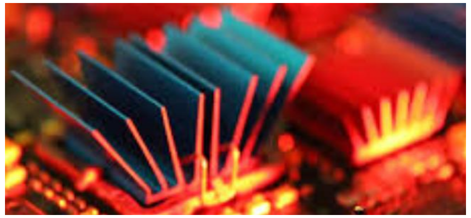
SPICE simulation



Drivers design



Thermal management



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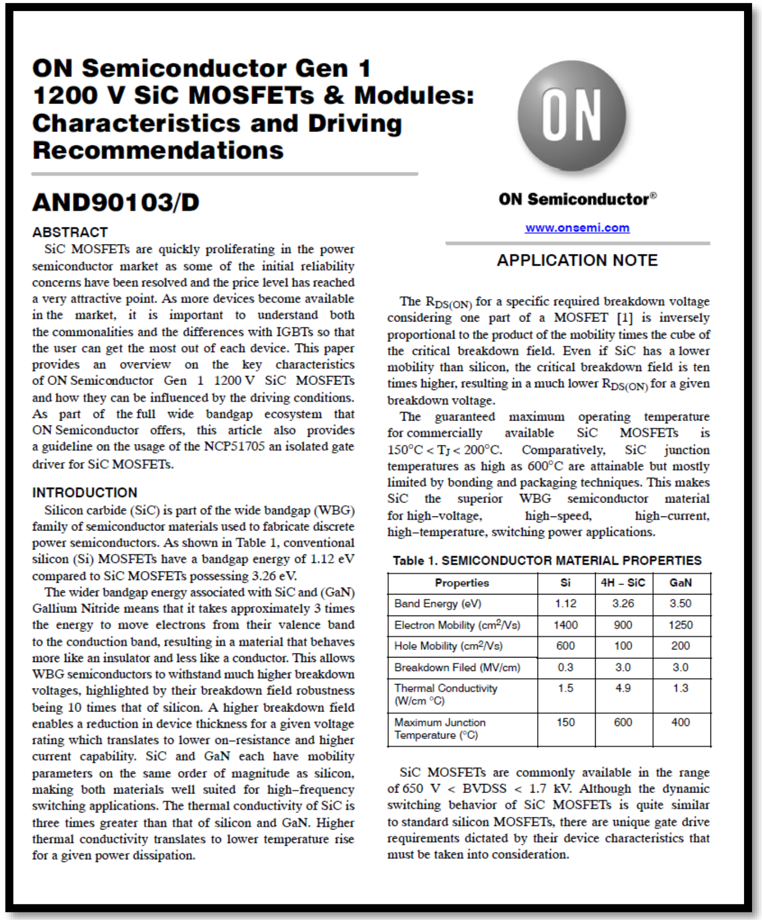
Learn with us about Fast DC EV Charging technologies

Find out more

SiC 1200 V Gen 1 Characteristics and Driving Recommendations


ON Semiconductor Gen 1 1200 V SiC MOSFETs & Modules: Characteristics and Driving Recommendations

AND90103/D

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APPLICATION NOTE

ABSTRACT

SiC MOSFETs are quickly proliferating in the power semiconductor market as some of the initial reliability concerns have been resolved and the price level has reached a very attractive point. As more devices become available in the market, it is important to understand both the commonalities and the differences with IGBTs so that the user can get the most out of each device. This paper provides an overview on the key characteristics of ON Semiconductor Gen 1 1200 V SiC MOSFETs and how they can be influenced by the driving conditions. As part of the full wide bandgap ecosystem that ON Semiconductor offers, this article also provides a guideline on the usage of the NCP51705 an isolated gate driver for SiC MOSFETs.

INTRODUCTION

Silicon carbide (SiC) is part of the wide bandgap (WBG) family of semiconductor materials used to fabricate discrete power semiconductors. As shown in Table 1, conventional silicon (Si) MOSFETs have a bandgap energy of 1.12 eV compared to SiC MOSFETs possessing 3.26 eV.

The wider bandgap energy associated with SiC and (GaN) Gallium Nitride means that it takes approximately 3 times the energy to move electrons from their valence band to the conduction band, resulting in a material that behaves more like an insulator and less like a conductor. This allows WBG semiconductors to withstand much higher breakdown voltages, highlighted by their breakdown field robustness being 10 times that of silicon. A higher breakdown field enables a reduction in device thickness for a given voltage rating which translates to lower on–resistance and higher current capability. SiC and GaN have mobility parameters on the same order of magnitude as silicon, making both materials well suited for high–frequency switching applications. The thermal conductivity of SiC is three times greater than that of silicon and GaN. Higher thermal conductivity translates to lower temperature rise for a given power dissipation.

The $R_{DS(ON)}$ for a specific required breakdown voltage considering one part of a MOSFET [1] is inversely proportional to the product of the mobility times the cube of the critical breakdown field. Even if SiC has a lower mobility than silicon, the critical breakdown field is ten times higher, resulting in a much lower $R_{DS(ON)}$ for a given breakdown voltage.

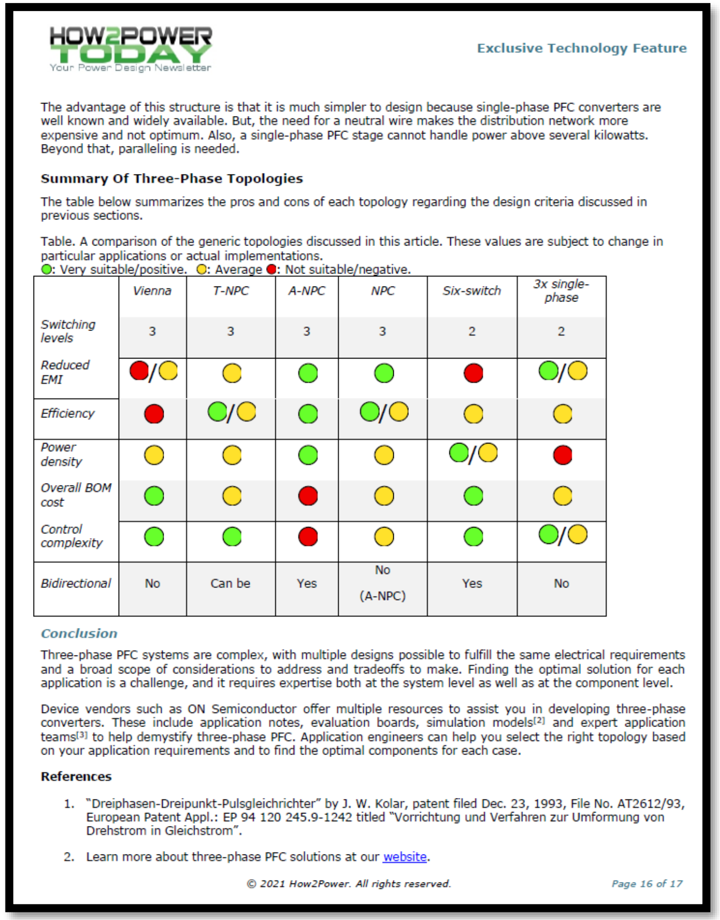
The guaranteed maximum operating temperature for commercially available SiC MOSFETs is 150°C < T_J < 200°C. Comparatively, SiC junction temperatures as high as 600°C are attainable but mostly limited by bonding and packaging techniques. This makes SiC the superior WBG semiconductor material for high–voltage, high–speed, high–current, high–temperature, switching power applications.

Table 1. SEMICONDUCTOR MATERIAL PROPERTIES

Properties	Si	4H – SiC	GaN
Band Energy (eV)	1.12	3.26	3.50
Electron Mobility (cm²/Vs)	1400	900	1250
Hole Mobility (cm²/Vs)	600	100	200
Breakdown Filed (MV/cm)	0.3	3.0	3.0
Thermal Conductivity (W/cm °C)	1.5	4.9	1.3
Maximum Junction Temperature (°C)	150	600	400

SiC MOSFETs are commonly available in the range of 650 V < BVDSS < 1.7 kV. Although the dynamic switching behavior of SiC MOSFETs is quite similar to standard silicon MOSFETs, there are unique gate drive requirements dictated by their device characteristics that must be taken into consideration.

Demystifying 3-phase PFCs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The advantage of this structure is that it is much simpler to design because single-phase PFC converters are well known and widely available. But, the need for a neutral wire makes the distribution network more expensive and not optimum. Also, a single-phase PFC stage cannot handle power above several kilowatts. Beyond that, paralleling is needed.

Summary Of Three-Phase Topologies

The table below summarizes the pros and cons of each topology regarding the design criteria discussed in previous sections.

Table. A comparison of the generic topologies discussed in this article. These values are subject to change in particular applications or actual implementations.
●: Very suitable/positive. ●: Average ●: Not suitable/negative.

	Vienna	T-NPC	A-NPC	NPC	Six-switch	3x single-phase
Switching levels	3	3	3	3	2	2
Reduced EMI	●/●	●	●	●	●	●/●
Efficiency	●	●/●	●	●/●	●	●
Power density	●	●	●	●	●/●	●
Overall BOM cost	●	●	●	●	●	●
Control complexity	●	●	●	●	●	●/●
Bidirectional	No	Can be	Yes	No (A-NPC)	Yes	No

Conclusion

Three-phase PFC systems are complex, with multiple designs possible to fulfill the same electrical requirements and a broad scope of considerations to address and tradeoffs to make. Finding the optimal solution for each application is a challenge, and it requires expertise both at the system level as well as at the component level.

Device vendors such as ON Semiconductor offer multiple resources to assist you in developing three-phase converters. These include application notes, evaluation boards, simulation models[2] and expert application teams[3] to help demystify three-phase PFC. Application engineers can help you select the right topology based on your application requirements and to find the optimal components for each case.

References

1. "Dreiphasen-Dreipunkt-Pulsgleichrichter" by J. W. Kolar, patent filed Dec. 23, 1993, File No. AT2612/93, European Patent Appl.: EP 94 120 245.9-1242 titled "Vorrichtung und Verfahren zur Umformung von Drehstrom in Gleichstrom".
2. Learn more about three-phase PFC solutions at our website.

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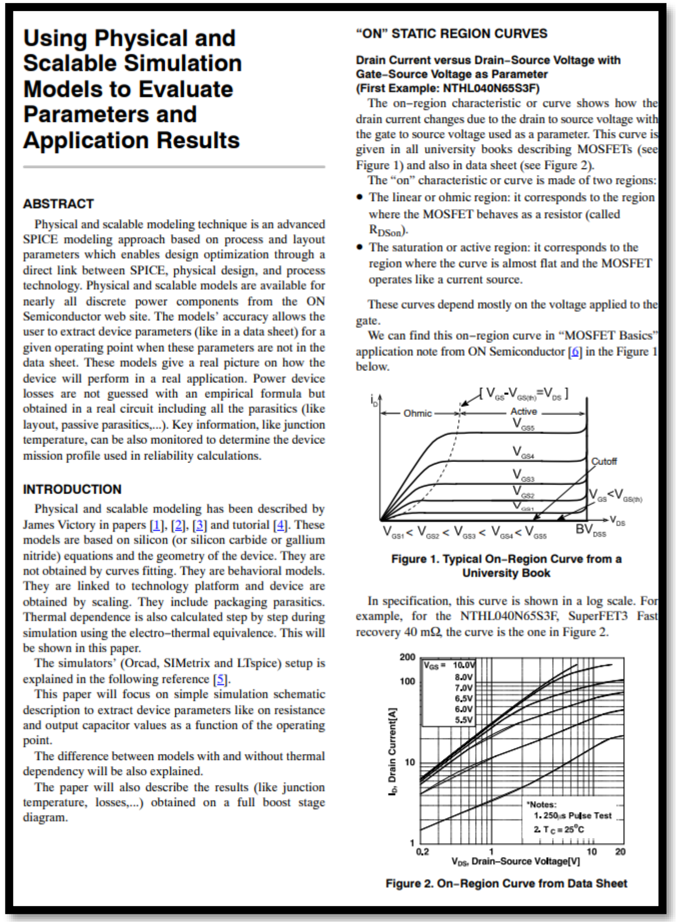
Using Physical and Scalable Simulation Models to Evaluate Parameters and Application Results '


Using Physical and Scalable Simulation Models to Evaluate Parameters and Application Results

ABSTRACT

Physical and scalable modeling technique is an advanced SPICE modeling approach based on process and layout parameters which enables design optimization through a direct link between SPICE, physical design, and process technology. Physical and scalable models are available for nearly all discrete power components from the ON Semiconductor web site. The models' accuracy allows the user to extract device parameters (like in a data sheet) for a given operating point when these parameters are not in the data sheet. These models give a real picture on how the device will perform in a real application. Power device losses are not given with an empirical formula but obtained in a real circuit including all the parasitics (like layout, passive parasitics,...). Key information, like junction temperature, can be also monitored to determine the device mission profile used in reliability calculations.

INTRODUCTION

Physical and scalable modeling has been described by James Victory in papers [1], [2], [3] and tutorial [4]. These models are based on silicon (or silicon carbide or gallium nitride) equations and the geometry of the device. They are not obtained by curves fitting. They are behavioral models. They are linked to technology platform and device are obtained by scaling. They include packaging parasitics. Thermal dependence is also calculated step by step during simulation using the electro–thermal equivalence. This will be shown in this paper.

The simulators' (Orcad, SIMetrix and LTspice) setup is explained in the following reference [5].

This paper will focus on simple simulation schematic description to extract device parameters like on resistance and output capacitor values as a function of the operating point.

The difference between models with and without thermal dependency will be also explained.

The paper will also describe the results (like junction temperature, losses,...) obtained on a full boost stage diagram.

"ON" STATIC REGION CURVES

Drain Current versus Drain–Source Voltage with Gate–Source Voltage as Parameter (First Example: NTHL040N65S3F)

The on–region characteristic or curve shows how the drain current changes due to the drain to source voltage with the gate to source voltage used as a parameter. This curve is given in all university books describing MOSFETs (see Figure 1) and also in data sheet (see Figure 2).

The "on" characteristic or curve is made of two regions:

- The linear or ohmic region: it corresponds to the region where the MOSFET behaves as a resistor (called R_{DSon}).
- The saturation or active region: it corresponds to the region where the curve is almost flat and the MOSFET operates like a current source.

These curves depend mostly on the voltage applied to the gate.

We can find this on–region curve in "MOSFET Basics" application note from ON Semiconductor [6] in the Figure 1 below.

Figure 1. Typical On–Region Curve from a University Book

In specification, this curve is shown in a log scale. For example, for the NTHL040N65S3F, SuperFET3 Fast recovery 40 mΩ, the curve is the one in Figure 2.

Figure 2. On–Region Curve from Data Sheet

Thank you

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