SiC Simulations with Physical & Scalable Models

Tips and Applications

Didier Balocco

EMEA Business Marketing Engineer

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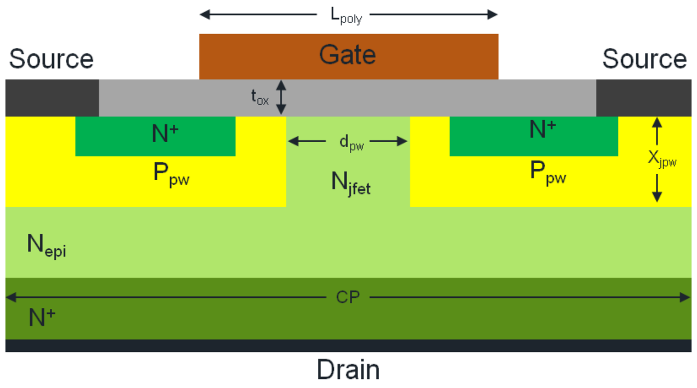
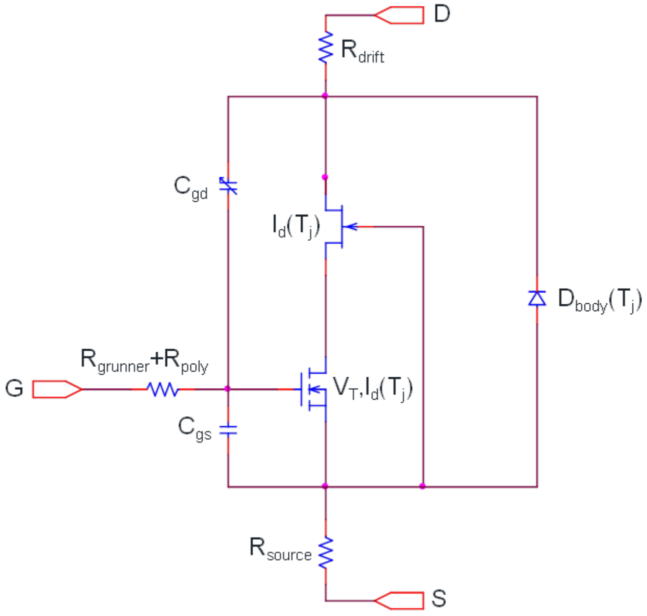
Why Physical & Scalable models are the Best ?

Physically Based SPICE Models for SiC MOSFETs

Each zone inside the physical structure is modeled by a device.
Each device equation considers dimensions and physics quantities
- Current density, Electrical field, Temperature, …



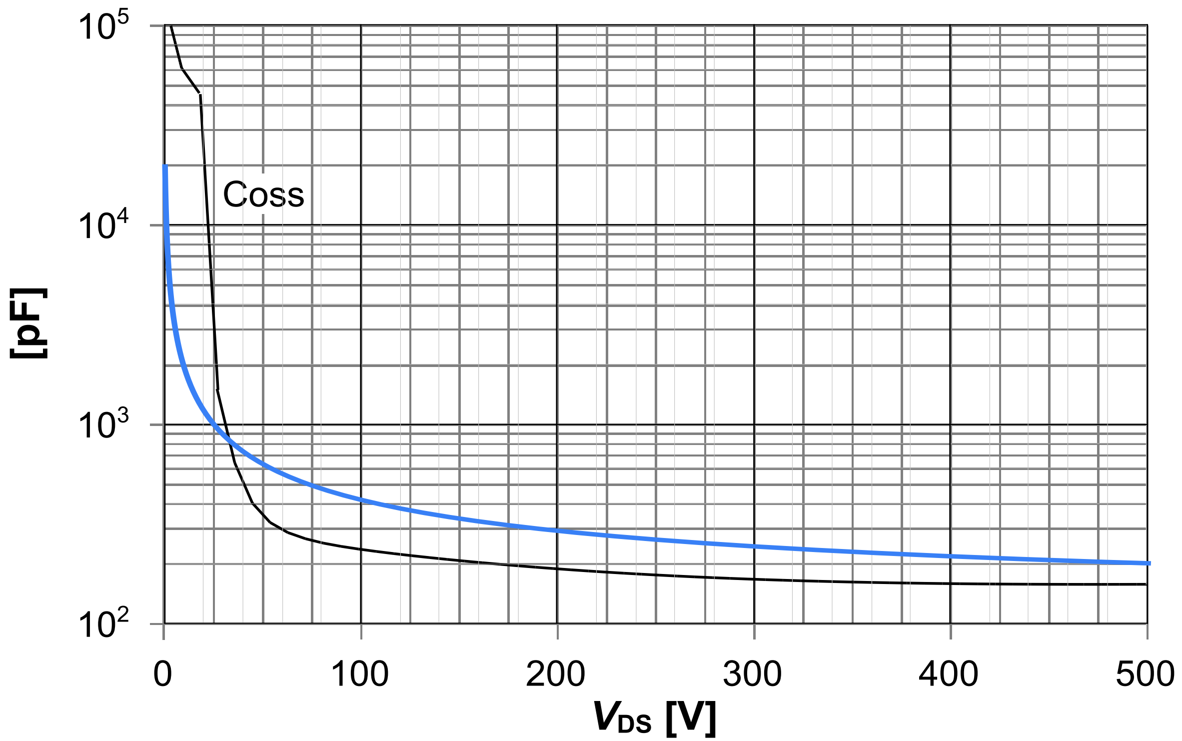


Physical Structure → Physical & Scalable Model

- Contains
  - SiC Physics Equations
  - One model per Technology
  - Electro-Thermal
  - Can predict performances of not available parts…
- Benefits
  - Accurate, consistent, and correlated with process variation modeling
  - Best IC industry standard practice

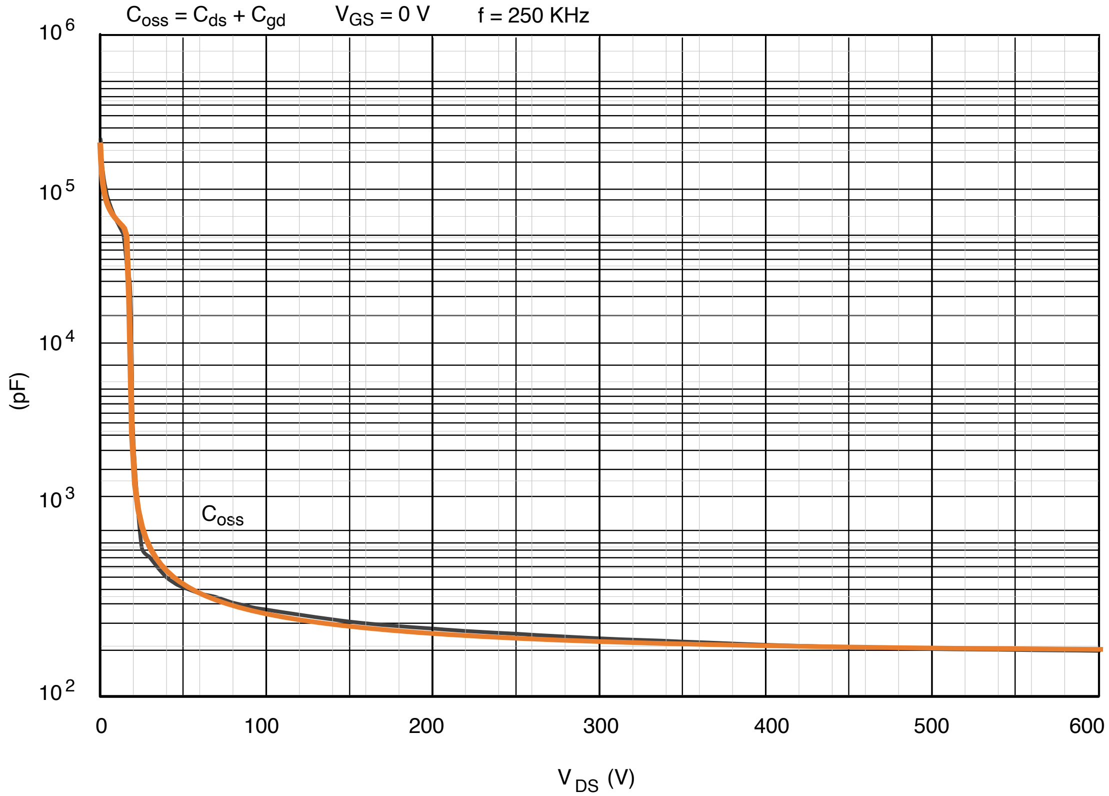
SuperJunction Output Capacitor (Coss) Simulation

- **With Behavioral Model**



✗ It is clear the behavioral model cannot capture the nearly 3-decade drop in output capacitance inherent to all Super-Junctions

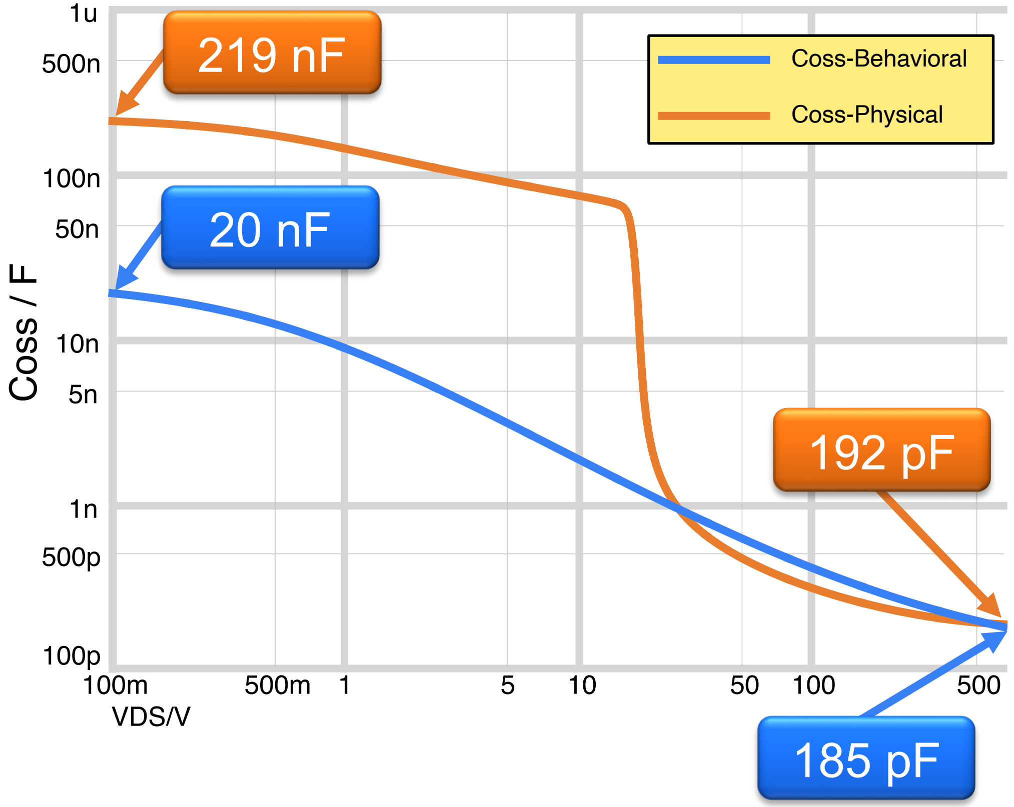
- **With Physical & Scalable Model**



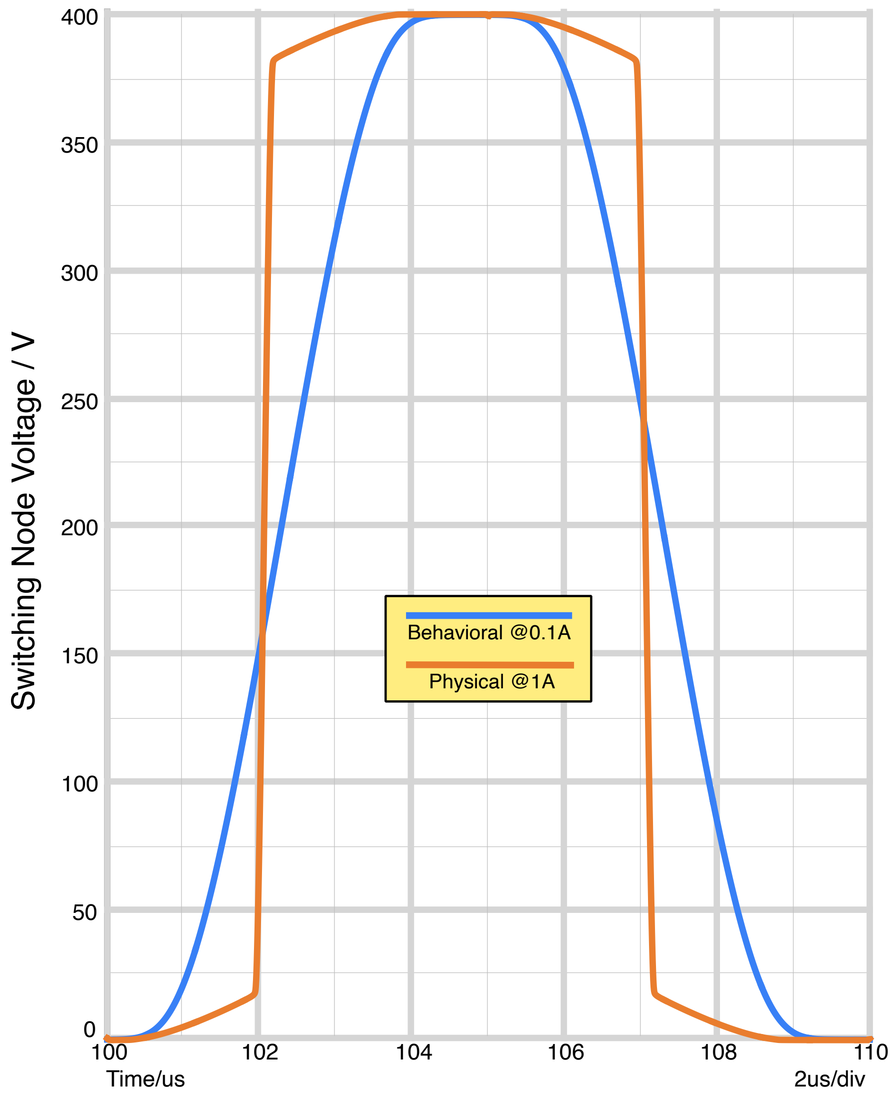
✓ Physical & Scalable well predicts the 3-decade drop in Coss.

Resonant Transition Simulation under Constant Current

Coss comparison



Resonant Transition



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Physical & Scalable Simulation Model Capabilities

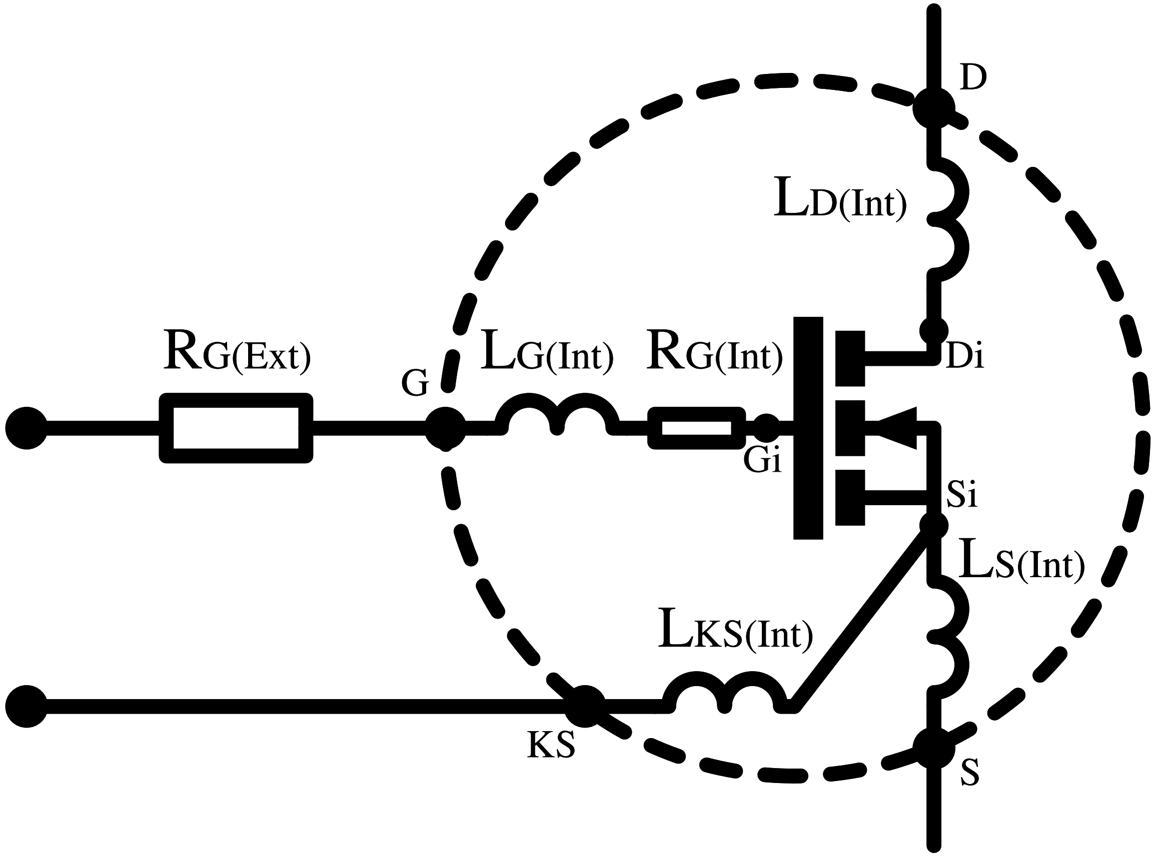
Tips and Interesting Results

Die Nodes Access Inside the Package

What is happening internally ?

Access Die Nodes

- Schematic



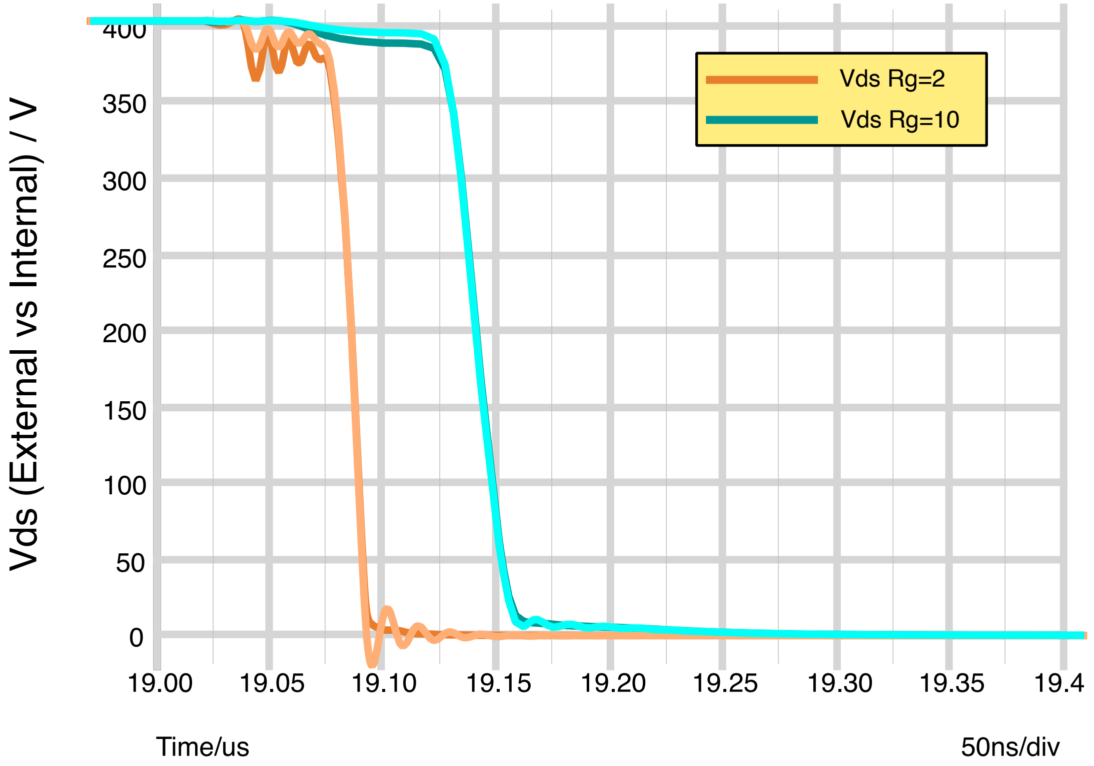
- Internal node manes :
  - Ends with a ‘i’
  - In SIMetrix : like ‘**Q**n:xy:**di**’

- Useful to study package parasitic impedances effects on waveforms…

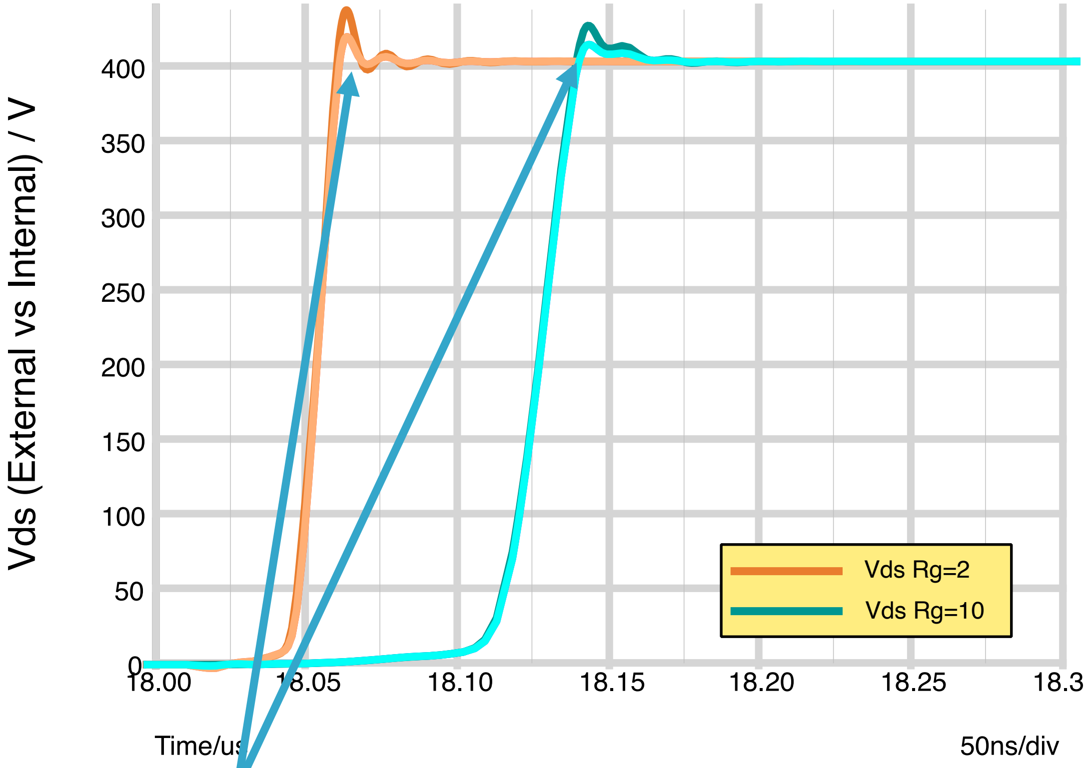
Drain-to-Source voltage differences

Light-colored = Die nodes
Dark-colored = Pin nodes

- **Turn-ON**



- **Turn-OFF**



Less overvoltage stress on the die than seen on the pins

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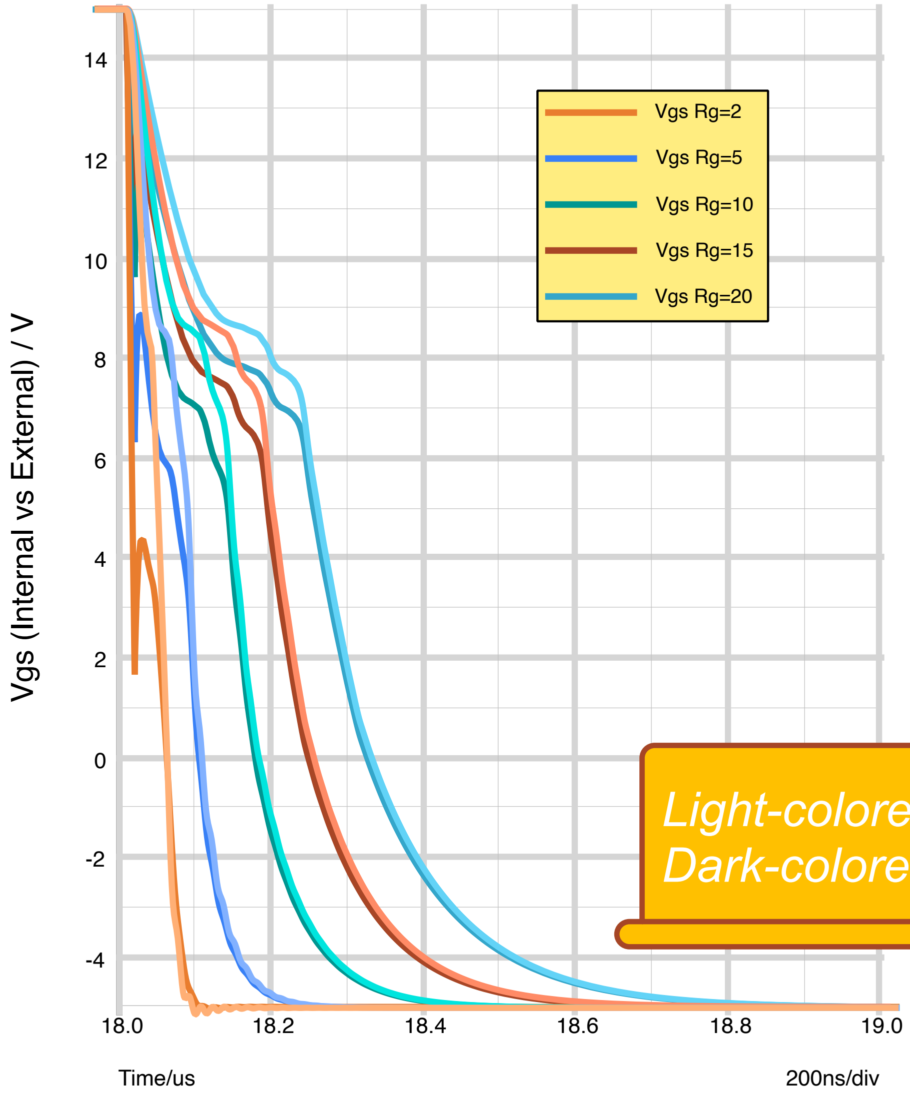
Gate-to-Source voltage differences vs External Gate Resistor

MOSFET with LOW internal Rg

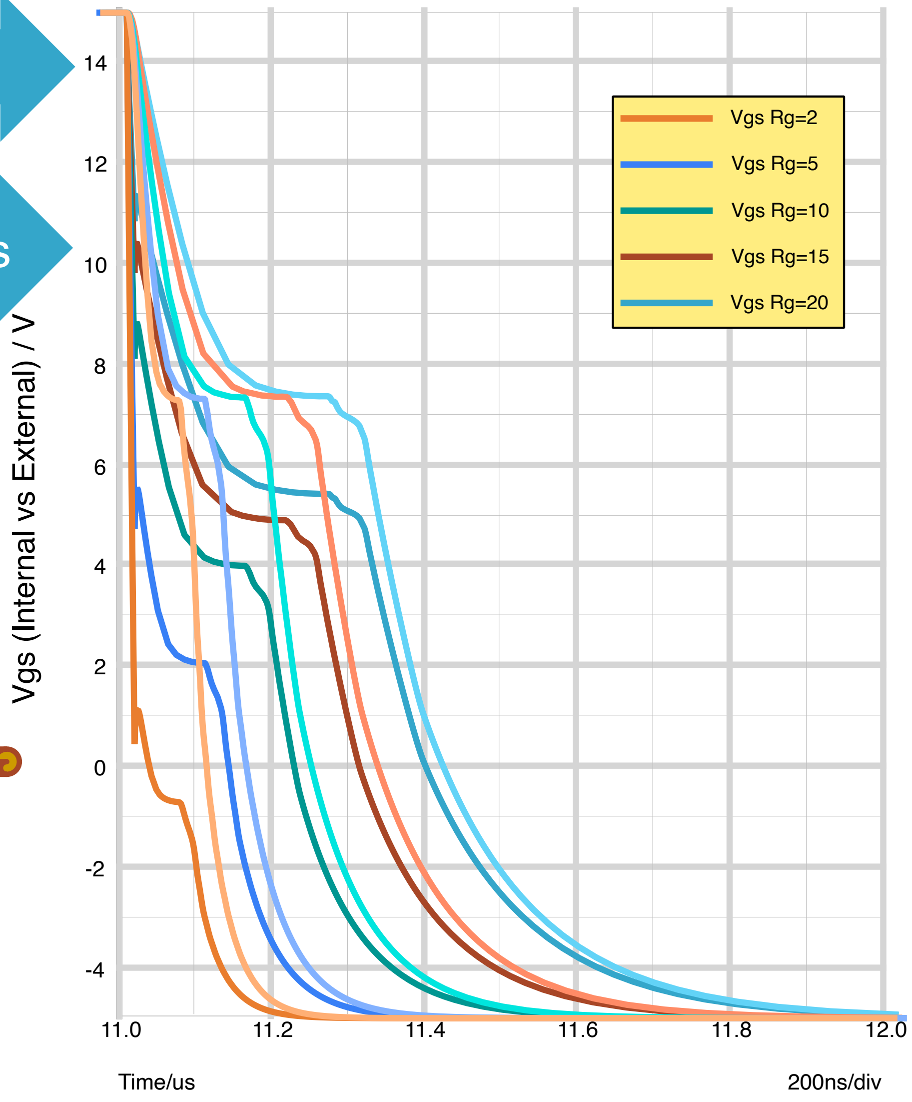


More delay

Less Ringings

Light-colored = Die nodes
Dark-colored = Pin nodes

MOSFET with HIGH internal Rg



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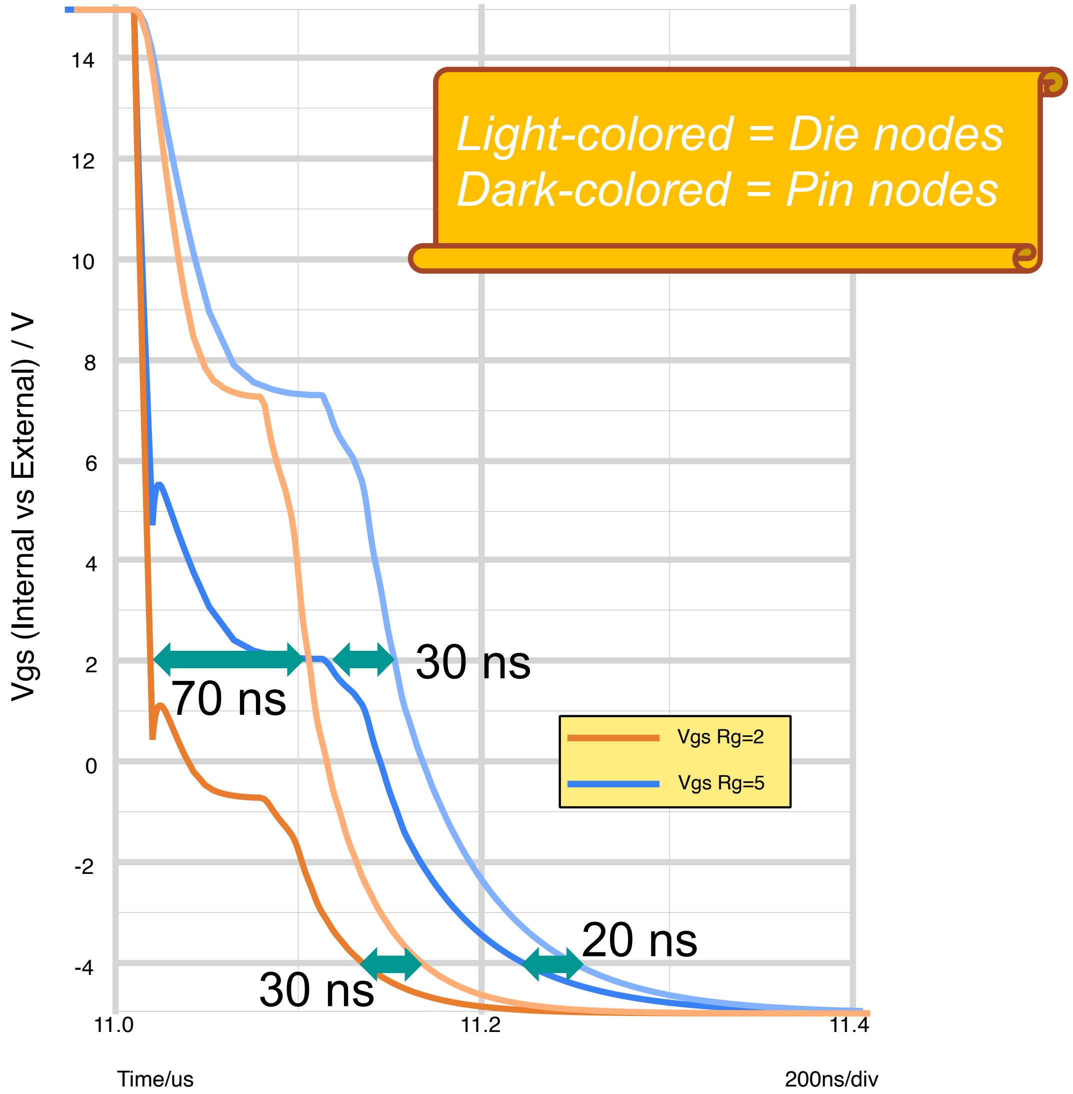
Gate-to-Source voltage differences vs External Gate Resistor

Impact…

- The delays between external gate signal and internal gate signal when crossing the Threshold are :
  - For Rg = 5 Ω ➡ Delay = 30 ns
  - For Rg = 2 Ω ➡ Delay = 70 ns…
- It is a large difference !
- With High Internal Gate Resistance, In Half- or Full-Bridge, Wrong delays can lead malfunction…
  - ➢ Due to the bad information available when looking to external gate signal only.

MOSFET with HIGH internal Rg (Details)



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Corner Models

Nothing is Perfect…

Corner Models

- Models online are made and calibrated to give nominal or typical values
- Parameters have Gaussian distribution
- Corner models are the :
  - Maximum threshold device

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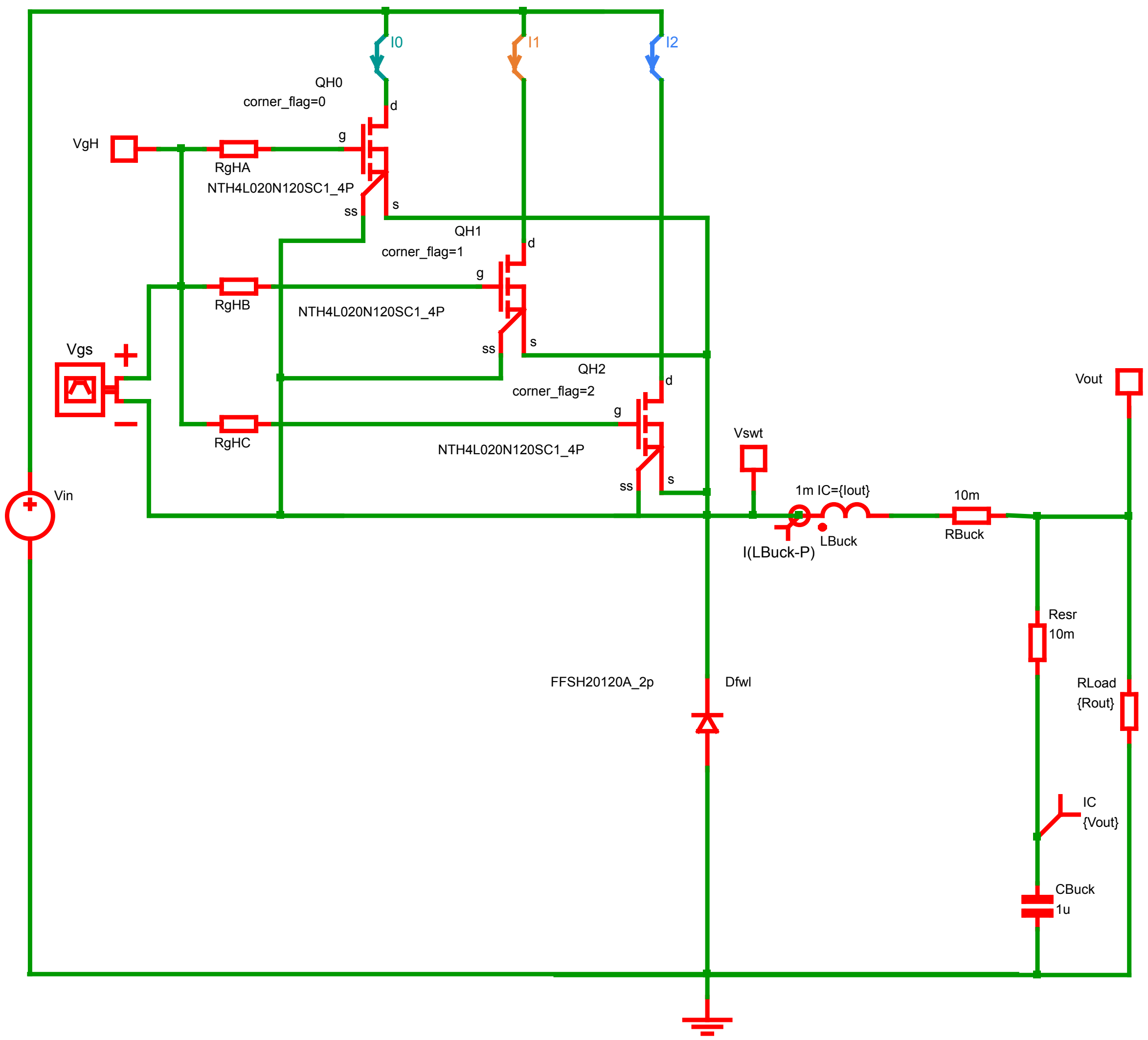
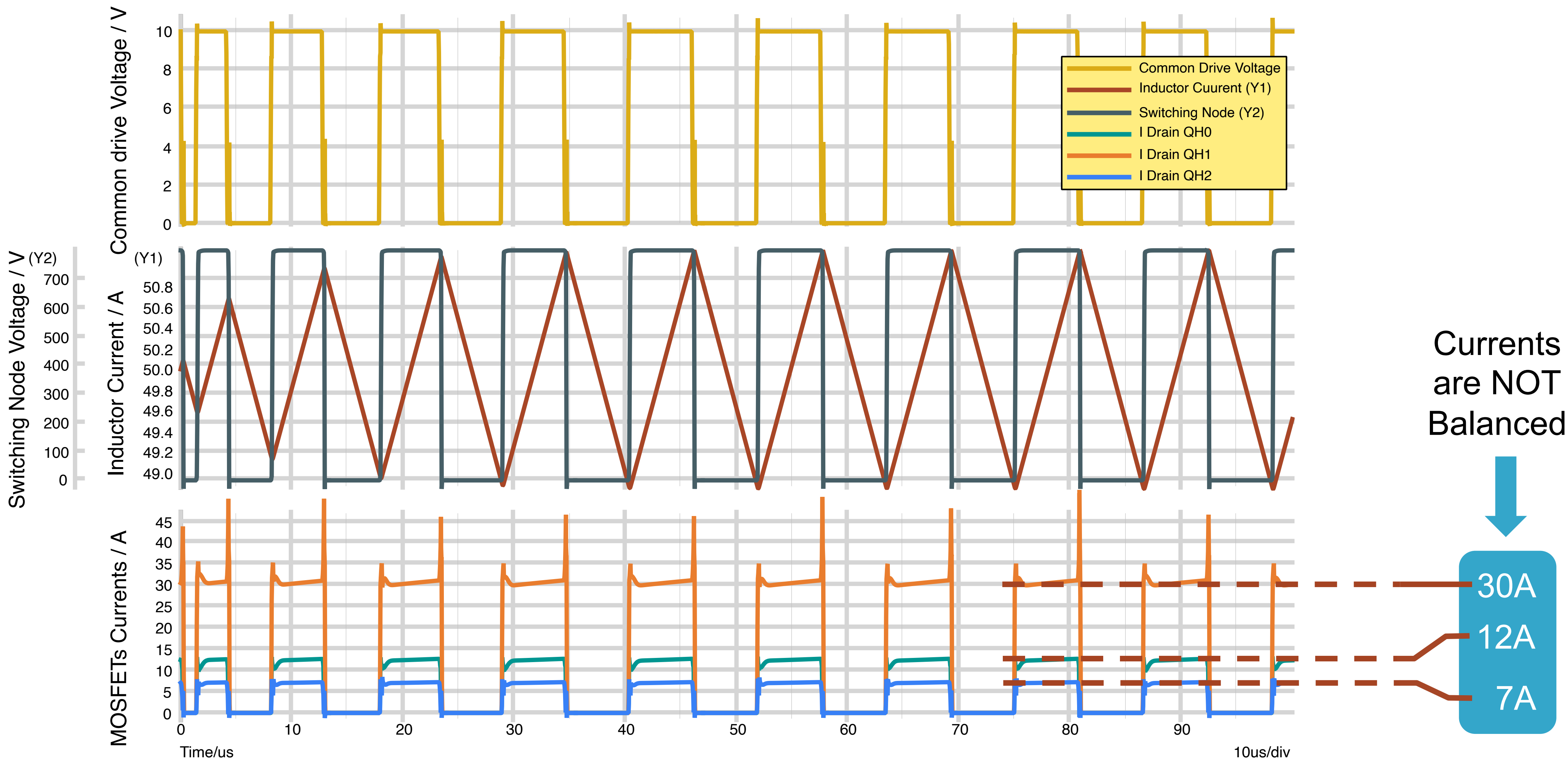
  - Minimum threshold device.
- What happens if we parallel them ?



Buck stage waveforms with Corner Models



Currents are NOT Balanced

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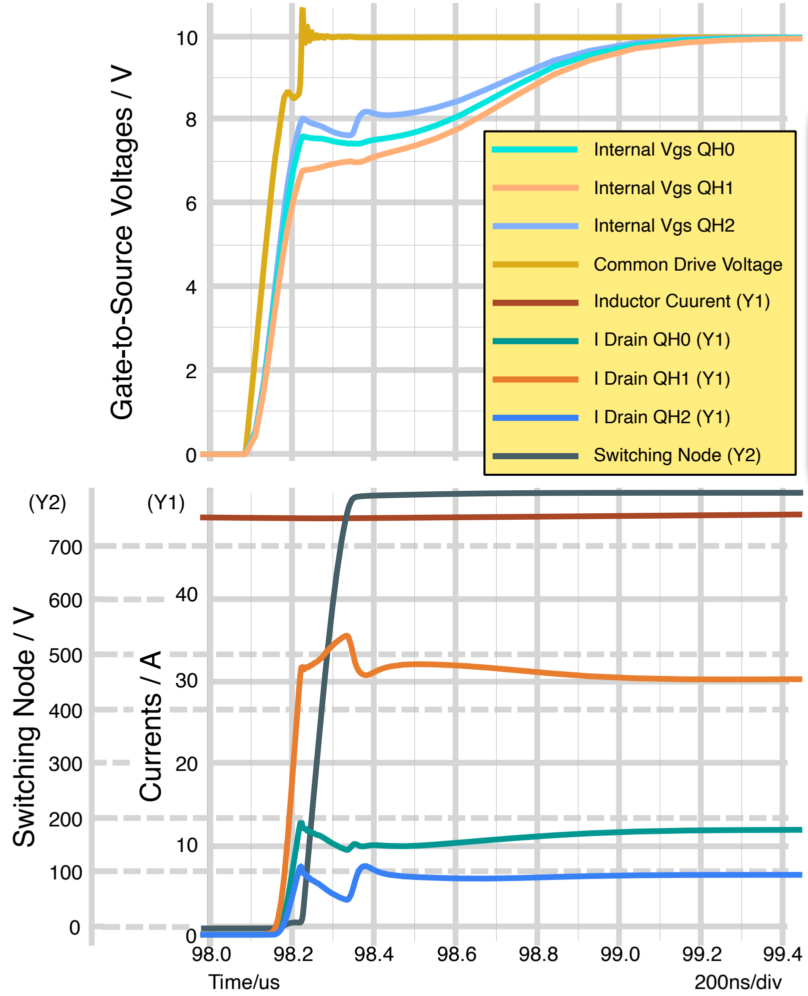
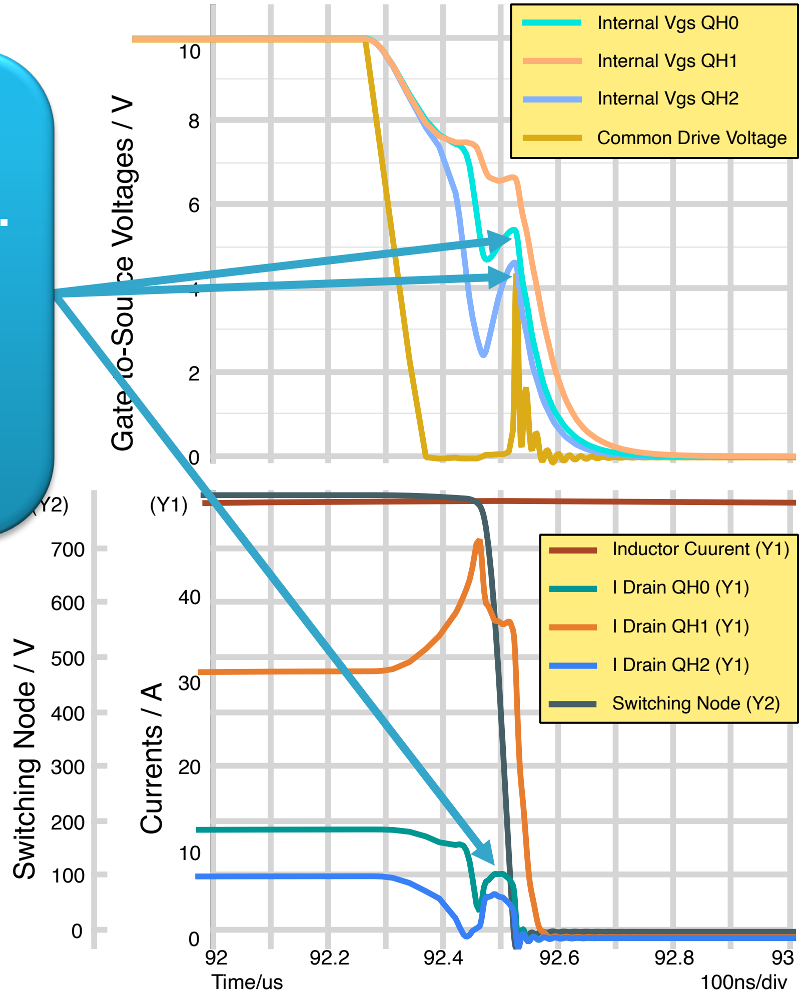
Buck stage waveforms with Corner Models

Light-colored = Die nodes
Dark-colored = Pin nodes

- **Turn-ON**

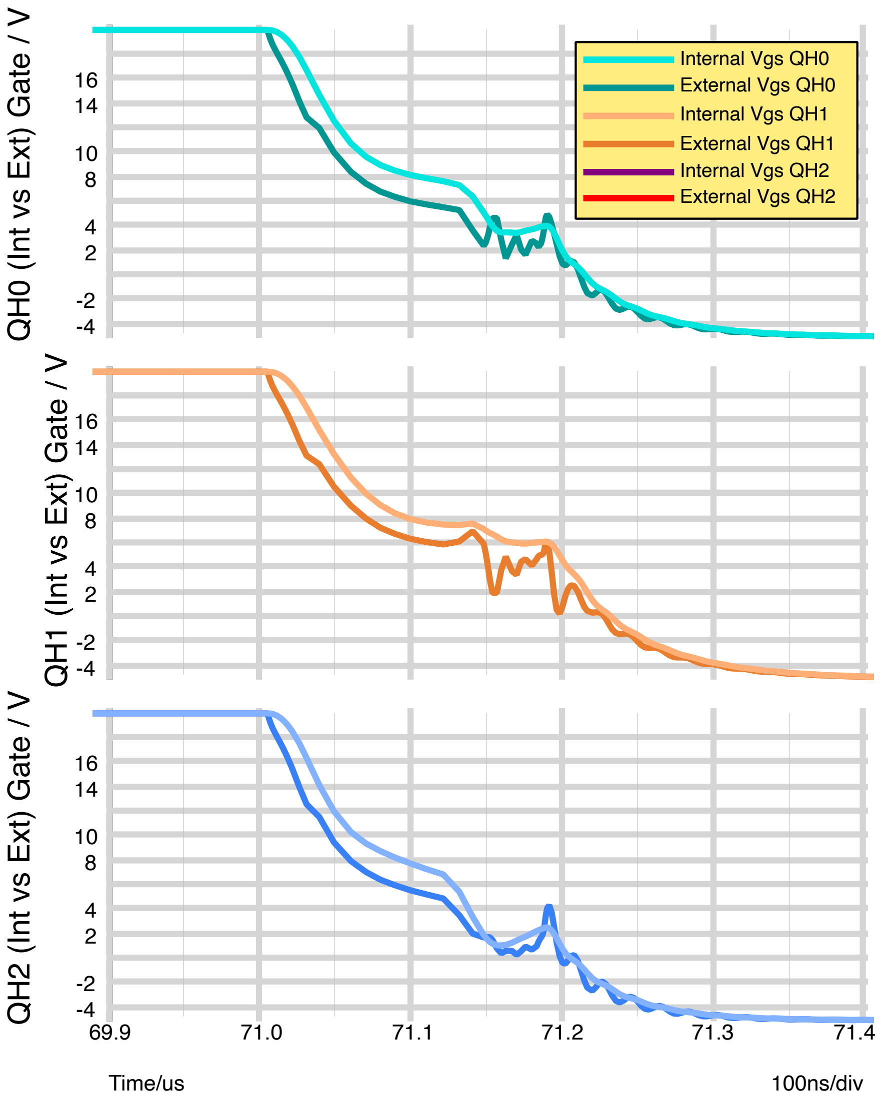


- **Turn-OFF**



During **Turn-OFF**, **QH0** and QH2 **restart** to **conduct.** It may be link to Gate-to-Source network (Internal+External) coupling

Buck stage waveforms with Corner Models



- We can see a lot of ringing on all external Gate-to-Kelvin Source waveforms…
- When QH0 and QH2 re-start to conduct, we have a peak of voltage above 2V (the threshold) on the internal Gate-to-Source waveforms.

Light-colored = Die nodes
Dark-colored = Pin nodes

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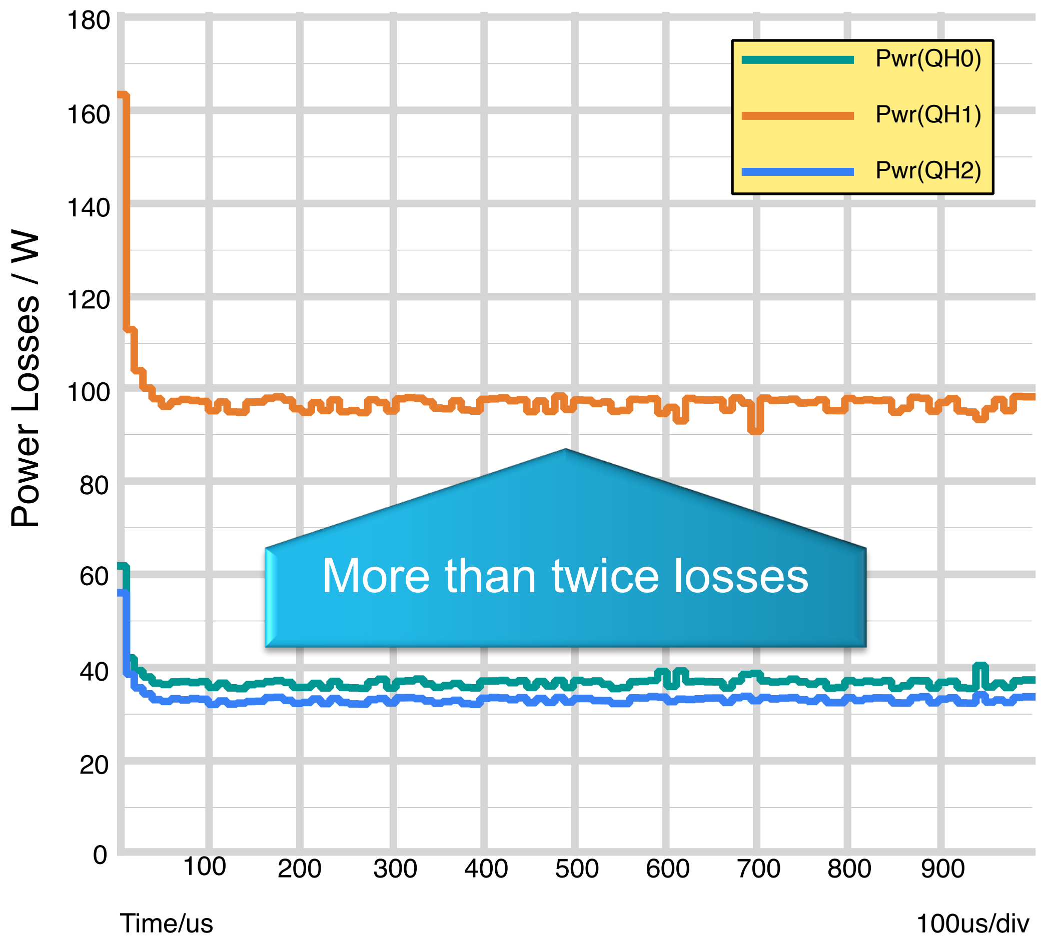
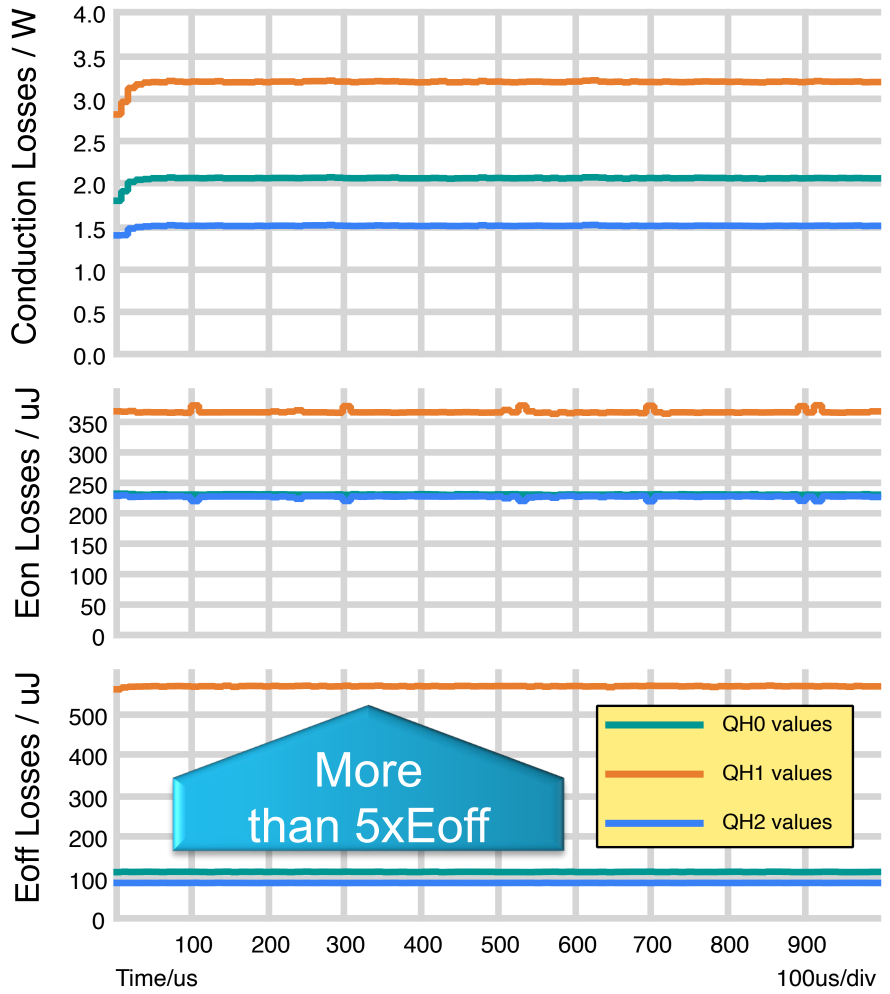
Buck stage waveforms with Corner Models

- **Losses (W)**



- **Energies (µJ)**



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Electro-Thermal Simulations

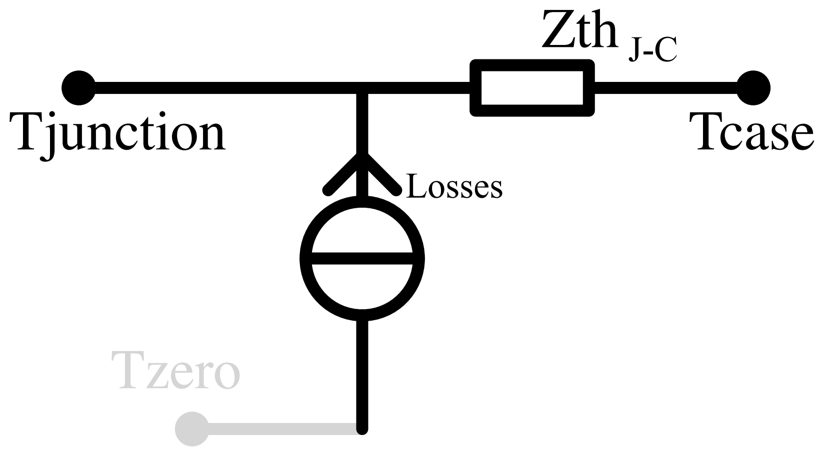
Using Cauer Networks.

Electro-Thermal simulations

- We can simulate thermal behaviors using the following equivalences :
  - Power flow => Current
  - Temperature => Voltage

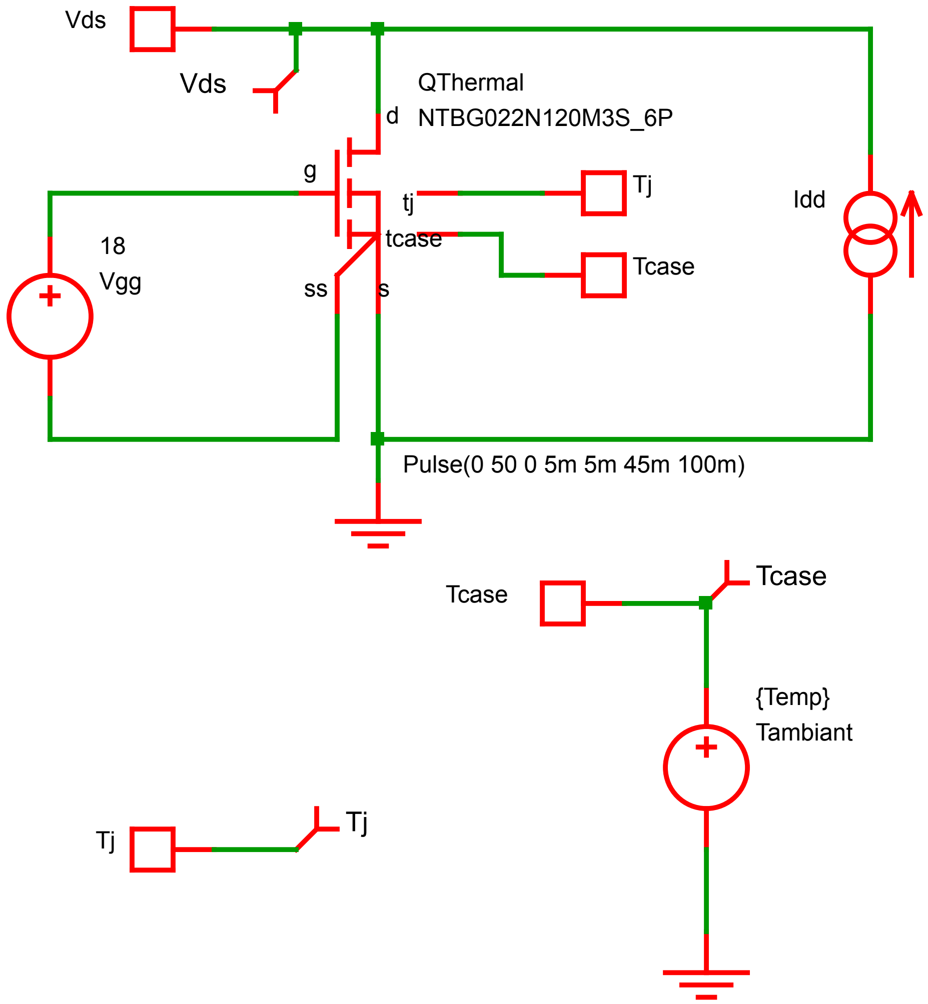
- Thermo-Electrical models have 2 extra pins :
  - Tcase = Case temperature
  - Tj = Junction temperature

- Thermo-Electrical models internal :



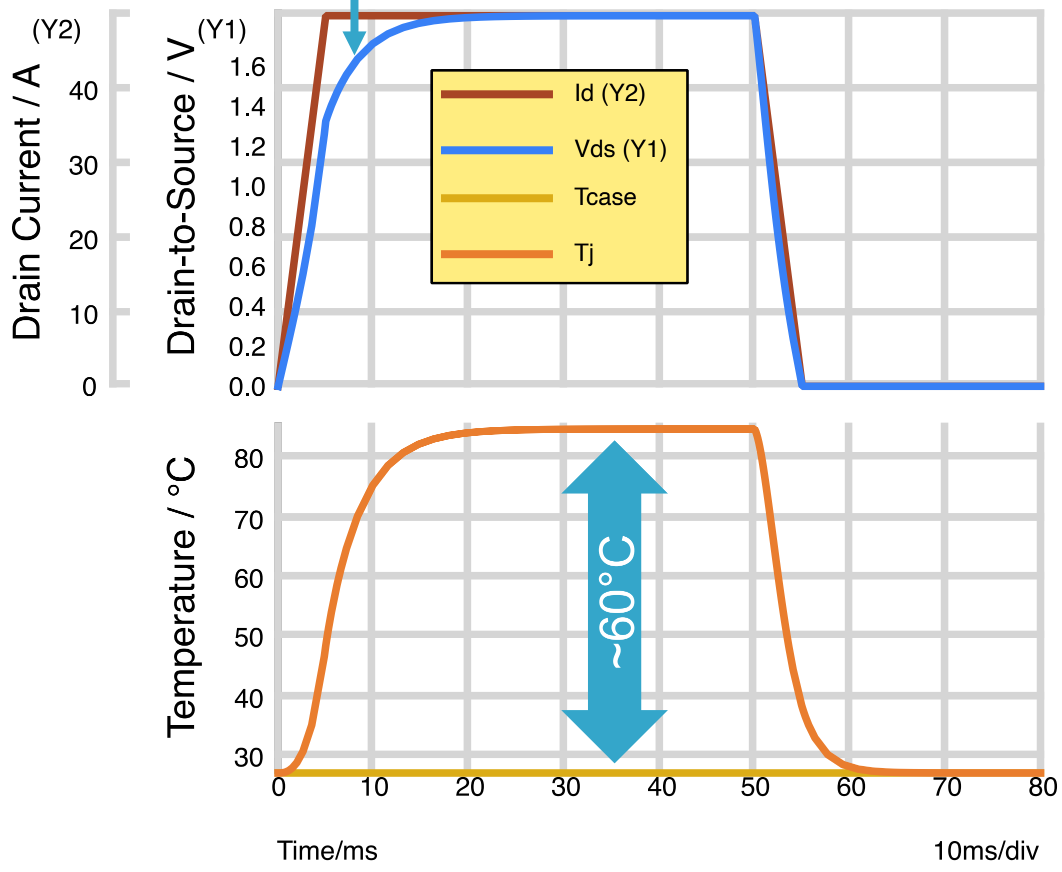
Electro-Thermal simulations : $\Delta T_{J\text{-}C}$

- **Simulation Schematic**



- **Results**

$R_{DS(on)}$ increases with Temperature



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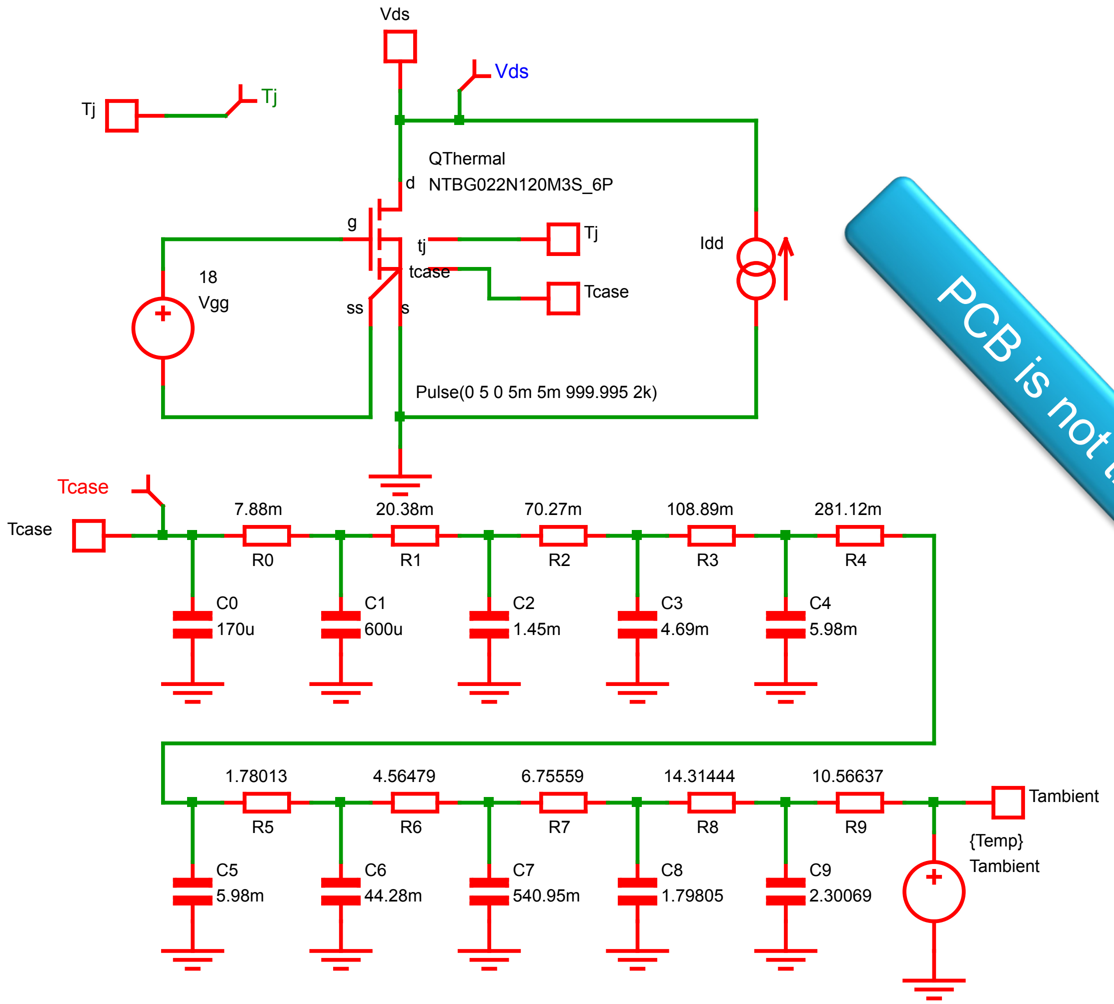
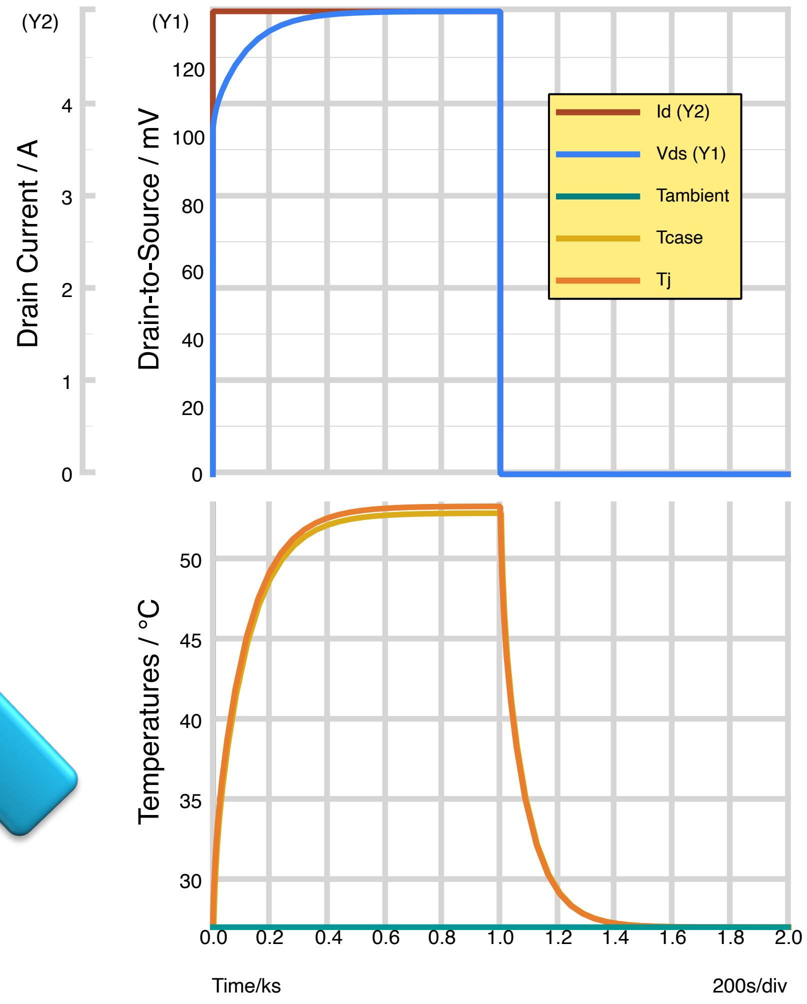
Electro-Thermal simulations : Heat Sink with Cauer network

- **Cauer network for 1-ich PCB**



PCB is not the best HeatSink

- **Results**



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Switching Losses vs V_{GS}, Package and Structure

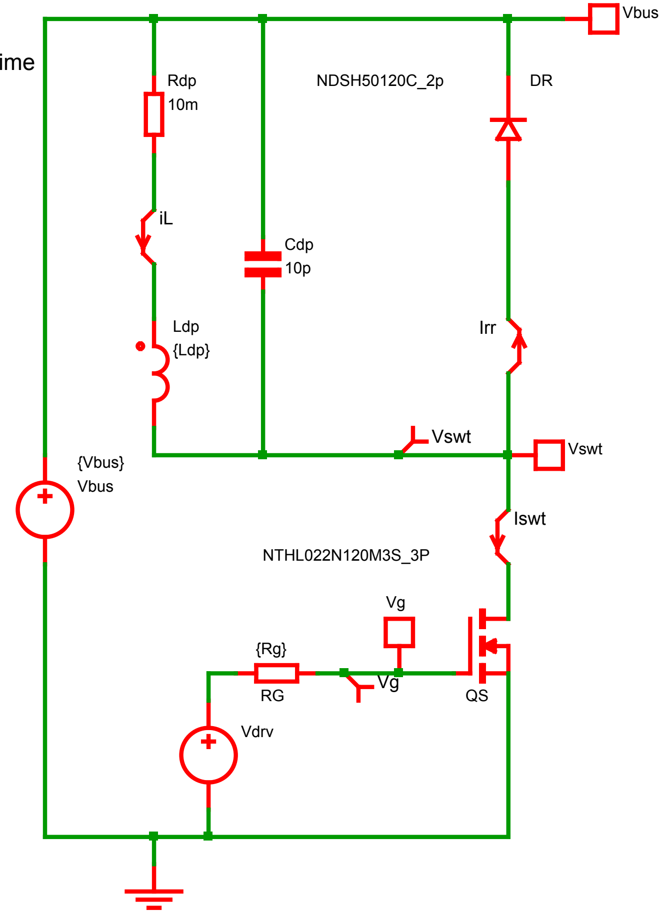
Using Double Pulse Measurement

Double Pulse Measurement Setup

- ## Schematic

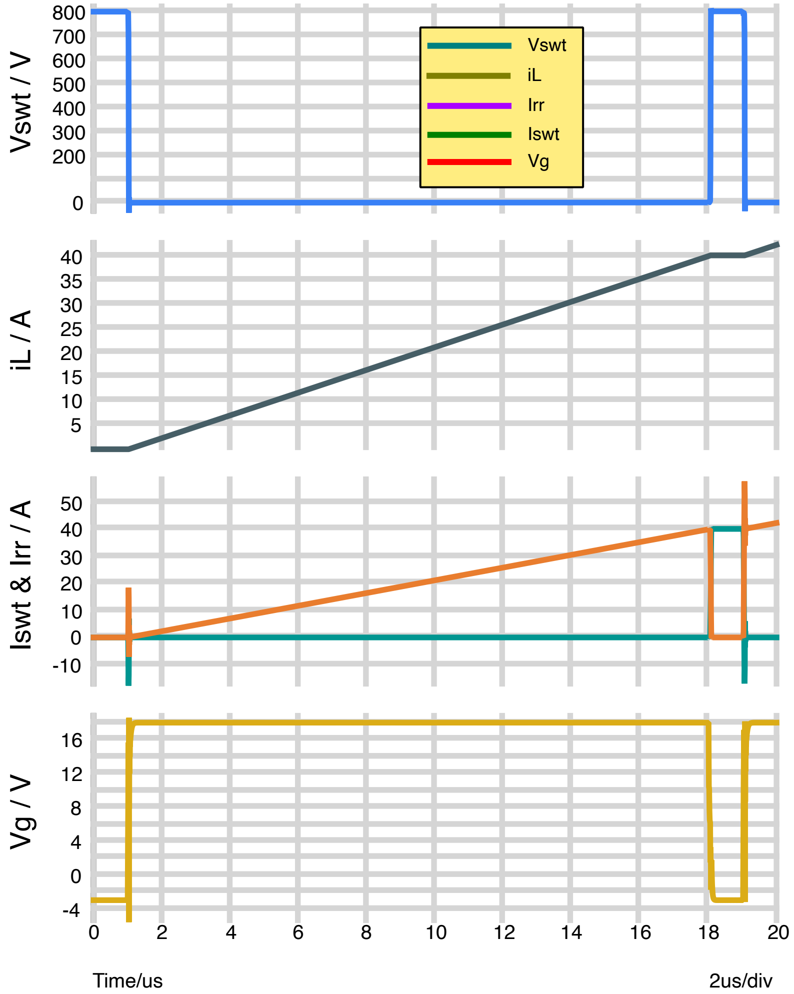
* Current and Voltage for Eon and Eoff measurement
.Param Im=40
.Param Vbus=800

* Driver parameters Rise & Fall time
.Param tRise=10n
.Param tFall=10n
* Driver output voltage
.Param vOn=18
.Param vOff=-3
* Gate series resistance
.Param Rg=5



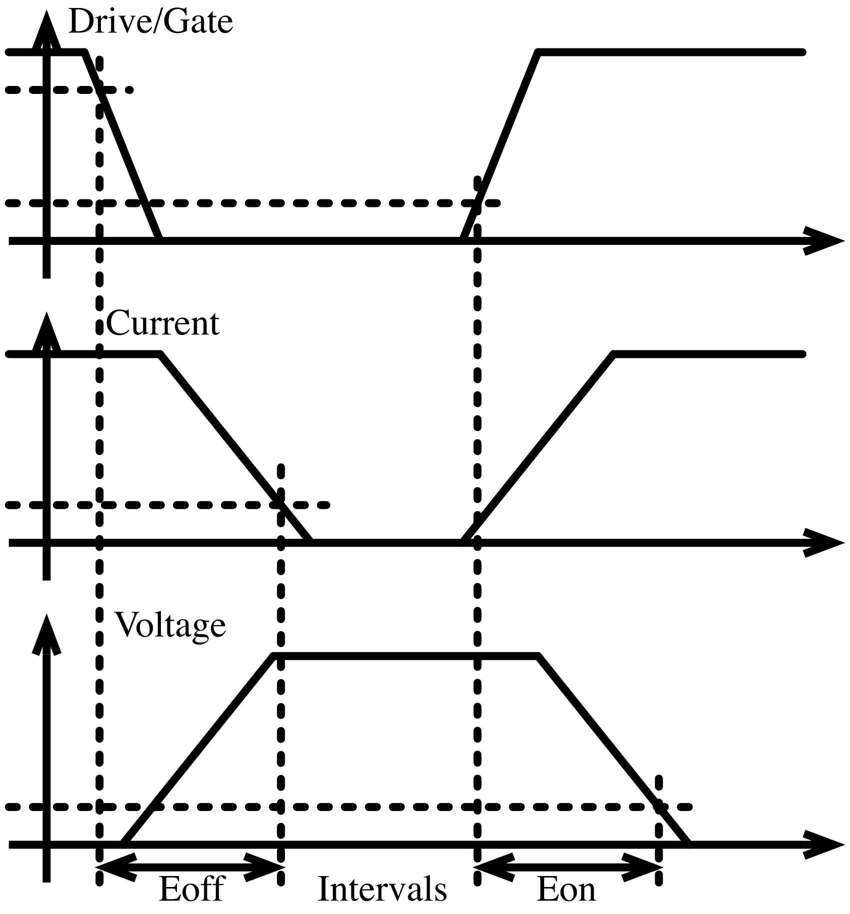
PWL(0 {vOff} {t1} {vOff} {t2} {vOn} {t3} {vOn} {t4} {vOff} {t5} {vOff} {t6} {vOn} {t7} {vOn} {t8} {vOff})

- ## Waveforms



Double Pulse Measurement Setup

- **Conventions**



- **Script**
- You can also use the waveform viewer math functions :
  - Multiply Voltage and Current = Losses
  - Integrate Losses
  - Measure using cursors the difference in between the two triggering points

- In our case, a script doing the previous steps has been created to measure Eon, Eoff, and many other parameters… at once.

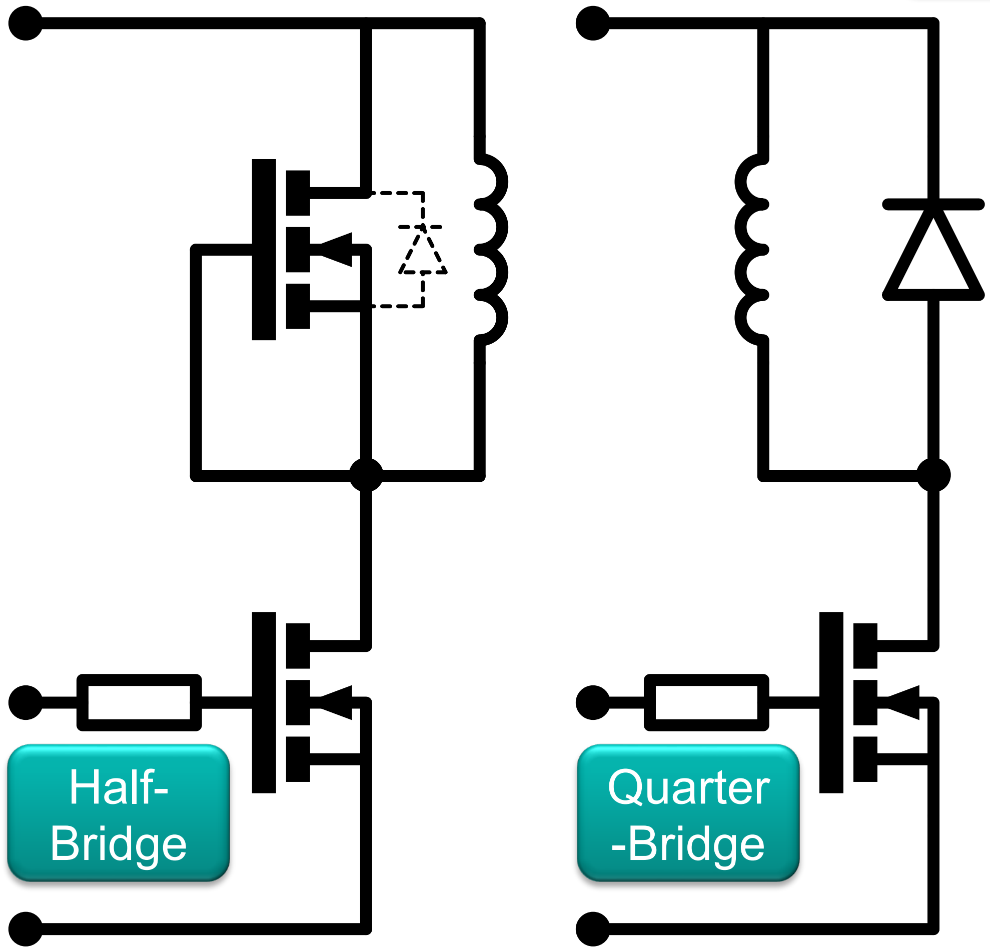
V_{GS} values' Influence

Setup : NDSH50120C (50 A, 1200 V, D3) freewheeling diode
NTH4L022N120M3S (22 mΩ, 1200 V, M3S) Switching MOSFET
Test point : 800 V / 40 A / 5Ω External Gate Resistor

V_{GS} Low/Off	V_{GS} High/On	Turn-on	Turn-off
0 V	12V	686.73 µJ	168.08 µJ
-3 V	12 V	685.52 µJ	109.03 µJ
0 V	15 V	467.44 µJ	168.75 µJ
-3 V	15V	461.23 µJ	108.92 µJ
0 V	18 V	376.66 µJ	168.56 µJ
-3 V	18 V	369.35 µJ	109.18 µJ

Structure Influence

Setup : NDSH50120C (50 A, 1200 V, D3) Quarter-brick only
NTH4L022N120M3S (22 mΩ, 1200 V, M3S) MOSFET
Test point : 800 V / 40 A / 5Ω External Gate Resistor



Structure	Quarter-Bridge	Half-Bridge
Turn-on	369 μJ	421 μJ
Turn-off	109 μJ	117 μJ

As SiC Schottky diode has less reverse current than SiC P-N Junction Body diode,
Quarter-Bridge shows better results because there is less losses due to less reverse current flow.

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Package Influence

Setup : NDSH50120C (50 A, 1200 V, D3) freewheeling diode
NTH4L022N120M3S (22 mΩ, 1200 V, M3S) Switching MOSFET
Test point : 800 V / 40 A / 5Ω External Gate Resistor

Package	TO247-3L	TO247-4L	D2Pak-7L
Turn-on	1115 μJ	421 μJ	483 μJ
Turn-off	257 μJ	117 μJ	111 μJ
Total	1372 μJ	**538 μJ**	**594 μJ**

Kelvin Packages show more than Half switching losses.

Topologies Simulations with Physical & Scalable Models

Flying Capacitor Boost, I-NPC vs T-NPC, 6-Pack Boost Active front End

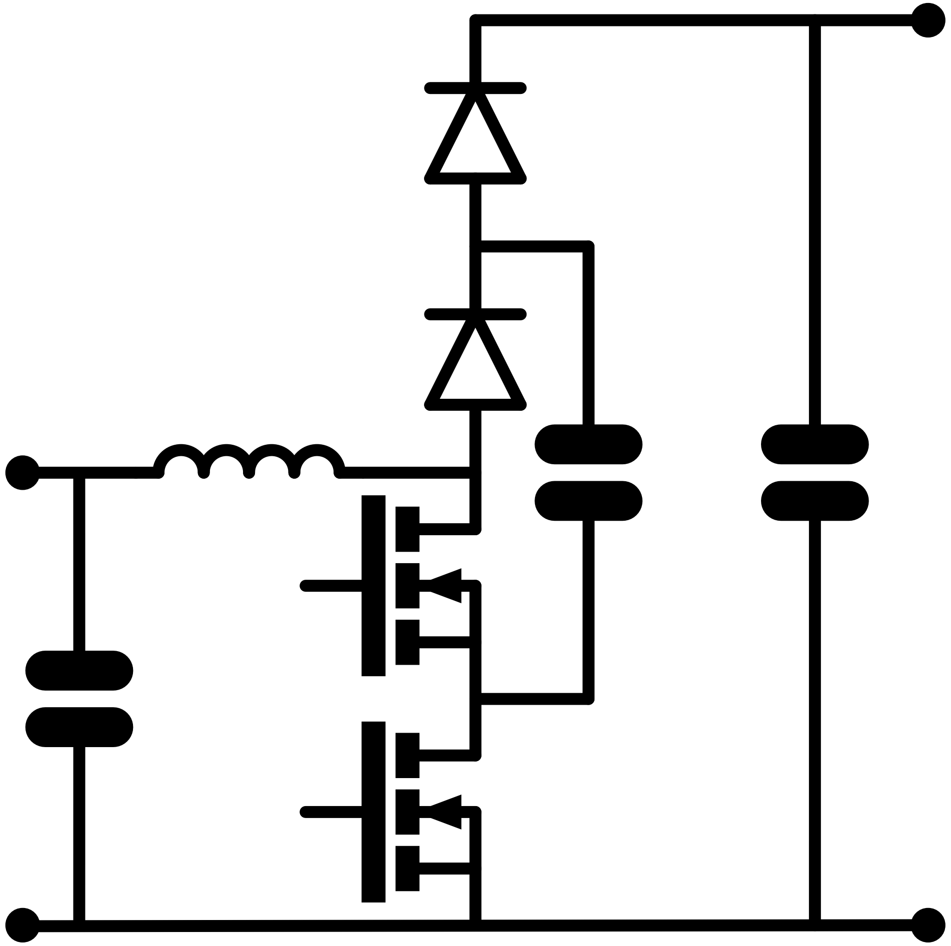
Flying Capacitor Boost

DC-DC deep analysis

Flying Capacitor Boost

- Single Input — Single output
- Stacked Switches and Diodes
- Operates like an interleaved topology

- Example :
- 700 V in, 1100 V out
- 30 kW
- 30 kHz switching frequency
- Using M3S 1200V MOSFETs
- Using D1 30A 1200V Diodes



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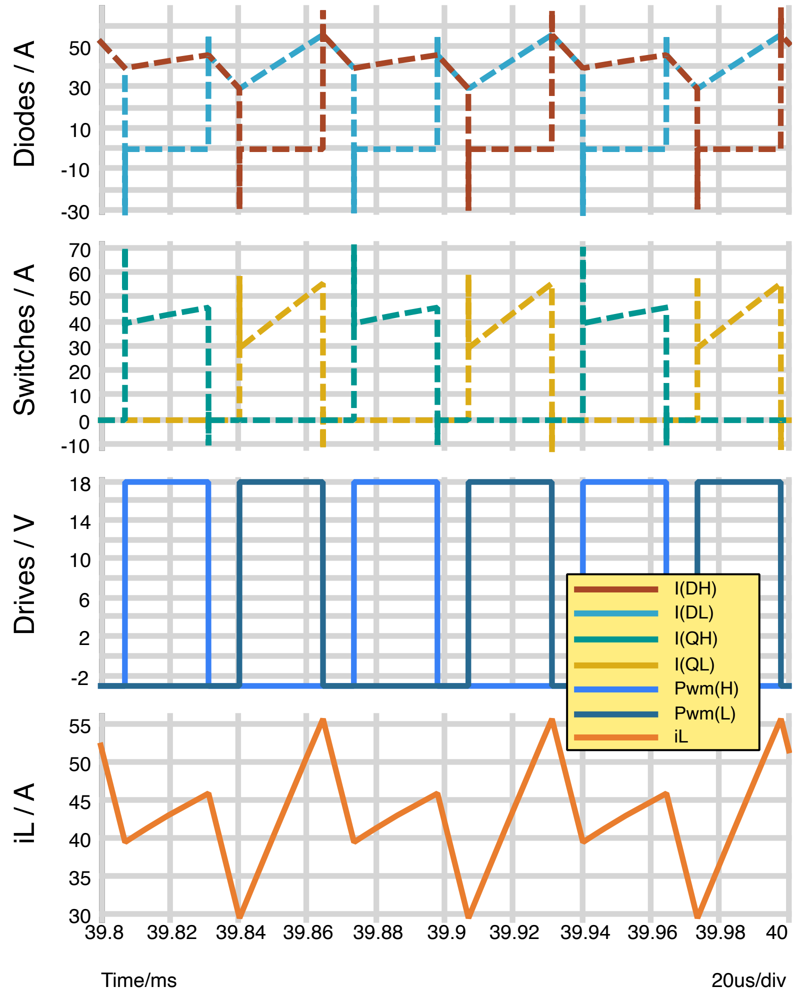
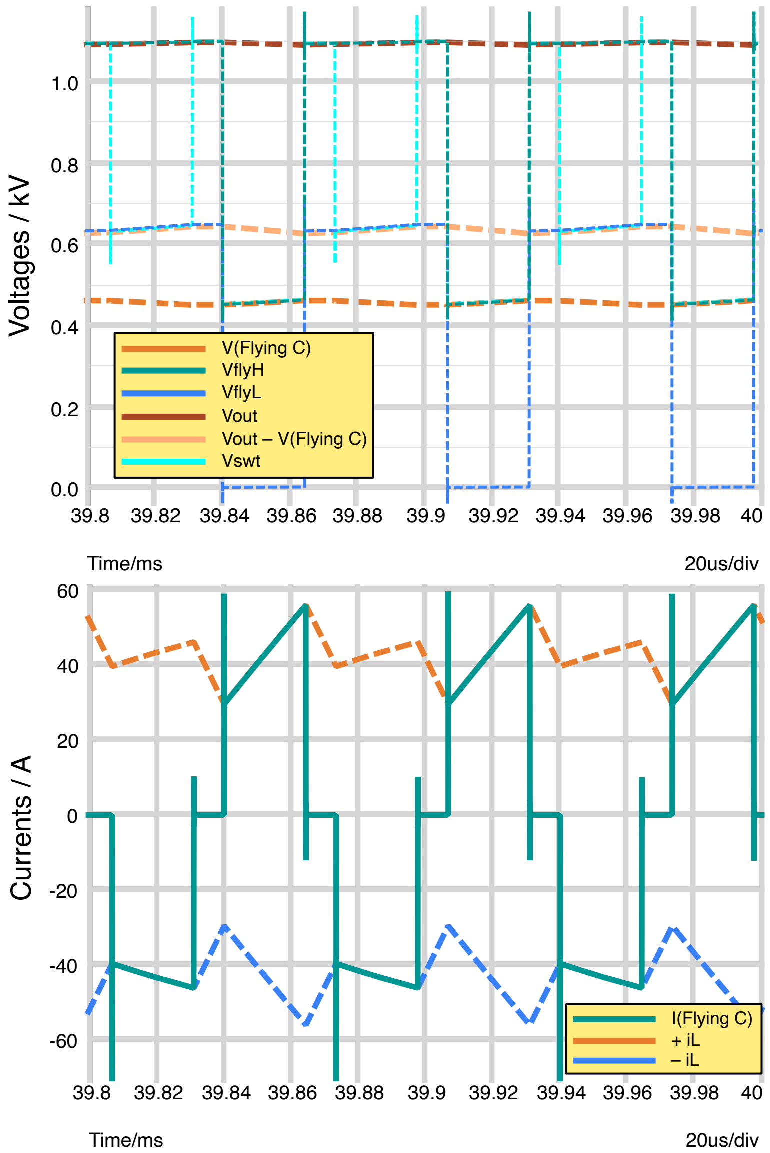
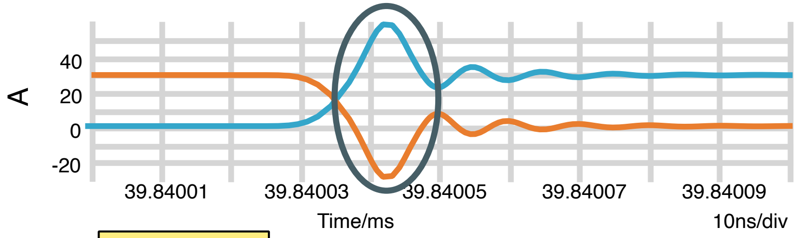
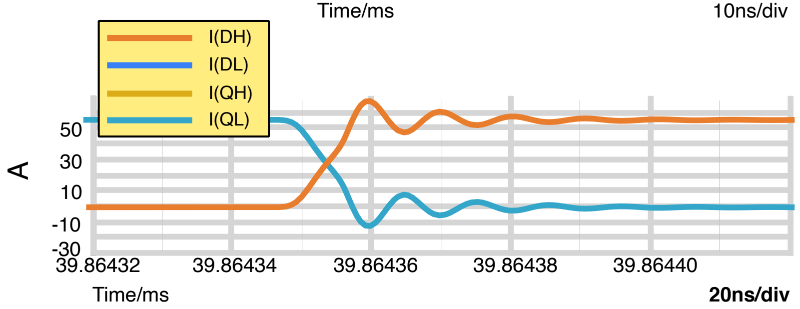
Flying Capacitor Boost waveforms

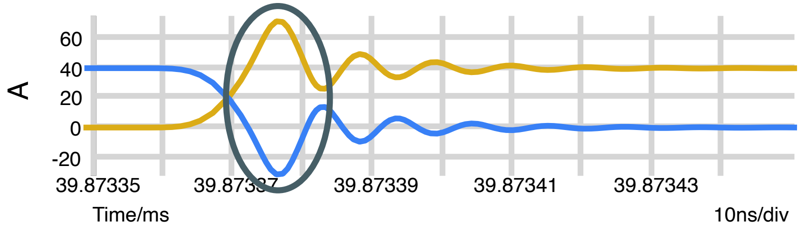


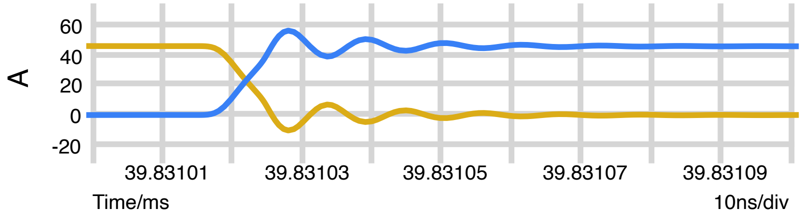


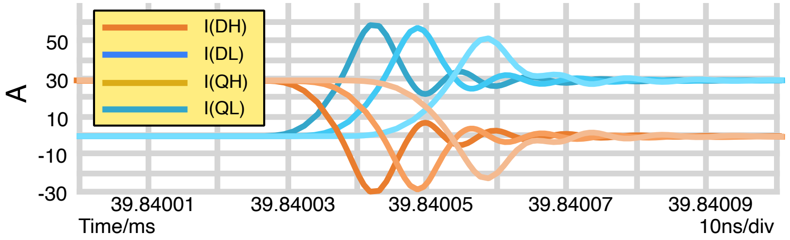
Flying Capacitor Boost Turn-ON and Turn-OFF zoom

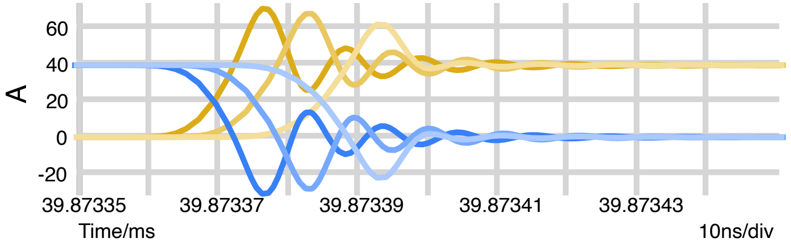










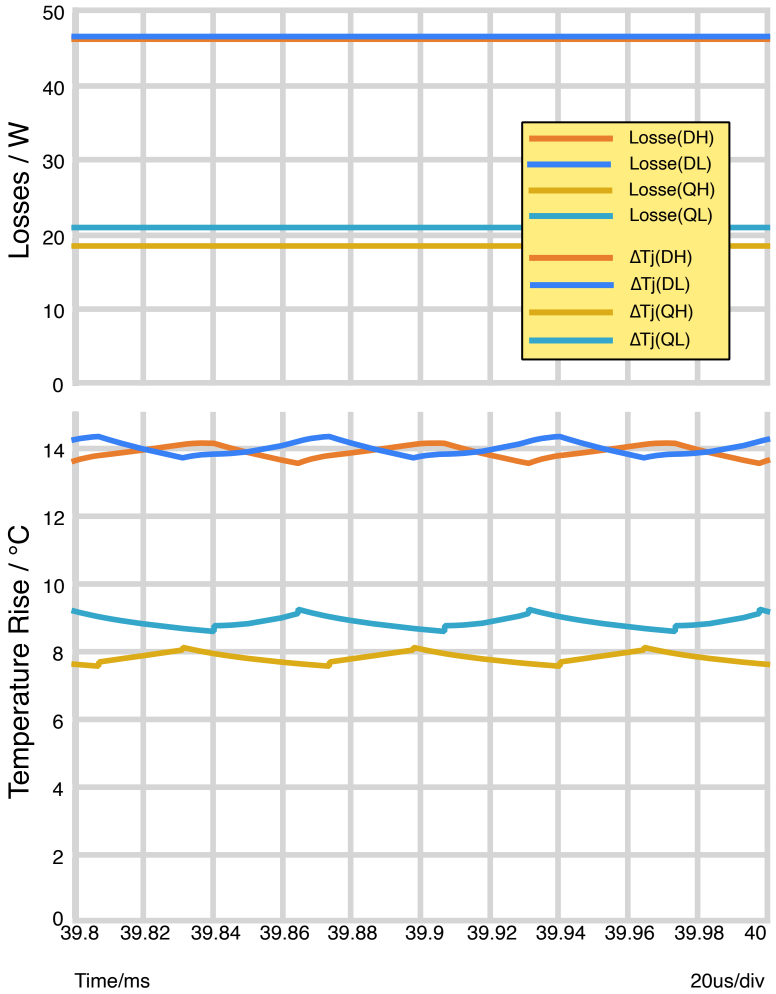


External Gate Resistor	Negative peak I(DH)	Negative peak I(DL)
Rg = 2.5 Ω	-29.3 A	-30.6 A
Rg = 5 Ω	-27.8 A	-28.4 A
Rg = 10 Ω	-22.3 A	-22.3 A

Flying Capacitor Boost performances

Losses using Current flowing out of Tcase

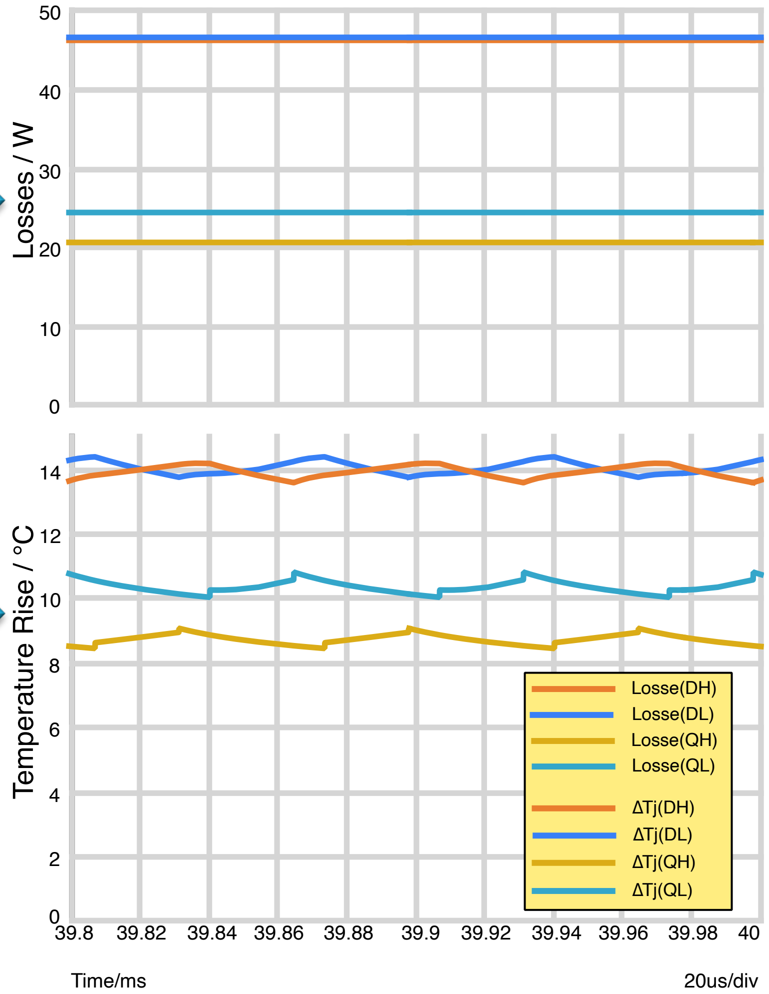
- $R_G = 2\ \Omega$



Only MOSFETs losses increase by 2 or 3 W

Only MOSFETs $\Delta T_{J\text{-}C}$ increase around 1°C

- $RG = 10\ \Omega$



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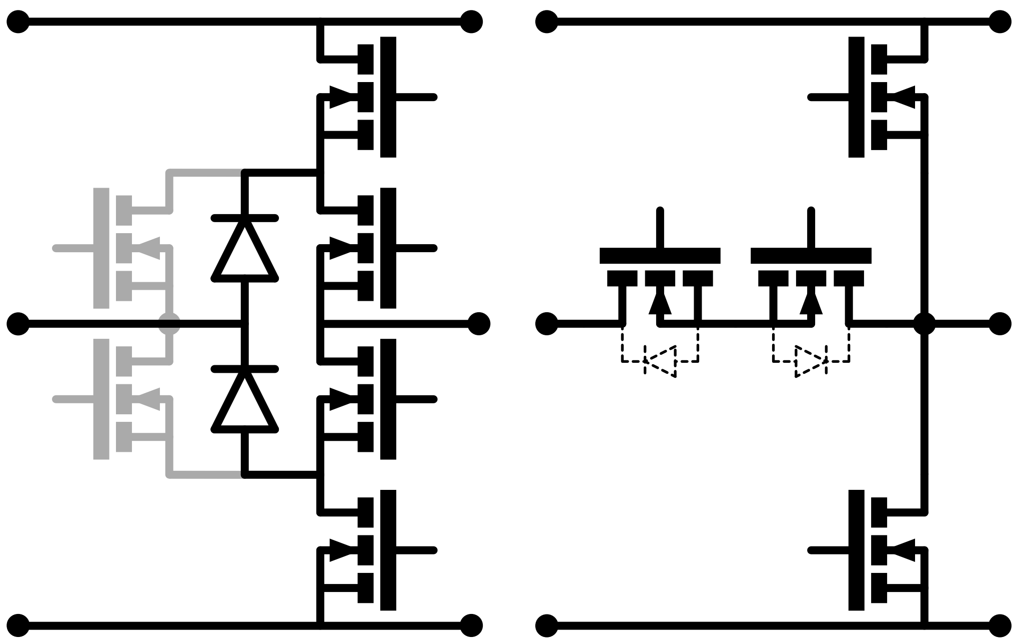
I-NPC vs T-NPC

Which is the best cell ?

I-NPC vs T-NPC : Quick comparison



- Comparison setup : Buck stage
  - 400 V in, 200 V / 20 A out
  - Switching frequency around 100 kHz (Self oscillating PWM)
  - D1 or D2 diodes = 50A / 650V
  - M2 MOSFET = 15 mΩ / 650V
  - M3S MOSFET = 22 mΩ / 1200V

Topology	I-NPC	I-NPC	I-NPC	A-NPC	A-NPC	T-NPC	SR T-NPC	SR T-NPC
QsH	M2 32.6 W	M2 18.7 W	M3S 7.8 W	M2 36.3 W	M3S 7.7 W	M3S 8.6 W	M3S 6.5 W	M3S 8.6 W
QdH/DH	D1 11.5 W	D2 10.9 W	D2 10.9 W	M2 18.1 W	M3S 18.8 W	M3S 50.4 W	M2 61.4 W	M3S 26.2 W
QmH	M2 4.4 W	M2 4.3 W	M2 4.3 W	M2 4.4 W	M3S 6.2 W	M3S 3.0 W	M2 2.2 W	M3S 3.1 W
Total	48.5 W	33.9 W	23.0 W	58.8 W	32.7 W	62 W	70.1 W	37.9 W

6-Pack Boost Active Front End

Or 3-Phase Grid Power Factor Corrector

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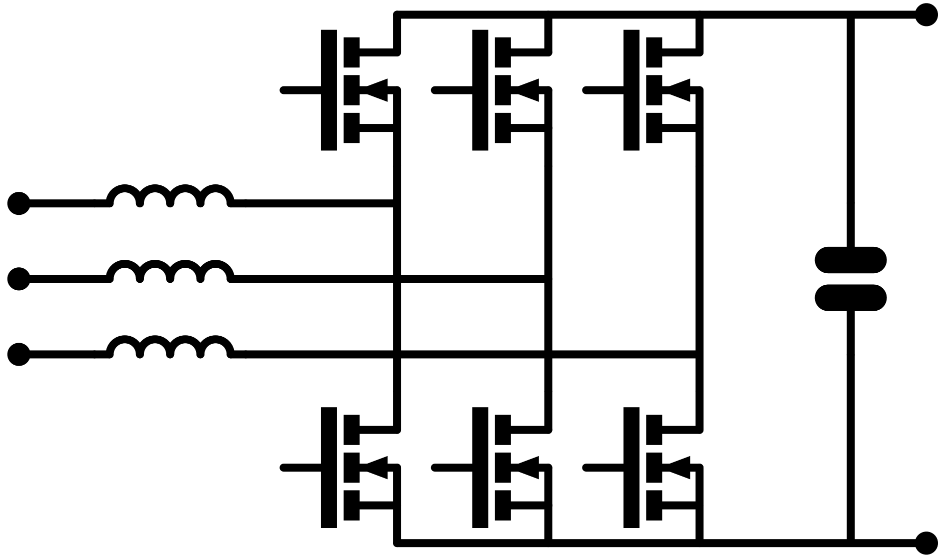
6-Pack Boost Active Front End

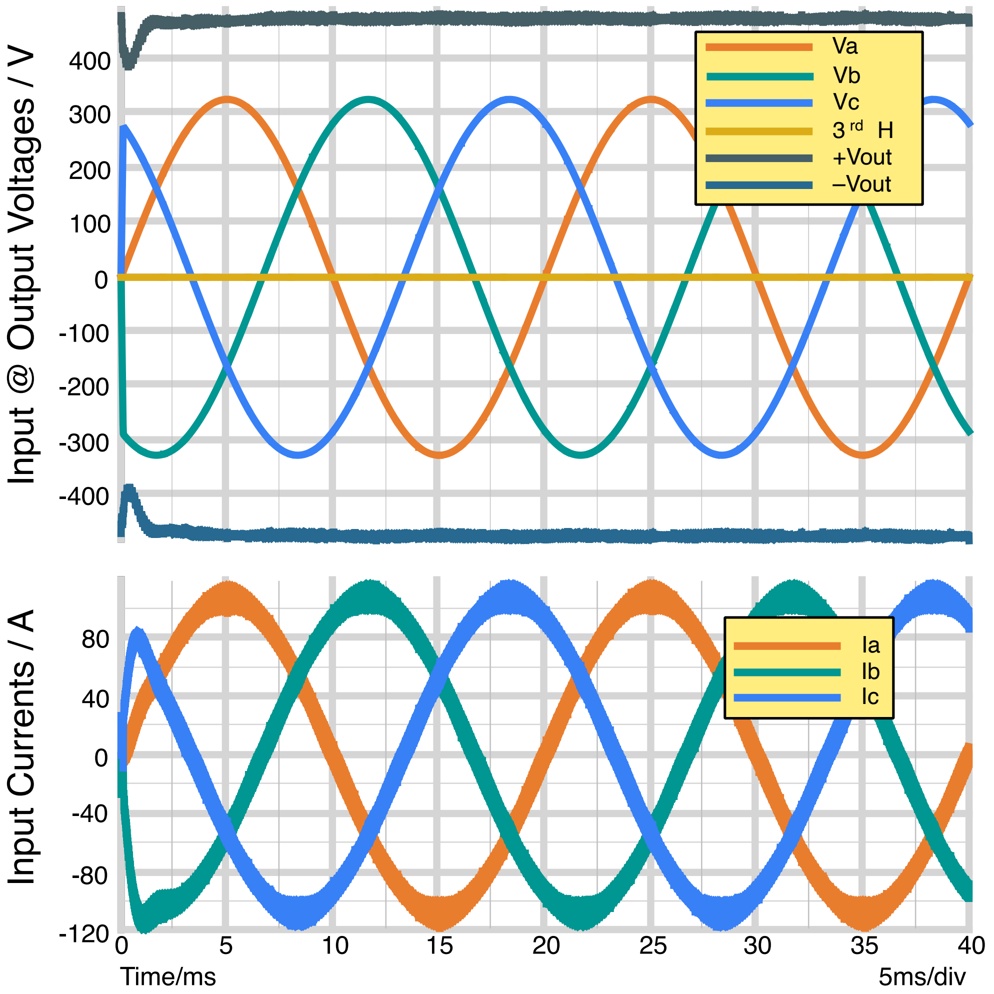
- 230 Vrms 3-Phase 50 Hz Grid input
- 950 V 50 kW output
- 72 kHz Switching frequency
- 80 µH inductor, 10 mΩ ESR, 70 pF //
- 60 µF capacitor, 2.5mΩ ESR

- D-Q control with Sine PWM
- FeedForward Duty cycle prediction
- 3rd Harmony Injection

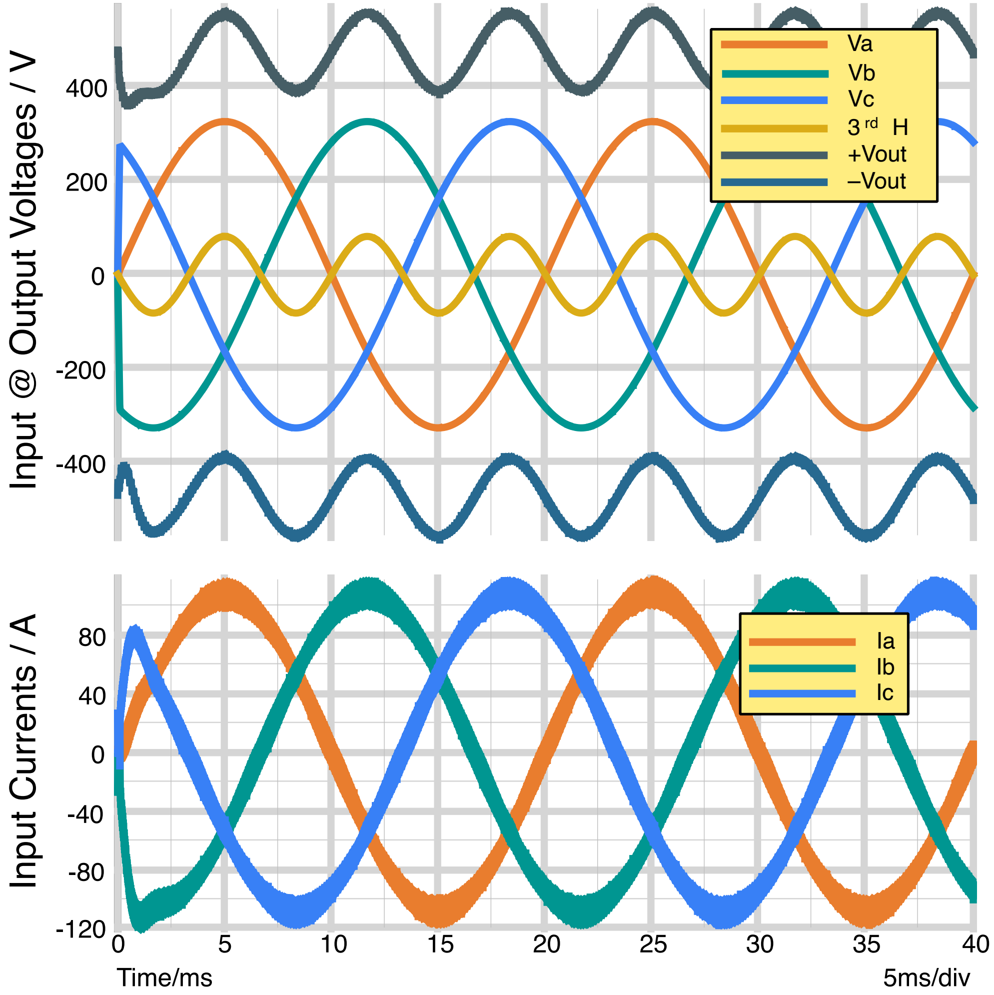


6-Pack Boost Active Front End : Waveforms

- **Without 3rd Harmonic Injection**



- **With 3rd Harmonic Injection**



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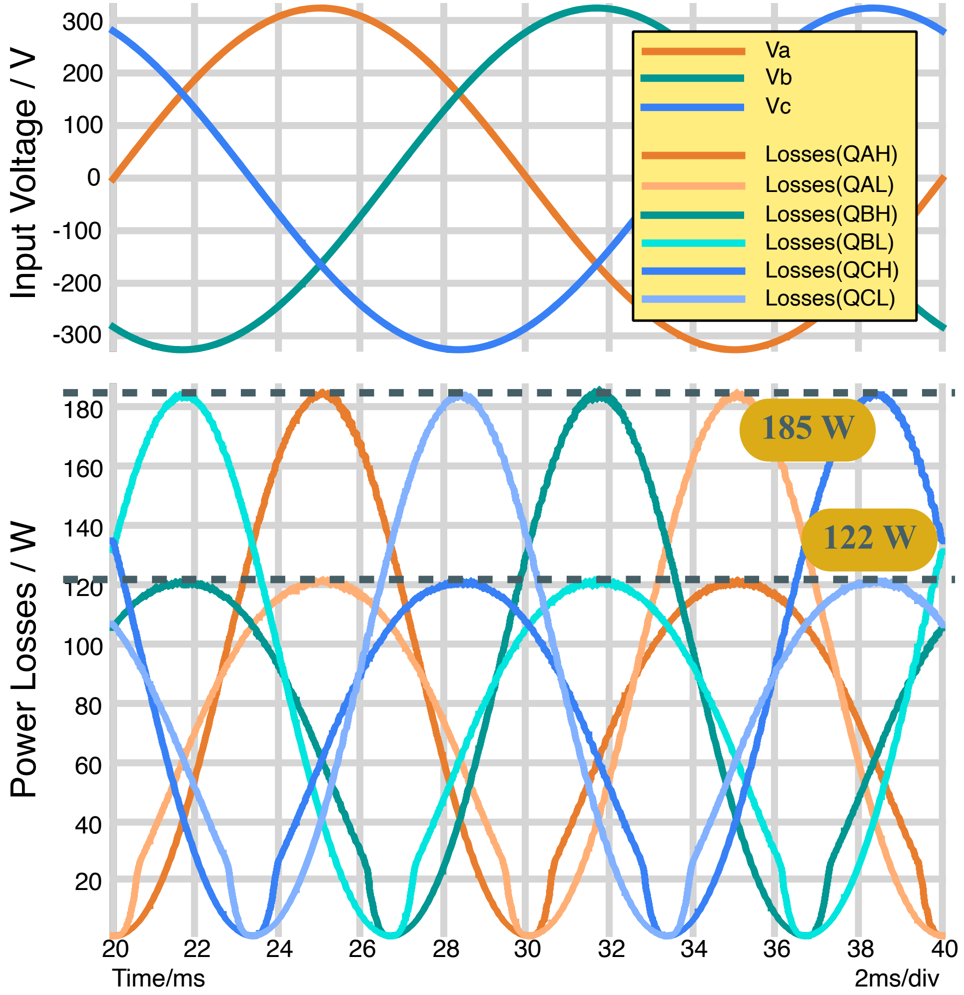
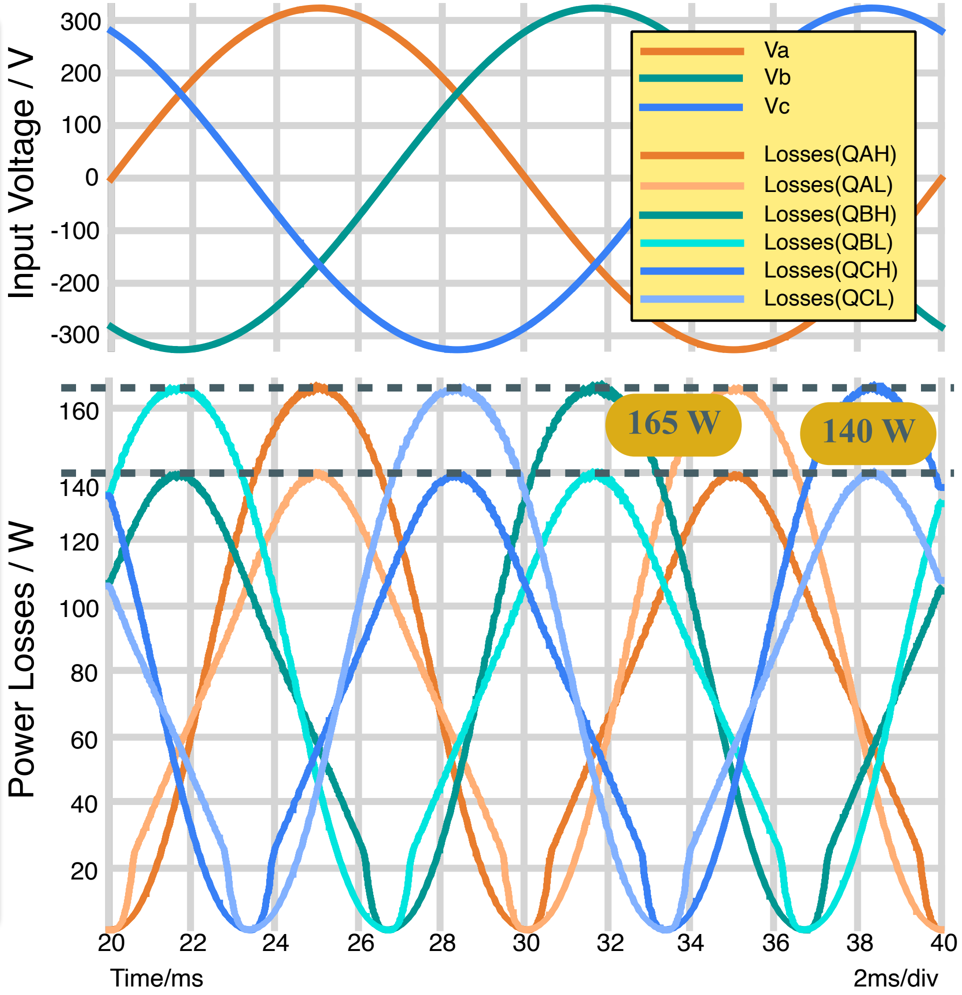
6-Pack Boost Active Front End : Losses Cycle by Cycle

- **Without 3rd Harmonic Injection**



Less differences between two half cycles

- **With 3rd Harmonic Injection**



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6-Pack Boost Active Front End : Average Losses over Grid Cycle

- **Without 3rd Harmonic Injection**

QAH Power Losses : 83.5584W

QAL Power Losses : 83.5516W

QBH Power Losses : 83.55W

QBL Power Losses : 83.5384W

QCH Power Losses : 83.5505W

QCL Power Losses : 83.5402W

- Total

Power Losses : 501.289W

- **With 3rd Harmonic Injection**

QAH Power Losses : 83.6955W

QAL Power Losses : 83.6902W

QBH Power Losses : 83.6783W

QBL Power Losses : 83.6803W

QCH Power Losses : 83.6782W

QCL Power Losses : 83.6865W

- Total

Power Losses : 502.109W

Same Losses

Conclusion

Conclusion

- **onsemi** simulation models offer unique features like :
  - Access to internal nodes
  - Accurate results for device have large non-linearities over several decades
- We have seen how to set Electro-Thermal simulations and get more out of them :
  - Junction temperature rise,
  - Heat propagation and Average Losses using power flow.
- Topologies simulations and analysis can bring very useful information like :
  - Junction temperature rise,
  - Losses analysis (switching energy, reverse current effect, $R_{DS(on)}$ variations, …)
  - Impact of parasitic components on **Silicon Carbide** devices performances
- Physical & Scalable models make virtual prototyping much more real.

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