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A High Voltage Input Supply 12 W Adaptor with NCP1362 Primary Side Regulated Quasi Resonant Controller

AND9890/D

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APPLICATION NOTE

The NCP1362 controlling a 1 kV Power MOS offers a new solution targeting output power levels up to 12 W continuously in a universal−mains flyback application up to 500 V rms for Industrial applications.

Thanks to a Novel Method, this new controller saves the secondary feedback circuitry for Constant Voltage and Constant Current regulation, achieving excellent line and load regulation without traditional opto coupler and TL431 voltage reference.

The NCP1362 operates in valley lockout quasi−resonant peak current mode control mode at high load to provide high efficiency. When the power on the secondary side starts to diminish, the controller automatically adjusts the duty−cycle then at lower load the controller enters in pulse frequency modulation at fixed peak current with a valley switching detection. This technique allows keeping the output regulation with tiny dummy load. Valley lockout at the first 4 valleys prevents valley jumping operation and then a valley switching at lower load provides high efficiency.

This application note focuses on the experimental results of a 12−W power supply driven by the NCP1362.

Table 1. EVALUATION BOARD SPECIFICATION

Parameter	Value
Minimum input voltage	85 V rms*
Maximum input voltage	500 V rms
Bulk Over Voltage Protection	750 V DC**
Output voltage	12 V
Nominal output power	12 W
Full load Efficiency	>75%
1 W / <10% Load Efficiency	> 60%
“No Load” consumption < 400 V Bulk	<70 mW
“No Load” consumption > 400 V Bulk	<150 mW
Startup time	<1 s

*Down to 85 V rms and full power with mandatory larger Bulk cap to reduce the low Frequency voltage ripple

**If a DC voltage supply is used, the source has to be connected directly on the bulk capacitor C4 / C17. CM1 cannot handle this high dc voltage.

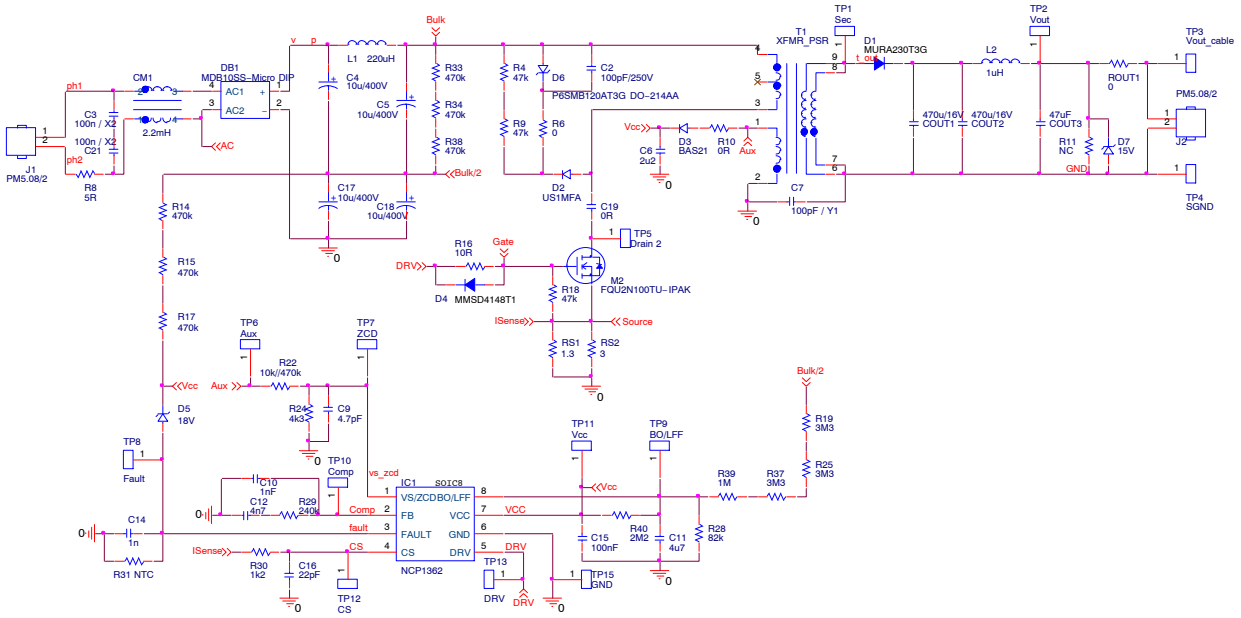

Figure 1. Evaluation Board Schematic

Figure 2. EVB Picture (Top View)

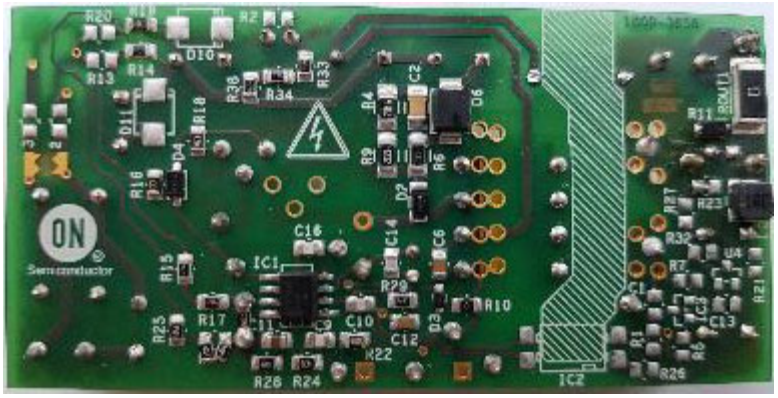

Figure 3. EVB Picture (Bottom View)

Impacts of Out of Range / High Input Voltage Supply

The extremely high input supply has multiple impacts on the Switch Mode Power Supply design.

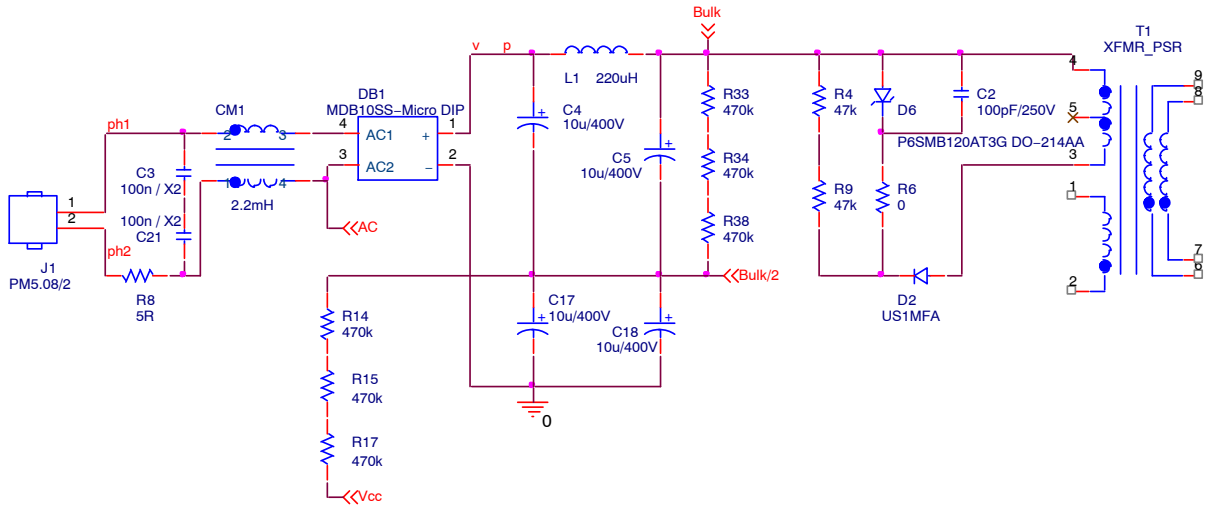

Figure 4. Mains Input & Bulk Schematic

- With twice the classical max input voltage, the design should use two X2 Capacitors for EMI resulting of 50 nF without necessary discharge resistors.
- As the max possible voltage of 450 V Bulk electrolytic capacitors is not enough, two of 400 V−type should be connected in series with parallel resistor to secure the voltage balancing despite the tolerances of capacitors. As the equivalent value is divided by 2, the lower possible mains supply in this case will be limited to 140 V rms. It is possible to extend down the input supply voltage using much larger bulk capacitors (>> 22 μF x 4 @ 10 μF x 4)

- To reduce overall power consumption particularly critical in Standby mode, the lower balancing resistor are used also for Startup, connected to V_{cc} of NCP1362 instead of GND. This has not major impact on the voltage balancing with only 12 V V_{cc}. The same applies for BO/LFF using also only half of the bulk voltage.
- The next impact is on Max voltage capability of the Power switch. If 800 V−type provides good design margin with 400 V Bulk supply, we get added 350 V when supplied with 750 V: this asks for special design with 1 kV MOS solution.
- The next impact is on the primary snubber now forced to support up to 1 kV asking for larger reversed voltage diode and transil diode instead of simple discharge R to reduce as much as possible the consumption particularly critical in Standby mode.
- The last impact is on secondary rectifier diode. As reversed voltage for this diode is directly proportional to Bulk supply, we will get almost twice the reverse voltage when moving up to 750 V DC.

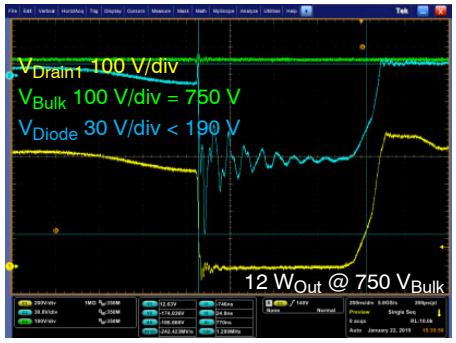

Figure 5. Secondary Diode Reversed Voltage @ Bulk Supply by Max Power

Start−up

The start−up sequence is performed with resistors connected to the middle point of bulk capacitors to reduce the power dissipation as those are used for both Voltage balancing and startup. To further reduce the standby power, the start−up current of the controller is extremely low, below 6.3 μA maximum. The start−up time is directly linked to the V_{cc} capacitor value. Also, this capacitor has to be large enough to maintain the V_{cc} voltage above $V_{cc(off)}$ level in no load condition. Indeed, in light load or no load condition, the controller operates at the minimum frequency clamp and the dead time between two cycles will be 1 ms. The V_{cc} voltage has to be kept above $V_{cc(off)}$. Finally, the last constraints regarding the V_{cc} capacitor is the start−up time. Generally, the power supply has to start in less than 3 s regardless the input voltage. Taking in account these parameters in the application board, we have selected a 2.2−μF value for C_6.

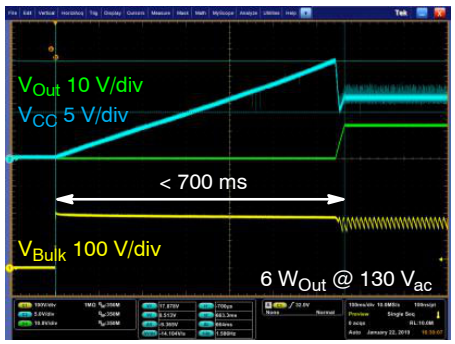

Figure 6. The Start−up Sequence is below 1 s at 130 V rms – Room Temperature

Brown−Out & Bulk OVP

To avoid unnecessary power consumption with our extremely high input supply, we connect the BO like, for Startup, to half Buck supply, using those resistors to balance serial Bulk capacitors.

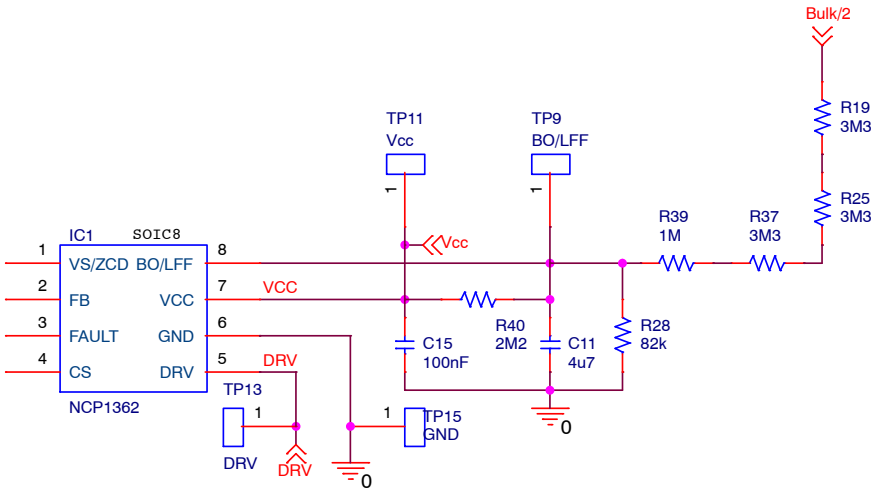

Figure 7. The Modified Brown−Out Allows Adjusting Both Bulk OVP and BO

The BO circuit has been modified to take into account the extremely wide range of input supply and to keep Bulk OVP NCP1362's feature

- The R divider from Bulk/2 to BO/LFF input adjust with R28 define the OVP sets to ~ 730 V DC in our application
- To compensate the too low voltage applied by low mains input, an added current is injected on BO/LFF through R40 connected to V_{cc}
- The higher $V_{cc-start}$ versus V_{cc} in ON Mode provides a larger Brown−in hysteresis helping for the starting phase

Valley Lockout

The valley lockout technique makes controller change valley (from the 1st to the 4th valley) as the load decreases and / or Input supply increases without any valley jumping. This allows extending the quasi−resonance (QR) operation range.

The following scope shoots show the operating valley versus load and input supply.

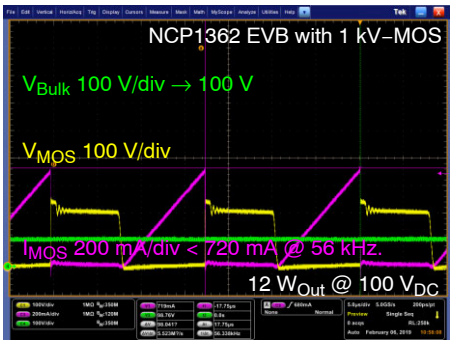

Figure 8. QR (1st Valley) Operation @ 1 A / ~ 90 V rms

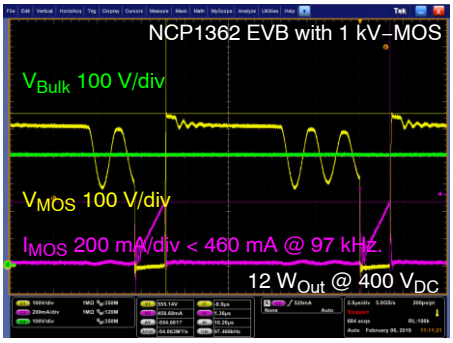

Figure 9. 2nd Valley Operation @ 1 A / 280 V rms

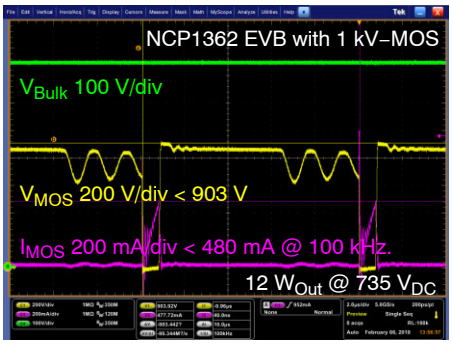

Figure 10. 3rd Valley Operation @ 1 A / 520 V rms

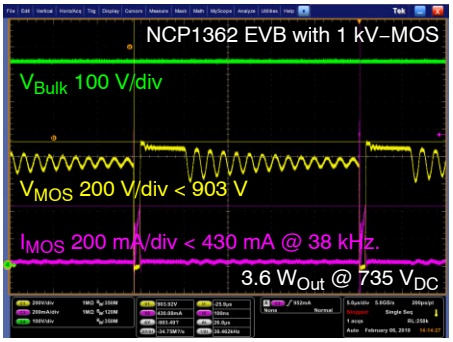

Figure 11. DCM / 19th Valley Operation @ 0.3 A / 520 V rms

Frequency Fold Back Mode

If while operating at valley 4, the load further decreases, the NCP1362 will operate in Frequency Foldback (FF) mode. Practically, the circuit enters in FF mode when comp voltage drops below 2.1 V. The current is frozen to $V_{CS(VCO)}$ and regulation is made by varying the switching frequency (f_{SW} reduces if the power demand diminishes). The system reduces the switching frequency by adding some dead−time after the 4th valley is detected. Moreover, in order to keep the high efficiency benefit inherent to the QR operation, the controller turns on again with the next valley after the dead time has ended. As a result, the controller will still run in valley switching mode even when the FF is enabled.

In this 12−W evaluation boards, at 130 V rms, the switching frequency is around 40 kHz @ 0.2 A at the beginning of the frequency fold back mode. The primary peak current is frozen to $V_{CS(VCO)}$.

Figure 12. FF Mode & $V_{CS(VCO)}$ @ 2.5 W / 130 V rms

200 Hz Minimum Frequency Clamp

Due to the primary side regulation, the only way to have an information of the output voltage is to generate a new cycle and read the voltage on the auxiliary winding. This voltage is an image of the output voltage affected by the transformer turns ratio. For this reason, the system has to impose a minimum switching frequency to refresh the sampling on the primary side and have a good transient response. The default minimum frequency clamp is set to 200 Hz.

So the frequency clamp impose to transfer energy from primary to secondary side each ms. Because there is no load on the output, the 12−V voltage cannot be maintained to the nominal level and will increase until the OVP protection is trigged. To avoid this fault, a Zener protection is generally connected on the output to dissipate this energy in no load condition to reduce the impacts on stand−by performance versus simple dummy load with resistor. For this reason, a second frozen peak current called $V_{CS(STB)}$ is implemented in this controller to reduce to the minimum the energy transfer each cycle and so limit the power dissipated in the dummy load.

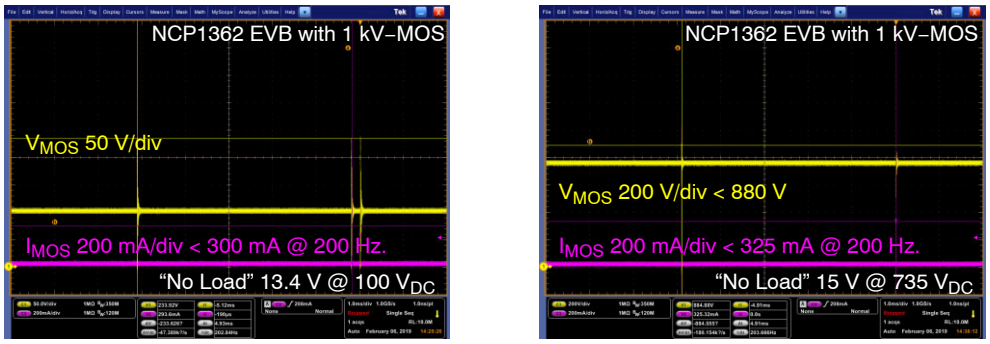

Figure 13. 200 Hz Minimum Frequency Clamp & $V_{CS(STB)}$ @ No Load / 90 V rms and 520 V rms

Transient load

Below Figure show an output transient load step 0% / 50% of the maximum output power versus line / input supply.

The step load response is 500 mV or 4.2% of the output voltage in the worth case.

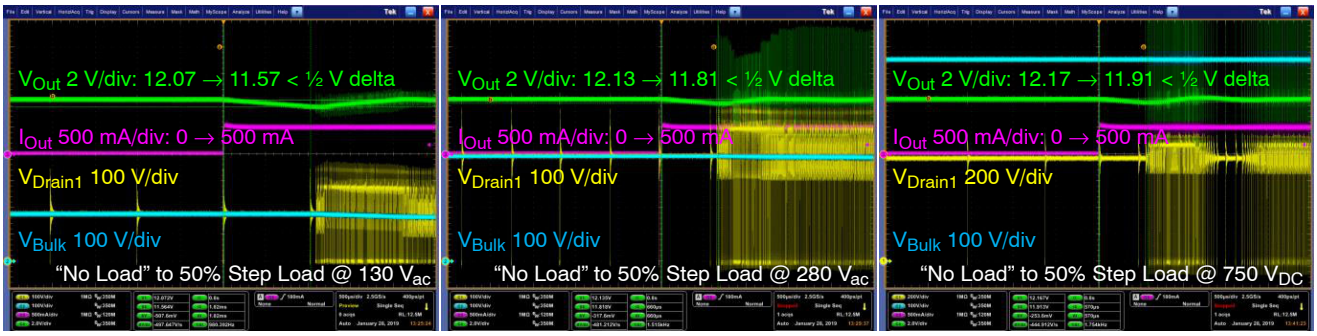

Figure 14. Step Load Response from 0% to 50% @ Input Supply

Figure 15. Step Load Response from 50% to 0% @ Input Supply

Next Figures show an output transient load step from 10% to 100% of the maximum output power at low line and high line. The slew rate is 1 A/μs and the frequency is 10 Hz.

The step load response is ±250 mV.

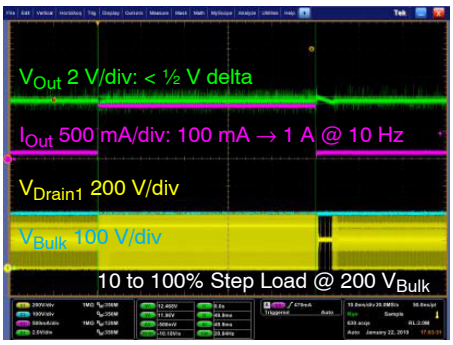

Figure 16. Step Load Response from 10% to 100% @ 130 V rms

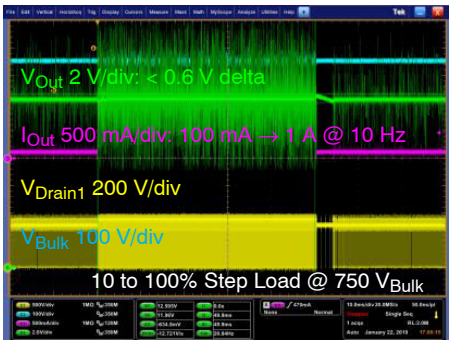

Figure 17. Step Load Response from 10% to 100% @ 520 V rms

Efficiency Results and Stand−by Performance

All measurements have been done after a 30 min warm−up phase at full load and an additional 5 min at the load under consideration.

The input power was measured with the power meter YOKOGAWA WT210.

The output voltage and output current were measured using digital multi−meters.

Table 2. EFFICIENCY @ INPUT SUPPLY (DC BULK)

Bulk	No Load	1 W	3 W	12 W	CC < 12 V
600 V	140 mW @ 14 V	65.2% @ 12.03 V	70.34% @ 12.05 V	76.5% @ 12.2 V	1.13 A @ 11.88 V
400 V	60 mW @ 12.2 V	71% @ 12.01 V	73.8% @ 12.02 V	75% @ 12.18 V	1.11 A @ 11.88 V
200 V	18 mW @ 13 V	75.2% @ 12 V	76.3% @ 12 V	79% @ 12.12 V	1.06 A @ 11.88 V
120 V	7 mW @ 12.18 V	75% @ 12 V	76% @ 12 V	75% @ 12.11 V	1.04 A @ 11.88 V

*The average efficiency was calculated from the efficiency measurements at ~ 8%, 25% and 100% of the nominal output power.

The stand−by consumption is a key parameter for this kind of application. Thanks to the double frozen peak current, both light load and no load condition are optimized. Thanks to this point, the standby consumption is below 70 mW regardless the standard input voltage (< 265 V rms) and below 150 mW regardless the extended large input voltage (< 520 V rms) like shown in the Table 2.

- The impacts of high mains input supply is only related to balancing R used on serial Bulk capacitors: the power consumption of 50 mW @ 280 V rms is moving up to 180 mW @ 520 V rms!
- The minimum Frequency clamp of 200 Hz is avoiding output voltage to move up to 15 V, reducing power consumption but limiting speed restart for strong step load. This could be improved with min 1 kHz switching Frequency feature but with direct drawbacks on standby performances. This is a trade−off to be considered versus end customers' applications & requests

Please note that both BO and startup functions are using low side balancing R and thus do not have impact on the overall power consumption.

The overall balancing R power consumption could be decreased with larger R if bulk capacitors values tolerance could be improved.

Constant Voltage and Constant Current Regulation

Thanks to the NCP1362, both voltage and current are regulated to insure safe operation. When the load is below the nominal level (i.e. 1.1 A for this application), the output voltage is regulated to 12 V. Then, if the load increased, the current loop takes the control to limit the output current regardless the output voltage information. Finally, the BO/LFF pin improves the constant current regulation by sensing the input voltage and compensates the propagation delay effect at high line. These functions put together allow us to extract the CC/CV curve depicted in below Figure.

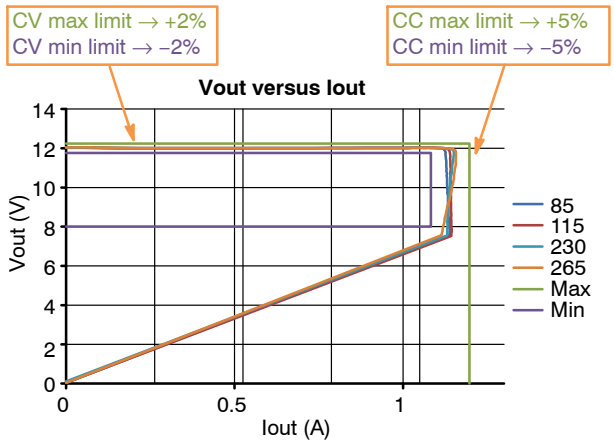

Figure 18. Constant Current (CC) / Constant Voltage (CV) Curve

Impacts on the Overall Design to Reduce Min Mains Input Supply

As already explained in introduction, the Bulk capacitors should be largely increased to avoid too strong ripple on Bulk supply and corresponding “instantaneous” supply for the converter.

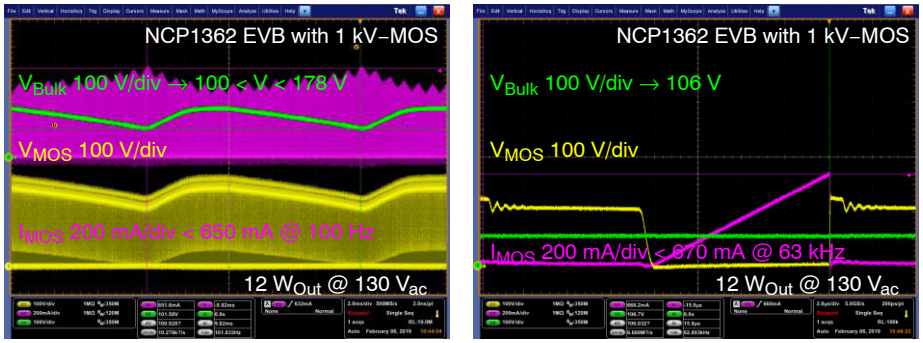

Figure 19. Original Design @ 130 V rms

With original 4 x 10 μF, we do have already 70 V ripple @ 130 V rms corresponding to 100 V min supply by Max 12 W Output.

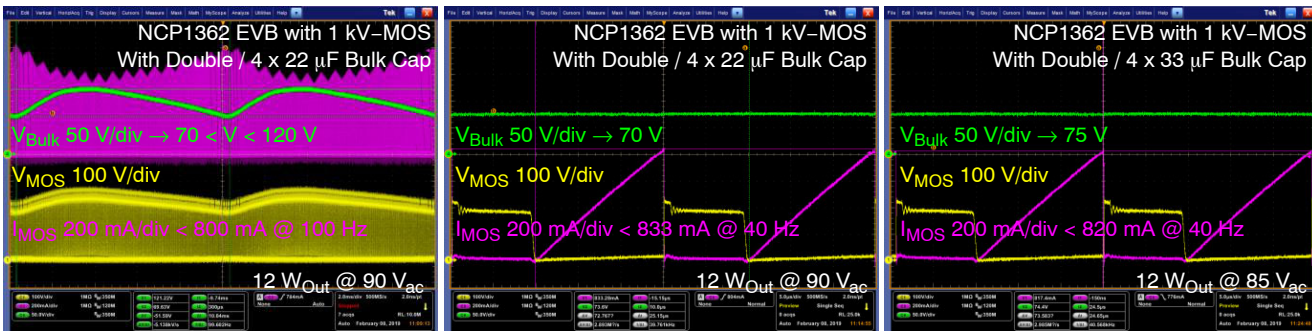

Figure 20. Modified Design with Double 4 x 22 μF Bulk Cap @ 90 V rms

With modified 4 x 22 μF, we do have only 50 V ripple @ 90 V rms corresponding to 70 V min supply by Max 12 W Output. This is extremely low and asks for much larger current (~ 830 mA) & reduced switching Frequency (<40 kHz) to keep regulation of the output voltage. To secure the correct behaviors by such low input supply, we may better move to larger cap with 4 x 33 μF despite larger size & cost.

Table 3. BILL OF MATERIAL (BOM)

Designator	Quantity	Description	Value	Tolerance	Manufacturer Part Number
C2	1	Ceramic capacitor, 1206, 1 kV	100 pF	10%, 1 kV	Standard
C3, C21	2	X2 capacitor, 305 V	100 nF	305 V	B32921C3104
C4, C5C,17, C18	4	Electrolytic capacitor, 400 V	10 μF	400 V	UVC2G100MPD
C6	1	Ceramic capacitor, 0805, 35 V	2.2 μF	10%, 35 V	Standard
C7	1	Y1 capacitor, 440 V	100 pF	440 V	CD70−B2GA101KYNKA
C9	1	Ceramic capacitor, 0805, 50 V	4.7 pF	10%, 50 V	Standard
C10	1	Ceramic capacitor, 0805, 50 V	1 nF	10%, 50 V	Standard
C11	1	Ceramic capacitor, 0805, 35 V	4.7 μF	10%, 10 V	Standard
C12	1	Ceramic capacitor, 0805, 50 V	4.7 nF	10%, 50 V	Standard
C14	1	Ceramic capacitor, 0805, 50 V	1 nF	10%, 50 V	Standard
C15	1	Ceramic capacitor, 0805, 50 V	100 nF	10%, 50 V	Standard
C16	1	Ceramic capacitor, 0805, 50 V	22 pF	10%, 50 V	Standard
C19	1	Ceramic Resistor, 1206	0 Ω	5%	Standard
CM1	1	Common mode choke	2.2 mH	0.5 A	Murata 50225C
COUT1, COUT2	2	Polymer capacitor, 16 V	470 μF	20%, 16 V	PLF1C471MDO1
COUT3	1	Electrolytic capacitor, 16 V	47 μF	20%, 16 V	ECA1CAK470X
D1	1	Ultra−Fast Diode, SMB, 2 A, 300 V	MURA230	2 A, 300 V, SMB	MURA230T3G
D2	1	Fast Recovery Diode, SMD, 1 A, 1000 V	US1MFA	1 A, 1000 V, SOD123FA	US1MFA
D3	1	Diode, SMD, 200 mA, 250 V	BAS21	200 mA, 250 V, SOD323	BAS21AHT1G
D4	1	Diode, SMD, 100 V	D1N4148	100 V	MMSD4148
D5	1	18 V Zener Diode	zener	18 V, SOD123	Standard
D6	1	Transient Voltage Suppression Diode	P6SMB120A		Littelfuse P6SMB120A
D7	1	15 V Zener Diode	zener	15 V, SOD123	Standard
DB1	1	Diode bridge, SMD, 1 A, 1000 V	MDB10S		MDB10S
IC1	1	PSR controller	NCP1362	SOIC8	NCP1362
J1, J2	2	Output Connector	PM5.08/2/90	10A, 300V	PM5.08/2/90
L1	1	Radial Coil, 220 μH, 0.5 A, 10%	220 μF	10%, 0.5 A	7447462221
L2	1	Radial Coil, 1 μH, 3 A, 30%	1 μH	30%, 3 A	SRN4026−1R0Y
M2	1	MOSFET,1000 V, 2 A	FQU2N100TU	TO251−IPAK	FQU2N100TU
R4	1	Ceramic Resistor, 1206, 0.25 W, 200 V	47 kΩ	5%	Standard
R6	1	Ceramic Resistor, 1206, 0.25 W	0 Ω	5%	Standard
R8	1	Through hole resistor, 1 W, 1%	5 Ω	1%	CMF605R0000FKBF
R9	1	Ceramic Resistor, 1206, 0.25 W, 200 V	47 kΩ	5%	Standard
R10	1	Ceramic Resistor, 0805, 0.25 W	0 Ω	5%	Standard
R14	1	Ceramic Resistor, 0805, 0.25 W	470 kΩ	5%	Standard
R15	1	Ceramic Resistor, 0805, 0.25 W	470 kΩ	5%	Standard
R16	1	Ceramic Resistor, 0805, 0.25 W	10 Ω	5%	Standard
R17	1	Ceramic Resistor, 0805, 0.25 W	470 kΩ	5%	Standard
R18	1	Ceramic Resistor, 0805, 0.25 W	47 kΩ	5%	Standard

Table 3. BILL OF MATERIAL (BOM) (continued)

Designator	Quantity	Description	Value	Tolerance	Manufacturer Part Number
R19	1	Ceramic Resistor, 0805, 0.25 W	3.3 MΩ	5%	Standard
R22	1	Ceramic Resistor, 0805, 0.25 W	10kΩ // 470 kΩ	5%	Standard
R24	1	Ceramic Resistor, 0805, 0.25 W	4.3 kΩ	5%	Standard
R25	1	Ceramic Resistor, 0805, 0.25 W	3.3 MΩ	5%	Standard
R28	1	Ceramic Resistor, 0805, 0.25 W	82 kΩ	5%	Standard
R29	1	Ceramic Resistor, 0805, 0.25 W	240 kΩ	5%	Standard
R30	1	Ceramic Resistor, 0805, 0.25 W	1.2 kΩ	5%	Standard
R31	1	NTC, 100 kΩ at 25°C, Beta = 4190	100 kΩ @ 25°C	0,05	NTCLE100E3104JB0
R32	1	Ceramic Resistor, 0805, 0.25 W	22 kΩ	5%	Standard
R33	1	Ceramic Resistor, 0805, 0.25 W	470 kΩ	5%	Standard
R34	1	Ceramic Resistor, 0805, 0.25 W	470 kΩ	5%	Standard
R37	1	Ceramic Resistor, 0805, 0.25 W	3.3 MΩ	5%	Standard
R38	1	Ceramic Resistor, 0805, 0.25 W	470 kΩ	5%	Standard
R39	1	Ceramic Resistor, 0805, 0.25 W	1 MΩ	5%	Standard
R40	1	Ceramic Resistor, 0805, 0.25 W	2.2 MΩ	5%	Standard
ROUT1	1	Ceramic Resistor, 2512, 1 W	0R	5%	Standard
RS1	1	Ceramic Resistor, 0805, 0.25 W	1.3 Ω	1%	Standard
RS2	1	Ceramic Resistor, 0805, 0.25 W	3.0 Ω	1%	Standard
T1	1	Transformer 12 V 12 W			Wurth 7508111333
TP1,TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP15	13	Test point			13.14.119

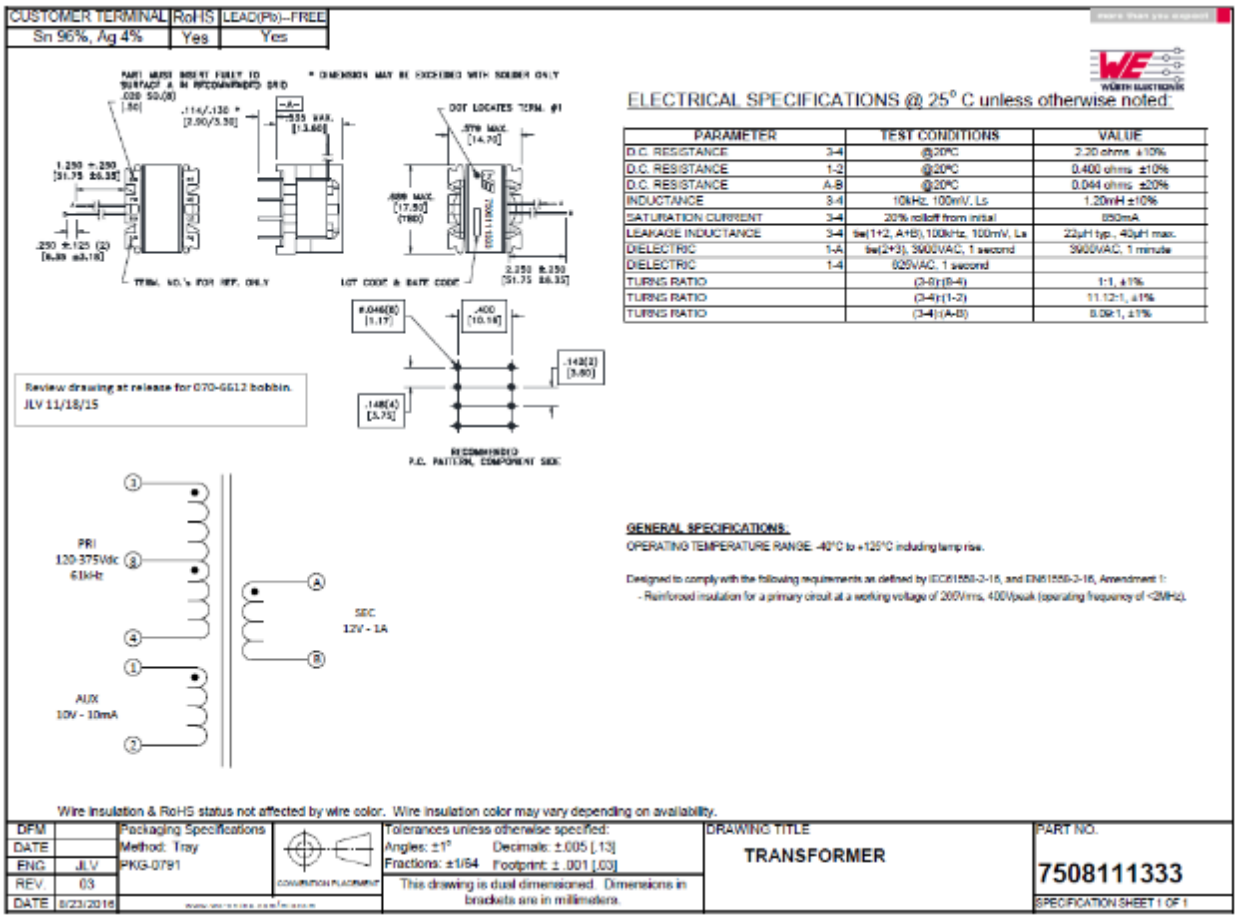

Figure 21. 12 V & 12 W Wurth Transformer Specifications

PCB Design

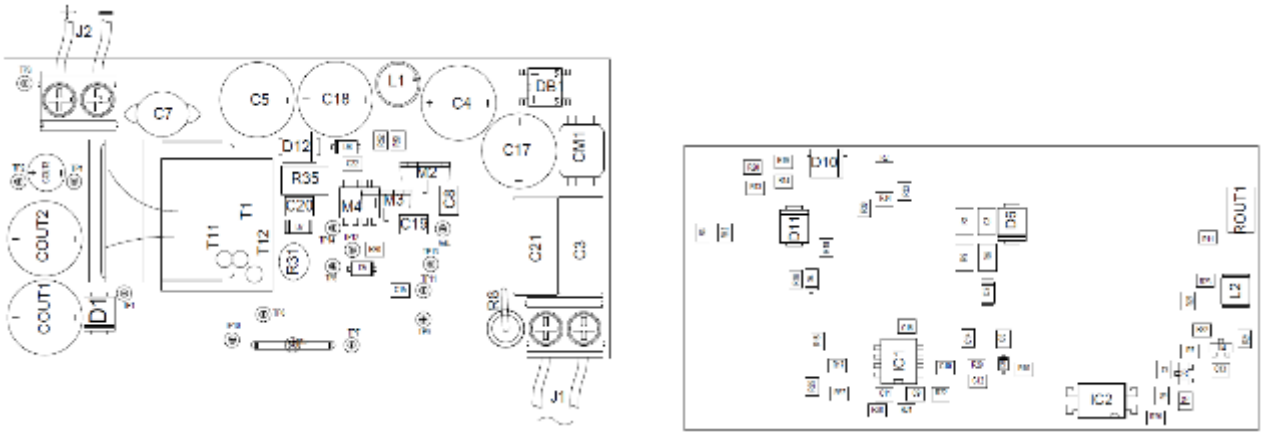

Figure 22. PCB Assembly Top & Bottom Views

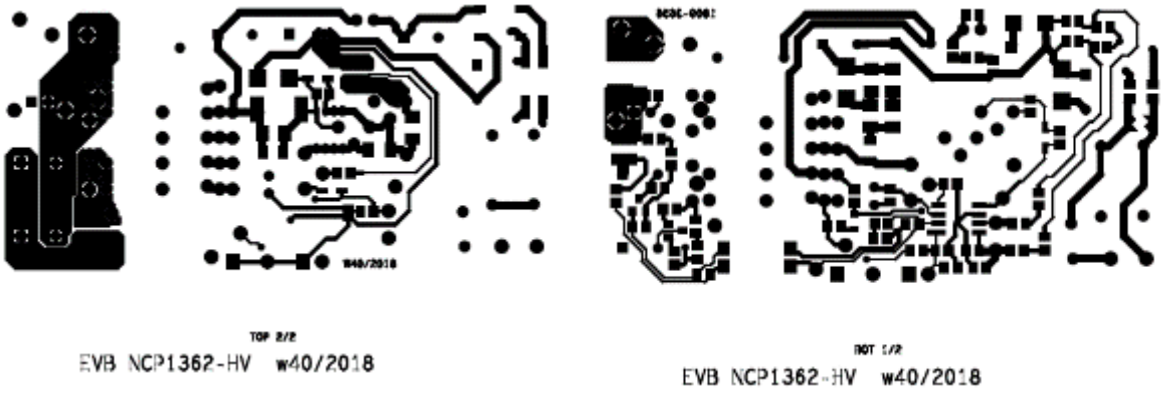

Figure 23. PCB Copper Tracks Top & Bottom Views

Conclusion

This application note has described the results obtained for a 12−W primary side regulation topology driven by the NCP1362 controller. Thanks to the dual frozen peak current in light and no load conditions, the consumption have been improved. The Line Feed Forward also brings a better constant current regulation compared to previous PSR generations. The controller offers all necessary protections needed to develop reliable power supply.

The implemented Dual Bulk capacitors solution allows to extend the input supply voltage to support Industrial / 3 phases supply without reliability compromise with good voltage margin of 1 kV Power MOS thanks to the Bulk OVP NCP1362's feature.

The secondary diode reversed voltage should be increased using Ultra−Fast Recovery instead of Schottky to get more voltage margin with 300 V diodes.

The author thanks Wurth Elektronik for the very good design support and sampling of transformer.

References

NCP1362 Datasheet, https://www.onsemi.com/pub/Collateral/NCP1362−D.PDF

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