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Maintaining Signal Integrity when Selecting ESD Protection for USB 3.0 Interface

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APPLICATION NOTE

$$\text{Where}: Z_0 = \sqrt{\frac{L}{C}} = \text{line impedance}$$

Figure 1. Lossless Transmission Line – Equivalent Circuit

Introduction

As today's lifestyle becomes more content rich through the use of streaming and sharing high quality video, photos, and music; data transfer rates have risen to new levels to keep up with the demand. High speed data rates are central to our ability to consume, share, back up, and create or edit content. With this increase in data transfer rates, chipset feature sizes are getting smaller and smaller which means the threat of Electrostatic Discharge (ESD) is more real now than ever before. This Application Note will discuss the challenges that designers are facing with regards to signal integrity when selecting ESD protection products for USB 3.0 and how ON Semiconductor's solutions overcome those challenges.

The Challenge to Preserve USB 3.0 Signal Quality

USB 3.0 is the latest revision in the Universal Serial Bus (USB) standard which allows data transfer rates up to 5 Gbit/s, over 10 times the 480 Mbit/s speed of USB 2.0.

In order to achieve the 5 Gbit/s data rate, two differential data pairs (SuperSpeed Tx and Rx) have been added to the already existent USB 2.0 data pair, D+ and D−. In addition, chipsets today that support USB 3.0 interfaces have process geometries as low as 22 nm in order to support the fast data rate. With the decrease in feature size of USB 3.0 compatible chipsets, the SuperSpeed lines that carry the USB 3.0 data signal become very sensitive to transients such as ESD. Not only is it critical to suppress ESD transients on these lines, it is also important to not degrade the quality of the USB 3.0 signal transmission. The increase in frequency, compared to USB 2.0 transmission, creates a strict impedance matching window that must be met when placing an external ESD protection device on the SuperSpeed lines. Any small amount of capacitance that is added to the signal line can change its impedance and thus degrade the overall signal integrity of the transmission. It is critical that designers understand the important device parameters of ESD protection products that can affect the impedance path of the data line.

Capacitance

Figure 1 shows a circuit representation of a lossless transmission line where the nominal impedance is represented by Z_0.

This transmission line model can be applied to a high speed data line present in almost any of today's high speed serial interfaces. The model can also be used to evaluate the effect of placing an ESD protection device onto the data line/s.

In its most basic form, an ESD protection device can be viewed as a Zener diode placed on the data line it is to protect. This zener diode has an associated junction capacitance, along with a small amount of series inductance from the internal bond wires in the package, which become parasitic to the data line as shown in Figure 2. Since the inductance of a typical wire bond in an ESD protection device is typically 1 nH or less and the capacitance of the ESD protection element must be 1 pF or below, the impedance of the inductors in Figure 2 are always well below the impedance of the capacitances at the 2.5 GHz speed of the USB signal. For that reason the inductance will be ignored in this discussion.

Figure 2. ESD Protection Device – Parasitic Model

As voltage on the data line changes, a small amount of current is needed to charge the parasitic capacitor. At high frequencies, where the voltage on the signal line is changing rapidly, this ex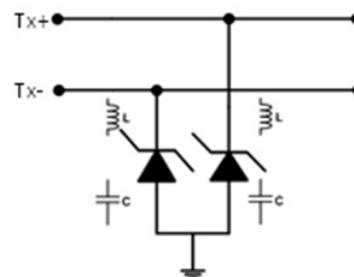tra charging current can be quite large, thus reducing the overall current flow in the data line. This reduction causes a slight change in impedance of the signal line and affects the amount of power being transferred on the line. If the power transfer loss is excessive, degradation in the data line signal integrity will occur. To limit the amount of parasitic capacitance in systems that use high speed serial interfaces, the maximum amount of parasitic capacitance is normally listed in the interface specification. The USB 3.0 specification lists a max of 1.1 pF maximum for parasitic capacitance. This maximum spec includes any capacitance in the system that is external to the USB controller. ESD protection devices are only a fraction of the external capacitance in the system. Therefore, when choosing ESD protection solutions, the designer should always keep in mind that lower capacitance of the protection device not only preserves signal integrity on the data lines, but also allows for more of a capacitance budget to work with in the downstream system. Table 1 shows the maximum capacitance of ON Semiconductor's ESD protection solution compared to three other competitor ESD protection solutions for the USB 3.0 interface.

It is practice that almost all ESD protection device suppliers will spec the junction capacitance at 1 MHz frequency. However, there a few suppliers that specify the capacitance at higher frequencies as seen by Competitor B

in Table 1. A capacitance measurement across frequency should be considered in order to get a good representation of the actual device capacitance over the frequency of normal operation in a high speed application. In USB 3.0, this equates to a measurement at the fundamental frequency of 2.5 GHz and its third harmonic frequency of 7.5 GHz (harmonics will be discussed later). As with any capacitor, its capacitance will vary over the frequency at which it is used due to its own parasitic resistance called ESR (Equivalent Series Resistance). The impedance of the capacitor will stay capacitive with low ESR at lower frequencies and continue to decrease until the resonance frequency of the capacitor is reached. Once resonance is reached, the impedance of the capacitor becomes inductive as the ESR increases. Figure 3 highlights this characteristic as a sample capacitor's impedance response over frequency plot is shown.

Table 1. CAPACITANCE COMPARISON OF USB 3.0 ESD PROTECTION DEVICES

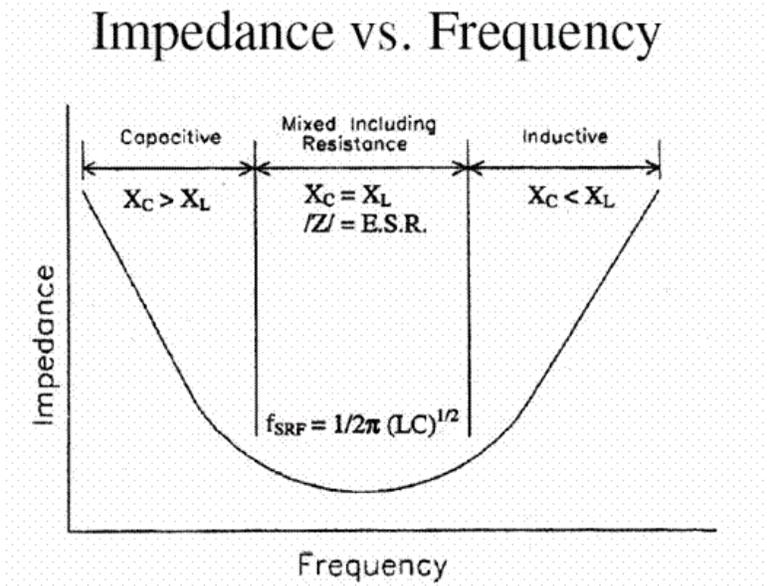| USB 3.0 ESD Protection Device (Diode Arrays)	Max Junction Capacitance (pF) Specified on Datasheet
ON Semiconductor ESD7016MUTAG	0.20 pF @ Vr = 0 V, f = 1 MHz
Competitor A	0.65 pF @ Vr = 0 V, f = 1 MHz
Competitor B	– (0.20 @ 3 GHz)
Competitor C	– (0.45 TYP at 0 V)

Figure 3. Impedance vs. Frequency Characteristic for a Capacitor

The ESD protection devices listed in Table 1 were measured for capacitance over frequency as shown in Figure 4.
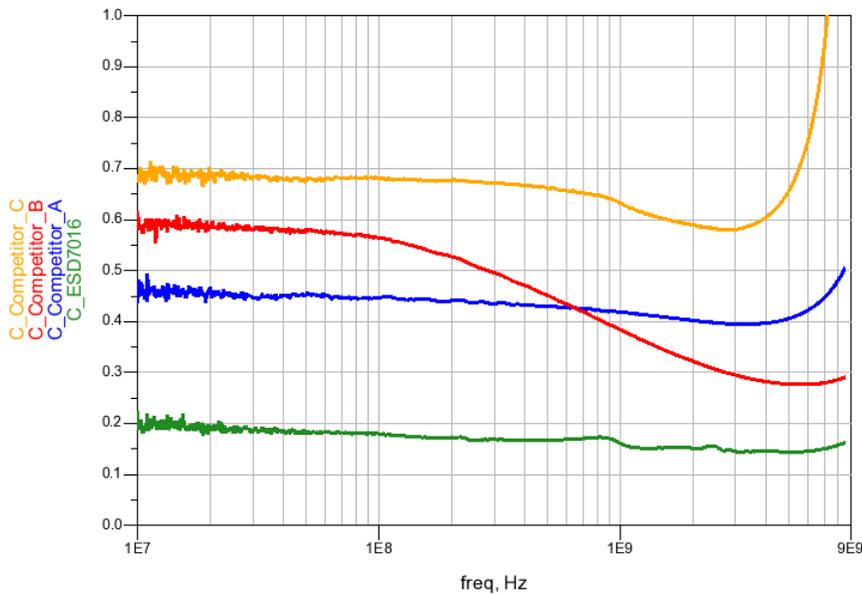
Figure 4. Capacitance Over Frequency Plot for Selected USB 3.0 ESD Protection Devices

As seen in Figure 4, competitor C's capacitance stays the highest over frequency and starts to become inductive around 3.5 GHz. Capacitance results from competitor B shows a significant decrease over frequency, dropping below competitor C's capacitance at higher frequencies. ON Semiconductor's ESD7016 provides a flat, 0.2 pF and below capacitance over frequency and does not reach resonance frequency out to 8.5 GHz. This plot is an example of how the capacitance of an ESD protection device varies over frequency and its results can correlate to how much the device affects the impedance path of the data line.

S Parameters, Return Loss, and Insertion Loss

Scattering parameters describe the behavioral model of how a interconnect or DUT interacts with an incident waveform. When a waveform is incident on a DUT, it can "scatter" back from the DUT and/or it can "scatter" into another interconnection. A point where the incident wave enters or exits the DUT is called a port for which two nodes, a and b, are defined. Node a represents where a wave enters a port and node b represents where a wave is reflected from the same port. Figure 1 can be redrawn with the addition of the ESD parasitic model to show how a two port electrical network containing the ESD protection device (the DUT in this case) is described (Figure 5).
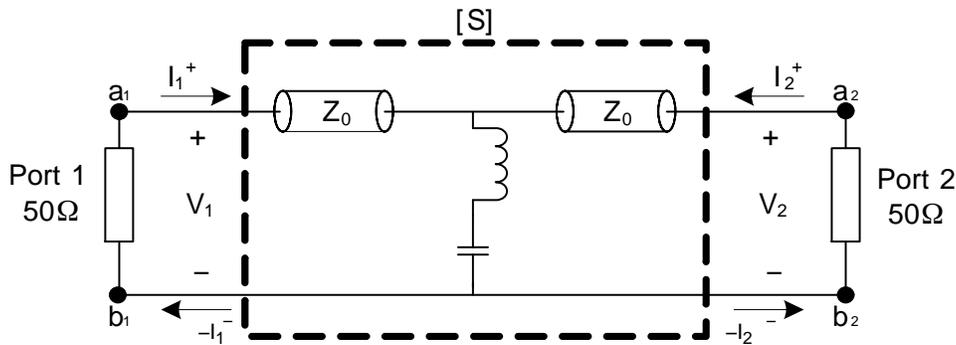

Figure 5. Two Port Electrical Network of Lossless Transmission Line

The signal flow diagram which describes how each S parameter is presented inside the behavior model [S] is drawn as the following in Figure 6.

As seen in Figure 6, each S parameter is the ratio of a wave scattered from the DUT at a specific port, to the wave incident to the DUT at a specific port.
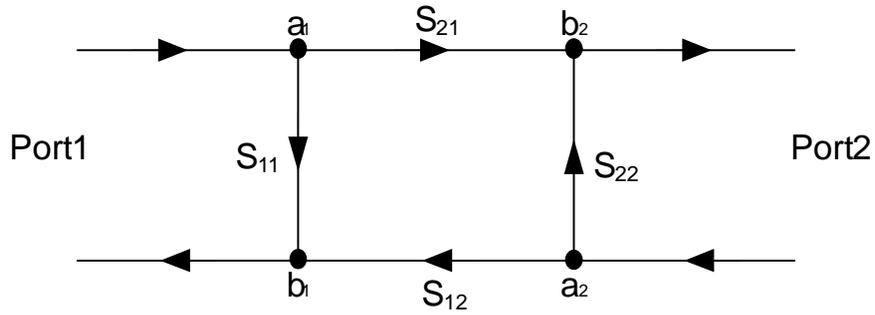
Figure 6. Signal Flow Diagram of the Two Port Electrical Network Shown in Figure 5

In every high speed interface application, the load impedance must be closely matched to source impedance. In USB 3.0 this impedance is matched to 90 Ω differential or 45 Ω per signal line. This matched load condition can be applied to the network in Figure 6 by terminating port 2 with a load impedance equal to that of Z_0. When this is the case, the reflected wave at node a_2 is equal to zero due to the incident wave being absorbed by the impedance matched load. This leaves the total energy of a signal, for the matched load case in a two port network, equal to the sum of the energy reflected (return loss) and energy transmitted (insertion loss). This can be represented using S parameters as shown in Equation 1. Both the insertion loss and return loss can be expressed in dB as shown in Equations 2 and 3. Both S parameters are important and can be used to measure how well the DUT is transparent to the system.

$$1 = S_{11}{}^2 + S_{21}{}^2 \qquad \text{(eq. 1)}$$

$$\text{Return Loss (dB)} = 10\log_{10}|S_{11}|^2 \qquad \text{(eq. 2)}$$

$$\text{Insertion Loss (dB)} = 10\log_{10}|S_{21}|^2 \qquad \text{(eq. 3)}$$

Both the S_{11} and S_{21} characteristic for the ESD protection device can be mapped over a suitable frequency range using a vector network analyzer (VNA). A VNA applies a signal of known amplitude and phase over a range of frequencies to port 1 and measures the signal amplitude and phase on port 2, allowing the measurement of S parameters as a function of frequency. The S_{11} and S_{21} characteristics of an ESD protection device can be measured with a VNA if the device is mounted on a circuit board with a 50 Ω through trace in order to match the VNA port impedance or if a direct probe connection to the device's pins is made. Because the VNA's ports can be calibrated before testing, the losses of the test coax cabling (Z_0 in Figure 5) are negligible. Figure 7 shows an S_{11} curve comparing the same USB 3.0 ESD protection devices used for evaluation throughout the note.
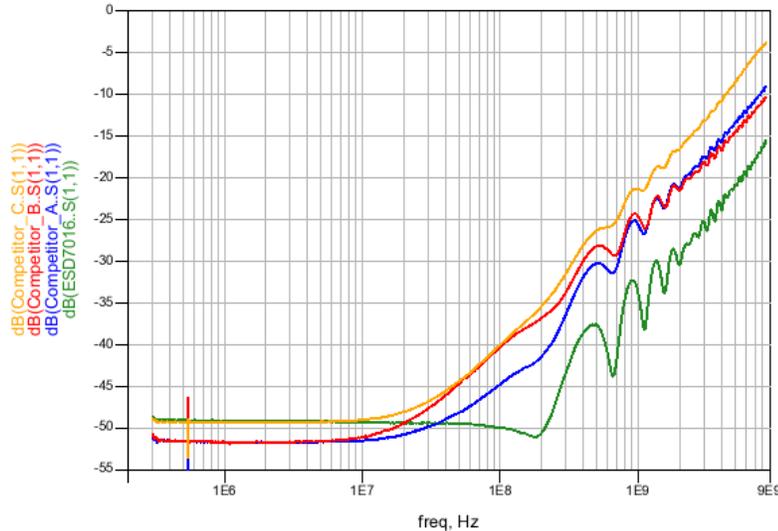

Figure 7. Return Loss (S_{11}) Characteristics of USB 3.0 ESD Protection Devices

Return loss is measuring how much loss is incurred by the incident wave reflecting off of the DUT. When the impedance throughout the DUT closely matches the Port 1 impedance, a small amount of the incident wave is reflected thus the return loss is small. This small amount of loss shows up as a large –dB value due to the impedance being matched between the two ports. The low capacitance of the ESD protection device that is parasitic to the line does not change the impedance enough and essentially the 50 Ω impedance of Port 2 effectively terminates the DUT. As frequency increases, the parasitic capacitance introduced by the ESD device changes the line impedance to where it is no longer

matching on each port and more of the incident wave gets reflected back into Port 1. This is seen as smaller –dB value on the return loss plot. ON Semiconductor's ESD7016 can be seen in Figure 7 as having the least amount of return loss thus keeping the interconnect the most transparent in comparison to the competitor devices. The lower the return loss of the ESD protection device means that less reflections are seen on Port 1 which translates into more of the signal, both amplitude and phase, being transmitted to Port 2. This is represented by a lower insertion loss and the plot containing the S_{21} characteristic for the ESD protection devices is shown in Figure 8.
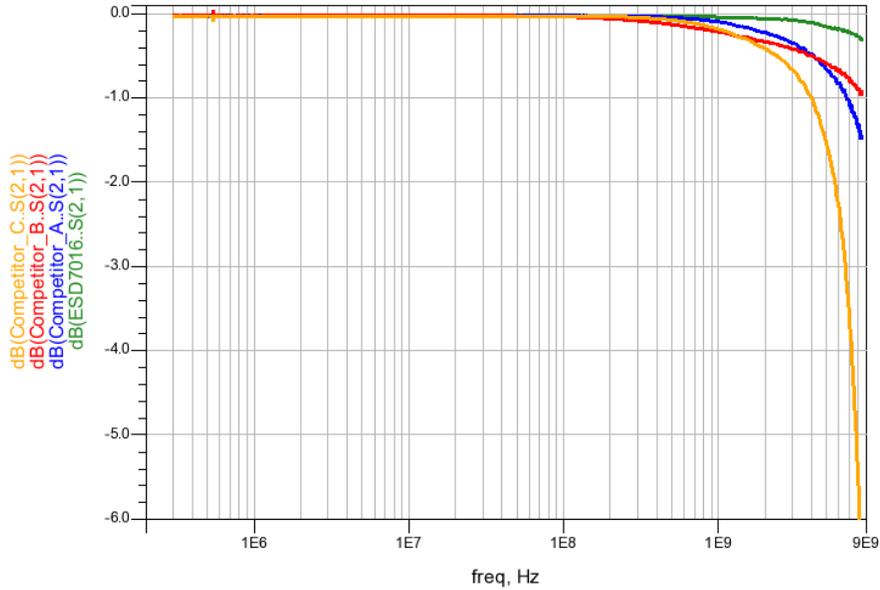

Figure 8. Insertion Loss (S_{21}) Characteristic of USB 3.0 ESD Protection Devices

Once again, ESD7016 shows the least amount of insertion loss across frequency with less than 0.5 dB of loss at 7.5 GHz. The competitor devices show loss close to or greater than 1 dB at 7.5 GHz, with competitor C being the highest with 4.5 dB of loss. This is primarily due to the fact that the parasitic capacitance has increased dramatically after 5 GHz due to the impedance reaching resonance and going inductive. It is also good to note that competitor A's device shows a better return and insertion loss above 5 GHz than competitor B's device. This is can be explained by device A having a lower capacitance value than device B at 5 GHz and above.

Signal loss due to reflection at the protection element is an important parameter whether it is expressed as return loss, S_{11}, or insertion loss, S_{21}. Each interface (USB, HDMI,

eSATA, etc…) transmits data at a different rate and consequently their data signals are operating at a different frequency. Because a typical data signal is a pattern of 1's and 0's transmitted over a line in the form similar to a square wave, the maximum frequency of the signal would be the pattern 1–0–1–0. With regards to USB 3.0, which has a data rate of 5 Gbit/s, this translates into the maximum frequency component being 2.5 GHz. Not only is it important to select an ESD protection device that contains little loss at this frequency, it is important to consider the spectral content of the data signal when comparing how much insertion loss is acceptable for the application. This can be understood with the Fourier series approximation of a square wave, shown in Equations 4 and 5.

$$x(t) = \frac{1}{2} + \frac{2}{\pi} \sum_{n=1}^{\alpha} \left[20 \frac{1}{2n-1} \sin((2n-1)\omega 0t) \right] \qquad \text{(eq. 4)}$$

$$x(t) = \frac{1}{2} + \frac{2}{\pi} \left[\frac{\sin(\omega 0t)}{1} + p20 \frac{\sin(3\omega 0t)}{3} + p20 \frac{\sin(5\omega 0t)}{5} + ... \right] \qquad \text{(eq. 5)}$$

Equation 5. (Simplified form of Equation 4)

From this, it can be seen that a square wave consists of odd order harmonics and to fully construct a square wave, it must go to infinity. However, to retain an acceptable portion of the waveform, the first two terms are generally sufficient. These two terms, the first and third harmonic, contain about 85% of the signal's information and allow a reasonable square wave to be reconstructed. Therefore, to reasonably pass a square wave of frequency x, the minimum ESD protection device bandwidth necessary is 3x. Violating this principle will result in rounding of the data waveform and will cause problems in transmitting the correct data. Table 2 shows the comparison in insertion loss values from Figure 3 relative to the first and third harmonics of a USB 3.0 data signal.

Table 2. INSERTION LOSS RESULTS OF USB 3.0 ESD PROTECTION DEVICES

USB 3.0 ESD Protection Device (Diode Arrays)	Insertion Loss (dB) @ Fundamental Frequency (2.5 GHz)	Insertion Loss (dB) @ Third Harmonic Frequency (7.5 GHz)
ON Semiconductor ESD7016MUTAG	−0.066	−0.240
Competitor A	−0.285	−1.176
Competitor B	−0.375	−0.830
Competitor C	−0.534	−4.485

It can be seen from the results in Table 2 that the ESD7016 has the lowest loss of all devices tested, at both the fundamental and third harmonic frequencies of a USB 3.0 signal. The competitor devices, with higher capacitance, have losses closer to and greater than 1 dB at 7.5 GHz.

Board Layout Considerations

Another important aspect for designers to consider when selecting ESD protection devices is the board layout/routing scheme once the device is placed in the circuit. Steps must be taken to ensure the maximum signal integrity for the application. Such steps are listed below.

- Differential design methodology should be used to ensure that all USB 3.0 high speed signal traces are impedance matched to 90 Ω.
- Keep the trace lengths equal between the positive and negative lines of the differential data lanes to avoid common mode noise generation and impedance mismatch.
- Place grounds between high speed pairs and keep as much distance between pairs as possible to reduce crosstalk.
- Use curved traces when possible to avoid unwanted reflections.

The ESD7016 accommodates all four USB 3.0 SuperSpeed signal traces as well as both USB 2.0 signal traces. This allows the designer to place a GND connection between all three differential lanes, thus reducing crosstalk between the signal lines and eliminating the need to split up the SuperSpeed traces. The ESD7016 utilizes a small uDFN package to take advantage of industry preferred flow-thru routing scheme, making the ESD7016 a top-notch ESD protection array to provide easy board routing and high quality signal integrity in the USB 3.0 application. Figures 4 and 5 show the suggested routing schemes for both the USB 3.0 Standard A and MicroB connectors using the ON Semiconductor ESD7016 six line ESD protection array.
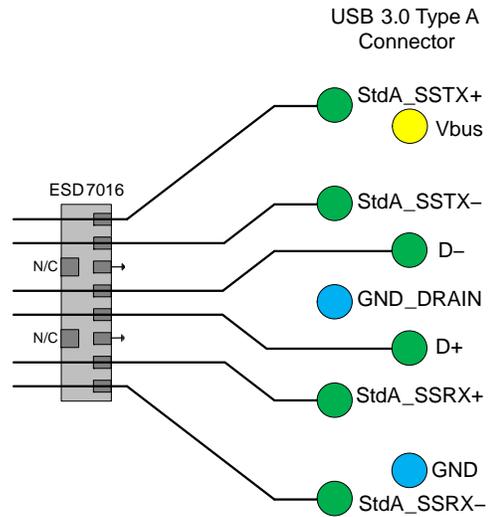

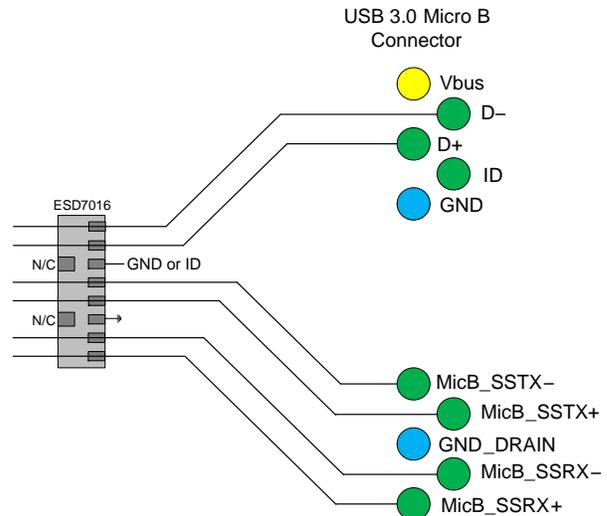**Figure 9. Suggested Routing Scheme Using ESD7016 for USB 3.0 Std_A Connector**

Figure 10. Suggested Routing Scheme Using ESD7016 for USB 3.0 Micro_B Connector

Summary

This Application Note discusses the important parameters to consider, regarding signal integrity, when selecting external ESD protection solutions for USB 3.0 applications. Too much parasitic capacitance, introduced by the ESD protection device, creates impedance mismatches by lowering the impedance of the USB 3.0 signal line and thus has the potential to degrade the signal quality. This was presented in the capacitance over frequency measurements as well as both the return loss (S_{11}) and insertion loss (S_{21}) measurements. These measurements showed that devices with higher capacitance, compared to ON Semiconductor ESD7016, showed more return and insertion loss at both the fundamental and third harmonic frequencies of the USB 3.0 data signal. The ESD7016 is a six I/O device that incorporates an industry leading low capacitance with a small form factor μDFN package to allow flow-thru routing. The combination of this device with good board layout techniques provides designers a high signal integrity, all-in one ESD protection solution that allows for a larger capacitance budget for USB 3.0 applications.

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