Key Steps to Design A Compact, High-Efficiency PFC Stage Using NCP1623A

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Description

This paper describes the key steps to rapidly design a CrM/DCM PFC stage driven by the NCP1623. The process is illustrated in a practical 100−W, universal mains application:

- Maximum Output Power: 100 W
- Rms Line Voltage Range: from 90 V to 264 V
- Regulation output voltage:
  - 250 V in low line (115−V mains)
  - 390 V in high line (230−V mains)

Introduction

There're several options of the NCP1623. This application note focuses on the A version (NCP1623A) which mainly differs from the other versions in the follower boost capability.

Housed in either SOIC−8 or TSOP−6 packages, the NCP1623A is an extremely compact PFC controller designed to optimize the efficiency of your PFC stage throughout the load range. It also incorporates protection features for a rugged operation. More generally, NCP1623A is ideal in systems where cost−effectiveness, reliability, high power−factor and efficiency ratios are key requirements:

- *Valley Synchronized Frequency Fold−back:*
  NCP1623A classically operates in *Cr*itical conduction *M*ode (*CrM*) until the power drops below a threshold level. At that moment, the PFC stage enters the *D*iscontinuous *C*onduction *M*ode (DCM) with a dead−time which prolongs as the load further decays (frequency foldback). This novel technique also provides stable valley turn−on for a maximized efficiency. In addition, the minimum frequency clamp (33 kHz typically) prevents audible frequencies and the on−time is modulated to ensure near−unity power factor in both CrM and DCM operations.
- *Compactness:*
  NCP1623A features the CS/ZCD multifunctional pin based on a novel technique which provides the input signals for an enhanced control and a large number of protections in a small TSOP6 (or SOIC8) package with few external components. In addition, the NCP1623A forces a lower output regulation level in low−line conditions to maximize the PFC stage efficiency and reduce its size. This 2−level Follower Boost technique best fits for applications where the downstream converter (like a flyback power supply) can withstand input voltage variations in a cost−effective and efficient manner.
- *Low VCC startup threshold:*
  NCP1623A is designed to start up when its VCC voltage exceeds 10.5 V typically, making it ideal in applications where the controller is fed by an external power source (from an auxiliary power supply or from a downstream converter). Its maximum start−up level (11.25 V) is set low enough to be powered from traditional 12−V rails. After start−up, the high VCC maximum rating allows a large operating range from 9.5 V up to 30 V, thus easing the circuit feeding.
- *Fast Line / Load Transient Compensation:*
  Since the regulation loop bandwidth of PFC stages must be low, abrupt changes in the load or input voltage (e.g. at start−up) may cause excessive over− or under−voltages. The over−voltage protection interrupts the power delivery when the output voltage is excessive. The circuit dramatically speeds up the regulation loop when the output voltage goes below the low detect threshold (dynamic response enhancer − DRE). This function is enabled only after the PFC stage has started up to allow normal soft−start operation to occur.
- *Safety Protections:*
  The system permanently monitors the input and output voltages, the MOSFET current and the die temperature to protect the system from possible over−stress making the PFC stage extremely robust and reliable. In addition to the OVP protection, the following methods of protection are provided:
  - *Maximum Current Limit:* The circuit senses the MOSFET current and turns it off if the sensed current exceeds the set current limit. In addition, the circuit enters a low duty−cycle operation mode when the current reaches 150% of the current limit as a result of an inductor saturation or a short of the bypass diode.
  - *Under−Voltage Protection:* This circuit turns off when the feedback pin voltage (V_{FB}) drops below 300 mV and remains off until V_{FB} exceeds 530 mV. When the follower boost is enabled at low−line, FB pin sources 25 uA current ($I_{FB(LL)}$) to regulate lowered output voltage and UVP hysteretic thresholds are increased to 1.2/1.3 V. This feature protects the PFC stage if the ac line is too low at startup or if there is a failure in the feedback network (e.g., accidental short−to−ground failure of the feedback pin).

- *Redundant over−voltage protection (OVP2):* CS/ZCD multi−functional pin is used to detect excessive output voltage levels and prevent a destructive output voltage runaway if the feedback network happens to be wrong (incorrect resistors value, aging effects...)
- *Thermal Shutdown:* An internal thermal circuitry disables the gate drive when the junction temperature exceeds 150°C (typically). The circuit resumes operation once the temperature drops below approximately 100°C (50°C hysteresis).

- *Eased Manufacturing and Safety Testing:*
  Elements of the PFC stage can be accidently shorted, badly soldered or damaged as a result of manufacturing or handling incidents, excessive operating stress or other troubles. In particular, adjacent pins of controllers can be shorted, grounded or badly connected. It is often required that such open/short situations do not cause fire, smoke nor loud noise. The NCP1623A integrates enhanced functions that help address the requirement, for instance, in case of an improper pin connection (including GND) or of a short of the boost or bypass diode.

Compared to the TSOP−6 version, the SOIC−8 option further features the sleep mode controlled by the DIS pin. A high level or open circuit on this pin disables the controller and reduces ICC bias current to less than 20 μA typically. This function helps meet the most severe standby power requirements.

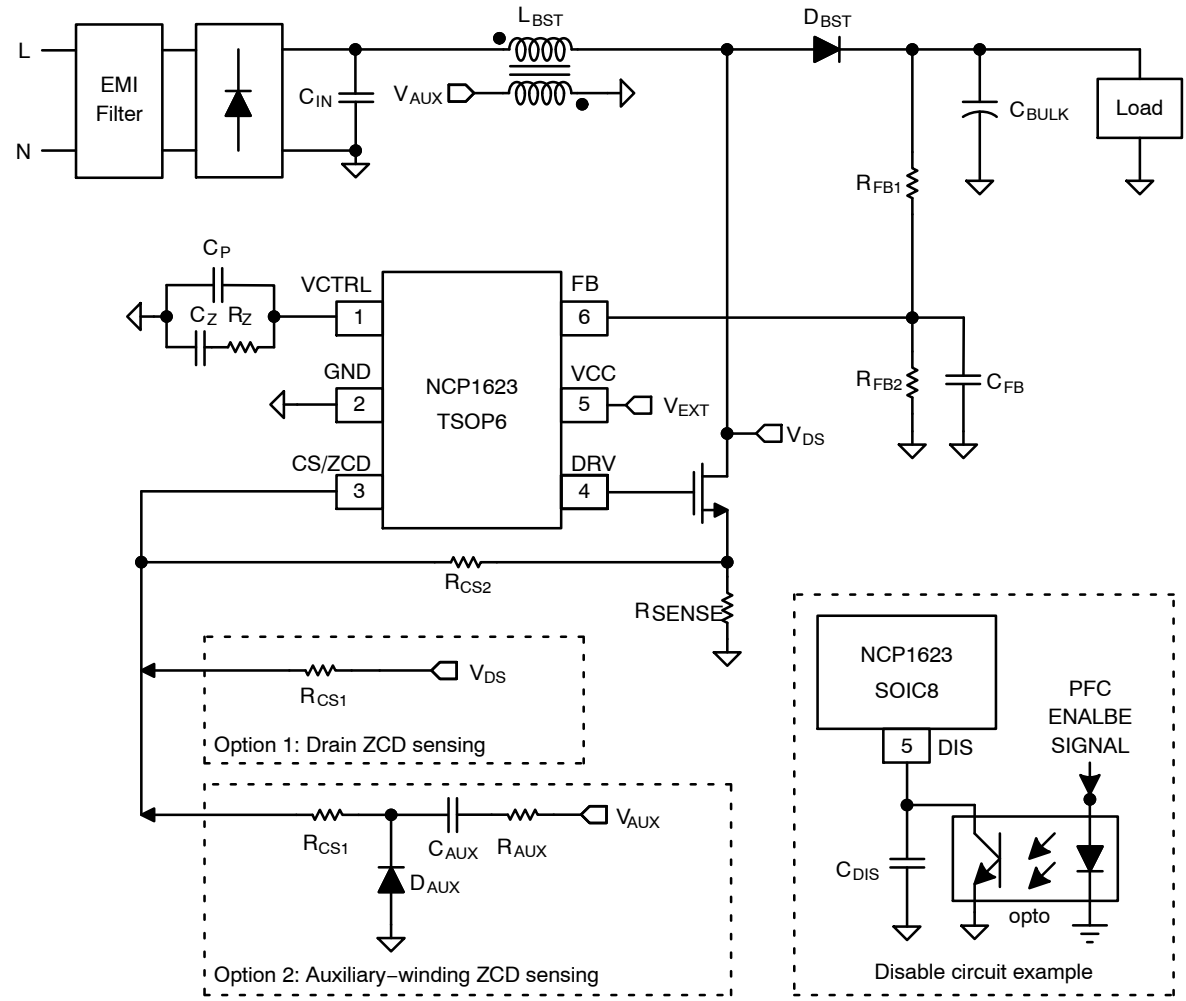

Figure 1. System Board Schematic

STEP 1: DEFINE KEY SPECIFICATIONS

- *Line frequency, f_{line}:*
  50 Hz /60 Hz applications are targeted. Practically, they are often specified in a range of 47 − 63 Hz. For calculations such as hold−up time, one has to factor in the lowest value specified.
- *The lowest line voltage, $(V_{line,rms})_{LL}$:*
  This is the minimum rms input voltage for which the PFC stage must operate. Such a level is usually 10 − 12% below the minimum typical voltage which could be 100 V in many countries. We will take: $(V_{line,rms})_{LL} = 90\ V$.
- *The highest line voltage, $(V_{line,rms})_{HL}$:*
  This is the maximum input rms voltage. It is usually 10% above the maximum typical voltage (240 V in many countries). We select: $(V_{line,rms})_{HL} = 264\ V$.
- *Nominal voltage, $V_{out,nom}$:*
  This is the high−line regulation level. $V_{out,nom}$ must be higher than $\left(\sqrt{2} \cdot (V_{line,rms})_{HL}\right)$. 390 V is our target value.
- *Output voltage at low line, $V_{out,LL}$:*
  The NCP1623A follower boost function provides the capability to select a lower regulation level at low line for a size and efficiency optimization of the PFC stage. It is generally set just above the high−line detection threshold. 250 V is our target value.
- *Peak−to−peak output voltage ripple, $(\delta V_{out})_{pk-pk}$:*
  This parameter is often specified in percentage of output voltage. It must be selected equal or lower than 6% V_{FB} peak−to−peak ripple to avoid triggering the Dynamic Response Enhancer (DRE) in normal operation.
- *Hold−up time, $t_{HOLD-UP}$:*
  This parameter specifies the amount of time the output will remain valid during line drop−out. One line cycle is typically specified. This requirement requires knowing the minimum voltage on the PFC stage output necessary for the proper operation in your application ($V_{out,min}$). We have assumed ($V_{out,min}$ = 180 V) is high enough to provide the downstream converter with a sufficient input voltage.
- *Output power, P_{out}:*
  This is the power consumed by the PFC load.
- *Maximum output power, $P_{out,max}$:*
  This is the maximum output power level, that is, 150 W in our application.
- *Maximum input power, $(P_{in,avg})_{max}$:*
  This is the maximum power that can be absorbed from the mains in normal operation. This level is obtained at full load, low line. Assuming an efficiency of 95% in these conditions, we will use:

$$\left(P_{in,avg}\right)_{max} = \frac{100}{95\%} \cong 105\ W \qquad \text{(eq. 1)}$$

STEP 2: POWER STAGE DESIGN

In heavy load conditions, the NCP1623A operates in Critical conduction Mode (CrM). Hence, the inductor, the bulk capacitor and the power silicon devices are dimensioned as usually done with any other CrM PFC. This chapter does not detail this process, but simply highlights key points.

PFC Inductor

The on−time of the circuit is internally limited. The power the PFC stage can deliver, depends on the inductor since L will determine the current rise for a given on−time. More specifically, the following equation gives the power capability of the PFC stage:

$$\left(P_{in,avg}\right)_{max} = \frac{V_{line,rms}^{2}}{2L} \cdot T_{on,max} \qquad \text{(eq. 2)}$$

The smaller the inductor, the higher the PFC stage power capability. Hence, L must be low enough so that the full power can be provided at the lowest line level:

$$L \le \frac{\left(V_{line,rms}\right)_{LL}^{2}}{2 \cdot \left(P_{in,avg}\right)_{max}} \cdot T_{on,max} \qquad \text{(eq. 3)}$$

Like in traditional CrM applications, the following equations give the other parameters of importance:

- Maximum peak current:

$$\left(I_{L,pk}\right)_{max} = 2\sqrt{2}\frac{\left(P_{in,avg}\right)_{max}}{\left(V_{line,rms}\right)_{LL}} \qquad \text{(eq. 4)}$$

- Maximum rms current:

$$\left(I_{L,rms}\right)_{max} = \frac{\left(L_{L,pk}\right)_{max}}{\sqrt{6}} \qquad \text{(eq. 5)}$$

In our application, the inductor must then meet the following requirements:

$$L \le \frac{90^2}{2 \cdot 105} \cdot 10.8\ \mu \cong 417\ \mu H$$

$$\left(I_{L,pk}\right)_{max} = 2\sqrt{2}\frac{105}{90} \cong 3.3\ A$$

$$\left(I_{L,rms}\right)_{max} = \frac{3.3}{\sqrt{6}} \cong 1.35\ A \qquad \text{(eq. 6)}$$

The minimum value for $T_{on,max}$ (the typical value being 12.5 μs) is 10.8 μs which is used in equation 6 since this is the worst case when calculating L. It is recommended to select an inductor value that is at least 25% less than that returned by equation 6 for a healthy margin. A 200−μH inductor is selected for system compactness. It consists of a 10:1 auxiliary winding for zero current detection. One can note that the switching frequency in CrM operation depends on the inductor value:

$$f_{sw} = \frac{V_{line}(t)^2 \cdot \left(V_{out} - V_{line}(t)\right)}{4 \cdot P_{in,avg} \cdot V_{out} \cdot L} \qquad \text{(eq. 7)}$$

For instance, at low line, full load (top of the sinusoid), the switching frequency is:

$$f_{sw} = \frac{\left(\sqrt{2} \cdot 90\right)^2 \cdot \left(250 - \sqrt{2} \cdot 90\right)}{4 \cdot 105 \cdot 250 \cdot 200 \cdot 10^{-6}} \cong 95\ \text{kHz} \quad \text{(eq. 8)}$$

Above calculation takes into account that the low−line regulation voltage is 250 V.

In the real design, PFC output power is not ideally delivered at input voltage zero cross so that the actual turn−on time is increased to regulate the desired load. As the turn−on time is lengthened, the inductor peak and rms current are higher and the switching frequency is lowered compared to the calculation results in equation 4, equation 5 and equation 7. Therefore, it is recommended to add at least 20% margin in the equations.

Power Devices

Generally, the diode bridge and the power switch are placed on the same heat−sink. As a rule of the thumb, one can estimate that the heat−sink will have to dissipate around:

- 4% of the output power in wide mains applications (95 % being generally the targeted minimum efficiency)
- 2% of the output power in single mains applications.

In our wide−mains application, about 4 W are then to be dissipated.

Among the sources of losses that contribute to this heating, one can list:

- The diodes bridge conduction losses that can be estimated by the following equation:

$$\left(P_{bridge}\right)_{max} = 2 \cdot V_f \cdot \frac{\frac{2\sqrt{2}}{\pi} \cdot \frac{P_{out,max}}{\eta}}{\left(V_{line,rms}\right)_{LL}} \approx \frac{1.8 \cdot V_f \cdot P_{out,max}}{\left(V_{line,rms}\right)_{LL} \cdot \eta} \quad \text{(eq. 9)}$$

where V_f is the forward voltage of the bridge diodes.

- The MOSFET conduction losses are given by:

$$\left(P_{on}\right)_{max} = \frac{4}{3} \cdot R_{DS(on)} \cdot \left(\frac{P_{out,max}}{\eta \cdot \left(V_{line,rms}\right)_{LL}}\right)^2 \cdot \left(1 - \frac{8\sqrt{2} \cdot \left(V_{line,rms}\right)_{LL}}{3\pi \cdot V_{out,LL}}\right) \quad \text{(eq. 10)}$$

In our application, we have:

- P_{bridge} = 2.1 W, assuming that V_f is 1 V.
- $(P_{on})_{max}$ = 1.03 · $R_{DS(on)}$ W. Assuming that $R_{DS(on)}$ doubles at high temperature, the maximum conduction losses are about 2.6 · $R_{DS(on)}$ W.

Switching losses cannot be easily computed. We will not attempt to predict them. Instead, as a rule of the thumb, we will assume a loss budget equal to that of the MOSFET conduction ones. Experimental tests will check that they are not under−estimated.

The boost diode is the source of the following conduction losses: $I_{OUT} \cdot V_f$, where I_{OUT} is the load current and V_f the diode forward voltage. The maximum output current being 0.4 A at low line (when the regulation level is set to 250 V), the diode conduction loss is in the range of 0.4 W (assuming V_f = 1 V). P_{DIODE} = 0.4 W.

PFC Output Bulk Capacitor

There generally are three main criteria / constraints when defining the bulk capacitor:

- Peak−to−peak output voltage ripple:

$$\left(\delta V_{out}\right)_{pk-pk} = \frac{P_{out,max}}{C_{BULK} \cdot \omega \cdot V_{out,LL}} \quad \text{(eq. 11)}$$

where ($\omega = 2\pi \cdot f_{line}$) is the line frequency.

The peak−to−peak FB pin voltage ripple, $(\delta V_{FB})_{pk-pk}$, is generally kept lower than ±3% (6% peak−to−peak) from FB reference voltage (V_{REF} = 2.5 V), not to trig the OVP and DRE functions with a good margin in nominal operation. Feedback resistor divider ratio is given by:

$$\frac{R_{FB2}}{R_{FB1} + R_{FB2}} = \frac{V_{REF}}{V_{out,nom}} \quad \text{(eq. 12)}$$

So, peak−to−peak FB voltage is:

$$\left(\delta V_{FB}\right)_{pk-pk} = \left(\delta V_{out}\right)_{pk-pk} \frac{R_{FB2}}{R_{FB1} + R_{FB2}} = \left(\delta V_{out}\right)_{pk-pk} \frac{V_{REF}}{V_{out,nom}} \quad \text{(eq. 13)}$$

Therefore, minimum C_{BULK} to limit the V_{FB} ripple in 6% at 47 Hz line frequency is:

$$C_{BULK} \geq \frac{P_{out,max}}{6\% \cdot V_{out,nom} \cdot \omega \cdot V_{out,LL}} = \frac{100}{6\% \cdot 390 \cdot 2\pi \cdot 47 \cdot 250} \cong 50\ \mu\text{F} \quad \text{(eq. 14)}$$

- Hold−up time specification:

$$C_{BULK} \geq \frac{2 \cdot P_{out,max} \cdot t_{HOLD-UP}}{V_{out,LL}^2 - V_{out,min}^2} = \frac{2 \cdot 100 \cdot 10m}{250^2 - 180^2} \cong 66\ \mu\text{F} \quad \text{(eq. 15)}$$

where hold−up time is 10 ms

- Rms capacitor current:

The rms current depends on the load characteristic. Assuming a resistive load, we can derive the following approximate expression of its magnitude:

$$\left(I_{c,rms}\right)_{max} \cong \sqrt{\frac{32\sqrt{2}}{9\pi} \cdot \frac{\left(P_{in,avg}\right)_{max}^2}{\left(V_{line,rms}\right)_{LL} \cdot V_{out,LL}} - \left(\frac{P_{out,max}}{V_{out,LL}}\right)^2} \quad \text{(eq. 16)}$$

In our application, we have:

$$\left(I_{c,rms}\right)_{max} \cong \sqrt{\frac{32\sqrt{2}}{9\pi} \cdot \frac{105^2}{90 \cdot 250} - \left(\frac{100}{250}\right)^2} \cong 0.79\ \text{A} \quad \text{(eq. 17)}$$

STEP 3: IC CONTROL CIRCUIT DESIGN

FB Pin Circuit

As shown by Figure 1, the feed−back arrangement consists of:

- A resistor divider that scales down the bulk voltage to provide the FB pin with the feedback signal. The upper resistor of the divider generally consists of two or three resistors for safety considerations. If not, any accidental shortage of R_{FB1} would apply the output high voltage to the controller and destroy it.
- A filtering capacitor that is often placed between the FB pin and ground to prevent switching noise from distorting the feedback signal. A 1−nF capacitor is often implemented. Generally speaking, the pole it forms with the feedback resistors must remain at a very high−frequency compared to the line one. Practically,

$$C_{FB} \leq \frac{1}{150 \cdot \left(R_{FB1} \parallel R_{FB2}\right) \cdot f_{line}} \quad \text{(eq. 18)}$$

generally gives good results.

- A type−2 compensation network. Consisting of two capacitors and of one resistor, this circuitry sets the crossover frequency and the loop characteristic.

The A version (NCP1623A) features the follower boost capability. This technique consists of reducing the output voltage to optimize the PFC stage efficiency and significantly shrink its size and cost. In particular, the boost inductance and the MOSFET losses can be dramatically reduced. Since the output voltage must remain higher than the line voltage, the output voltage is lowered in low line only while it remains regulated to the default nominal level ($V_{out,nom}$ generally set to 400 V or so) in high line conditions. Practically, the NCP1623A controls this 2−level follower boost operation through the feedback pin which sources the current $I_{FB(LL)}$ (25 μA typically) enabled only at low line.

As detailed in the data sheet, this leads to the following regulation levels:

- Output voltage at high−line, $V_{out,HL} = V_{out,nom}$:

$$V_{out,nom} = V_{REF} \cdot \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \quad \text{(eq. 19)}$$

- Output voltage at low line, $V_{out,LL}$:

$$V_{out,LL} = V_{out,nom} - R_{FB1} \cdot I_{FB(LL)} \quad \text{(eq. 20)}$$

Based on the output voltage spec at high and low line of our application, the feedback resistor values are obtained by:

- Upper feedback resistor, R_{FB1}

$$R_{FB1} = \frac{V_{out,nom} - V_{out,LL}}{I_{FB(LL)}} = \frac{390 - 250}{25\ \mu} = 5.6\ M\Omega \quad \text{(eq. 21)}$$

- Lower feedback resistor, R_{FB2}

$$R_{FB2} = \frac{R_{FB1} \cdot V_{REF}}{V_{out,nom} - V_{REF}} = \frac{5.6\ M \cdot 2.5}{390 - 2.5} = 36\ k\Omega \quad \text{(eq. 22)}$$

After selecting R_{FB1} and R_{FB2}, FB pin−related functions are defined as below in our application:

- Feedback resistor ratio, K_{FB}:

$$K_{FB} = \frac{R_{FB1} + R_{FB2}}{R_{FB2}} = \frac{5.6\ M\Omega + 36\ k\Omega}{36 k\Omega} \approx 157 \quad \text{(eq. 23)}$$

- Follower boost offset voltage, $V_{OFF(LL)}$:

$$V_{OFF(LL)} = R_{FB1} \cdot I_{FB(LL)} = 5.6\ M\Omega \cdot 25\ \mu = 140\ V \quad \text{(eq. 24)}$$

- DRE enter/exit V_{OUT} at high−line,

$$V_{OUT(DRE-EN/EX-HL)} = V_{REF} \cdot K_{FB(DRE-XX)} \cdot K_{FB} \quad \text{(eq. 25)}$$

Enter: 2.5 · 95.5% · 157 ≈ 375 V

Exit: 2.5 · 97.5% · 157 ≈ 383 V

- DRE enter/exit V_{OUT} at low−line,

$$V_{OUT(DRE-EN/EX-LL)} = V_{REF} \cdot K_{FB(DRE-XX)} \cdot K_{FB} - V_{OFF(LL)} \quad \text{(eq. 26)}$$

Enter: 2.5 · 95.5% · 157 − 140 ≈ 235 V

Exit: 2.5 · 97.5% · 157 − 140 ≈ 243 V

- SOVP enter/exit V_{OUT} at high−line,

$$V_{OUT(SOVP-EN/EX-HL)} = V_{REF} \cdot K_{FB(SOVP-XX)} \cdot K_{FB} \quad \text{(eq. 27)}$$

Enter: 2.5 V · 105% · 157 ≈ 412 V

Exit: 2.5 V · 103% · 157 ≈ 404 V

- SOVP enter/exit V_{OUT} at low−line,

$$V_{OUT(SOVP-EN/EX-LL)} = V_{REF} \cdot K_{FB(SOVP-XX-LL)} \cdot K_{FB} - V_{OFF(LL)} \quad \text{(eq. 28)}$$

Enter: 2.5 V · 110% · 157 − 140 ≈ 292 V

Exit: 2.5 V · 108% · 157 − 140 ≈ 284 V

- FOVP enter/exit V_{OUT} at high−line,

$$V_{OUT(FOVP-EN/EX-HL)} = V_{REF} \cdot K_{FB(FOVP-XX)} \cdot K_{FB} \quad \text{(eq. 29)}$$

Enter: 2.5 V · 107% · 157 ≈ 420 V

Exit: 2.5 V · 105% · 157 ≈ 412 V

- FOVP enter/exit V_{OUT} at low−line,

$$V_{OUT(FOVP-EN/EX-LL)} = V_{REF} \cdot K_{FB(FOVP-XX-LL)} \cdot K_{FB} - V_{OFF(LL)} \quad \text{(eq. 30)}$$

Enter: 2.5 V · 114% · 157 − 140 ≈ 307 V

Exit: 2.5 V · 112% · 157 − 140 ≈ 300 V

- UVP enter/exit V_{OUT} at high−line,

$$V_{OUT(UVP-EN/EX-HL)} = V_{FB(UVP-XX)} \cdot K_{FB} \quad \text{(eq. 31)}$$

Enter: 0.3 V · 157 ≈ 47 V

Exit: 0.53 V · 157 ≈ 83 V

- UVP enter/exit V_{OUT} at low−line,

$$V_{OUT(UVP-EN/EX-LL)} = V_{FB(UVP-XX)} \cdot K_{FB} - V_{OFF(LL)} \quad \text{(eq. 32)}$$

Enter: 1.2 V · 157 − 140 ≈ 48 V

Exit: 1.3 V · 157− 140 ≈ 64 V

VCTRL Pin Circuit

In order to find the control to output transfer function, the output voltage is defined by the multiplication of the output current and the output impedance. Using equation 2 and assuming the efficiency is 100%, the output current is given by:

$$i_{out}\left(v_{ctrl},\, v_{out}\right) = \frac{p_{in}}{v_{out}} = \frac{V_{line,rms}^{\,2} \cdot t_{on}}{2 \cdot L \cdot v_{out}} = \frac{V_{line,rms}^{\,2} \cdot T_{on.max} \cdot \left(v_{ctrl} - 0.5\right)}{8 \cdot L \cdot v_{out}} \quad \text{(eq. 33)}$$

The output current partial differentiation by the output voltage is equivalently the output load resistance, R_{load}, based on the equation:

$$\frac{\delta i_{out}}{\delta v_{out}} = -\frac{V_{line,rms}^{\,2} \cdot T_{on.max} \cdot \left(V_{ctrl} - 0.5\right)}{8 \cdot L \cdot v_{out}^{\,2}} = -\frac{i_{out}}{v_{out}} = -\frac{1}{R_{load}} \quad \text{(eq. 34)}$$

Therefore, $\delta i_{out} / \delta v_{out}$ can be included in the output impedance and total output impedance is:

$$z_{out}(s) = R_{load} \parallel R_{load} \parallel \frac{1}{s \cdot C_{BULK}} \quad \text{(eq. 35)}$$

The output current partial differentiation by the control voltage is:

$$\frac{\delta i_{out}}{\delta v_{ctrl}} = -\frac{V_{line,rms}^{\,2} \cdot T_{on.max}}{8 \cdot L \cdot V_{out}} \quad \text{(eq. 36)}$$

As a result, the control to output transfer function is defined by:

$$\frac{\delta v_{out}(s)}{\delta v_{ctrl}(s)} = \frac{\delta i_{out}}{\delta v_{ctrl}} \cdot z_{out}(s) = \frac{V_{line,rms}^{\,2} \cdot T_{on.max} \cdot R_{load}}{16 \cdot L \cdot V_{out}} \cdot \frac{1}{1 + s \cdot R_{load} \cdot C_{BULK} / 2} = G_0 \cdot \frac{1}{1 + s \cdot R_{load} \cdot C_{BULK} / 2} \quad \text{(eq. 37)}$$

where $T_{on.max}$ is 12.5 μs at low−line and 5 μs at high−line in A version and G_0 is static gain.

The output to control transfer function is obtained by FB resistive network ratio, OTA transconductance and VCTRL compensation network as below:

$$v_{ctrl} = i_{ctrl} \cdot z_{ctrl}(s) \quad \text{(eq. 38)}$$

where i_{ctrl} is OTA output current and $z_{ctrl(s)}$ is VCTRL compensation circuit impedance.

The OTA output current is defined by:

$$i_{ctrl} = \left(V_{REF} - v_{FB}\right) \cdot G_{EA} = \left(V_{REF} - \frac{V_{Ref}}{V_{out}} \cdot v_{out}\right) \cdot G_{EA} \quad \text{(eq. 39)}$$

where G_{EA} is OTA transconductance gain and V_{out} is DC output voltage.

Using equation 38 and equation 39, the output to control transfer function is obtained by:

$$\frac{\delta v_{ctrl}(s)}{\delta v_{out}(s)} = -\frac{V_{REF}}{V_{out}} \cdot G_{EA} \cdot z_{ctrl}(s) \approx -\frac{1}{s \cdot R_0 \cdot C_Z} \cdot \frac{1 + s \cdot R_Z \cdot C_Z}{1 + s \cdot R_Z \cdot C_P} \quad \text{(eq. 40)}$$

where $R_0 = V_{out} / (V_{REF} \cdot G_{EA})$ and the compensation network circuits are C_Z, R_Z and C_P (<< C_Z) as shown in Figure 2.

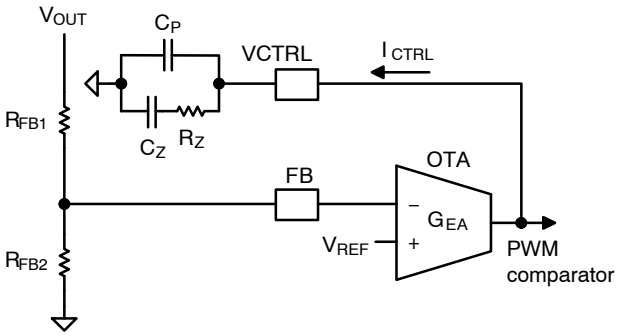

Figure 2. FB and VCTRL Circuit

Pole in equation 37 and zero in equation 40 are closely located and cross−over frequency, f_C, is placed between zero and second pole in equation 40. Phase margin, ϕ_m (in radians), is adjusted by C_P. From this, we obtain following equations:

- Feedback zero capacitor, C_Z:

$$C_Z = \frac{G_0}{2\pi f_C \cdot R_0} \quad \text{(eq. 41)}$$

- Feedback zero resistor, R_Z:

$$R_Z = \frac{R_{load} \cdot C_{BULK}}{2 \cdot C_Z} \quad \text{(eq. 42)}$$

- Feedback pole capacitor, C_P:

$$C_P = \frac{\tan\left(\frac{\pi}{2} - \phi_m\right)}{2\pi f_C \cdot R_Z} \quad \text{(eq. 43)}$$

Load resistance, R_{load} is calculated by:

$$R_{load} = \frac{V_{out,nom}^{\,2}}{P_{out,max}} = \frac{390\ V^2}{100\ W} = 1.52\ k\Omega \quad \text{(eq. 44)}$$

The cross−over frequency, f_C, should be higher than PFC boost stage pole, f_P:

$$f_P = \frac{1}{\pi \cdot R_{load} \cdot C_{BULK}} = \frac{1}{\pi \cdot 1.52\ k\Omega \cdot 68\ \mu F} = 3.1\ Hz \quad \text{(eq. 45)}$$

The condition of the highest cross−over frequency is the worst case of the phase margin where the line voltage is high to widen the bandwidth of the control to output transfer function. If we target a 25−Hz crossover frequency and a 60−degree phase margin (π/3 in radians) in our application, we have:

$$R_0 = \frac{390\ V}{2.5\ V \cdot 20\ \mu S} = 780\ k\Omega$$

$$G_0 = \frac{264\ V^2 \cdot 5\ \mu s \cdot 1.52\ k\Omega}{16 \cdot 200\ \mu H \cdot 390\ V} = 424$$

$$C_Z = \frac{424}{2\pi \cdot 25\ Hz \cdot 780\ k\Omega} = 3.46\ \mu F \approx 3.3\ \mu F$$

$$R_Z = \frac{1.52\ k\Omega \cdot 68\ \mu F}{2 \cdot 3.3\ \mu F} = 15.6\ k\Omega \approx 15\ k\Omega$$

$$C_P = \frac{\tan\left(\frac{\pi}{2} - \frac{\pi}{3}\right)}{2\pi \cdot 25\ Hz \cdot 15\ k\Omega} = 245\ nF \approx 220\ pF \quad \text{(eq. 46)}$$

CS/ZCD Pin Circuit

The circuit detects an over−current situation if the voltage across the current sense resistor exceeds 0.5 V. Hence:

$$R_{SENSE} = \frac{0.5\ V}{\left(I_{L,pk}\right)_{max}} \quad \text{(eq. 47)}$$

Combining the result in equation 6 leads to:

$$R_{SENSE} = \frac{0.5\ V}{3.3\ A} = 0.15\ \Omega \quad \text{(eq. 48)}$$

In our practical case, 0.12 Ω resistor is selected to have a bit of margin. R_{SENSE} losses can be computed using equation 10 giving the MOSFET conduction losses where R_{SENSE} replaces $R_{DS(on)}$:

$$\left(P_{RSENSE}\right)_{max} = \frac{4}{3} \cdot R_{SENSE} \cdot \left(\frac{P_{out,max}}{\eta \cdot \left(V_{line,rms}\right)_{LL}}\right)^2 \cdot \left(1 - \frac{8\sqrt{2} \cdot \left(V_{line,rms}\right)_{LL}}{3\pi \cdot V_{out,LL}}\right) \quad \text{(eq. 49)}$$

Hence, our 0.12 Ω current sense resistor will dissipate about 124 mW at full load, low line.

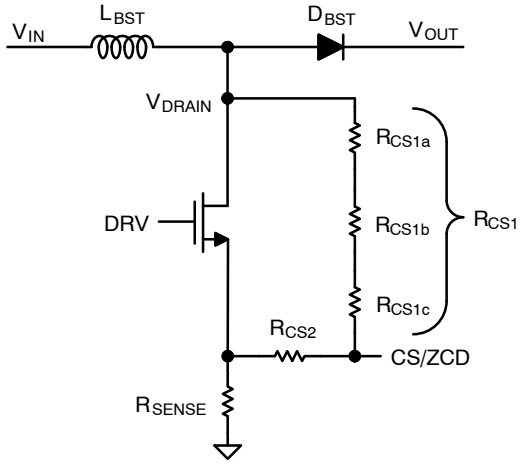

Figure 3. Drain Sensing for ZCD

The drain sensing based ZCD circuitry is shown in Figure 3. Drain voltage is sensed by CS resistor network and scaled down by K_{CS}:

$$K_{CS} = \frac{R_{CS1} + R_{CS2}}{R_{CS2}} \quad \text{(eq. 50)}$$

where K_{CS} is 133 and R_{CS2} is 62 kΩ in general.

The values of R_{CS1} and R_{CS2} must be chosen high for not consuming too much power during standby. During standby, there is no switching and the voltage seen by R_{CS1} in series with R_{CS2} is a constant voltage equal to $V_{mains,rms} \cdot \sqrt{2}$. The power consumed during standby is given by:

$$P_{CS,STBY} = \frac{\left(V_{mains,rms} \cdot \sqrt{2}\right)^2}{R_{CS1} + R_{CS2}} \quad \text{(eq. 51)}$$

The NCP1623 integrates leading edge blanking on the CS/ZCD pin that prevents the need for a filtering capacitor. No capacitor is allowed in the CS/ZCD circuitry as this will result in distorting the CS/ZCD signal leading to wrong or no ZCD detection. Care must be taken when probing the CS/ZCD signal with a scope probe as the scope probe will add typically a 10−pF capacitance.

In a boost converter, the averaged drain voltage which is one pin of the boost inductor is equal to the Vin voltage which is on the other pin of the boost inductor and this is because the average voltage drop across the inductor is zero volts in volt−sec balance if we neglect the series resistance of the inductor. Therefore, $V_{CS/ZCD}$ is averaged to obtain the input voltage information.

The averaged $V_{CS/ZCD}$, V_{SNS}, is used for ZCD, line detection, OVP2 (C version only) and brown−out (disabled in A and C version) in our application as below:

- Line range detection threshold:

$$\left(V_{line,rms}\right)_{HL} = \frac{K_{CS} \cdot V_{CS/ZDC(HL)}}{\sqrt{2}} = \frac{133 \cdot 1.8\ V}{\sqrt{2}} = 169\ V \quad \text{(eq. 52)}$$

$$\left(V_{line,rms}\right)_{LL} = \frac{K_{CS} \cdot V_{CS/ZDC(LL)}}{\sqrt{2}} = \frac{133 \cdot 1.55\ V}{\sqrt{2}} = 146\ V \quad \text{(eq. 53)}$$

- OVP2 threshold (C version only):

$$V_{OUT(OVP2)} = K_{CS} \cdot V_{ZCD(OVP2-EN)} = 133 \cdot 3.77\ V = 501\ V \quad \text{(eq. 54)}$$

- Brown−out threshold (Disabled in A and C version):

$$\left(V_{line,rms}\right)_{BO-EN} = \frac{K_{CS} \cdot V_{CS/ZCD(BO-EN)}}{\sqrt{2}} = \frac{133 \cdot 0.79\ V}{\sqrt{2}} = 74\ V \quad \text{(eq. 55)}$$

$$\left(V_{line,rms}\right)_{BO-EX} = \frac{K_{CS} \cdot V_{CS/ZCD(BO-EX)}}{\sqrt{2}} = \frac{133 \cdot 0.94\ V}{\sqrt{2}} = 88\ V \quad \text{(eq. 56)}$$

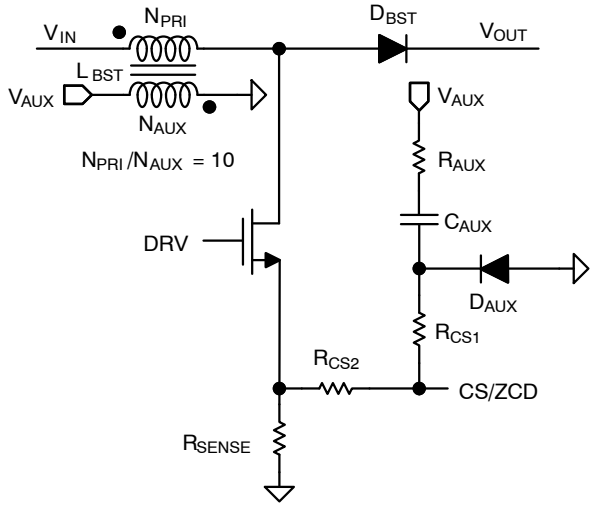

Figure 4. Aux. Winding Sensing for ZCD

It is possible to use the schematic shown in Figure 4 to generate the signal of CS/ZCD pin. Thanks to the auxiliary winding voltage capacitor C_{AUX}, R_{AUX} and D_{AUX}, it is possible to generate at the cathode of D_{AUX} a voltage equal to the power MOSFET drain voltage multiplied by the auxiliary (N_{AUX}) to primary (N_{PRI}) transformer turns ratio. The parameter K_{CS} previously described is now defined by:

$$K_{CS} = \frac{N_{PRI}}{N_{AUX}} \cdot \frac{R_{CS1} + R_{CS2}}{R_{CS2}} \quad \text{(eq. 57)}$$

where K_{CS} is 133, N_{PRI}/N_{AUX} is 10 and R_{CS2} is 22 kΩ in general.

With this approach, a lower voltage is carried and also low R_{CS1} values reduce the sensitivity to parasitic capacitors.

Another benefit of this circuitry is that there is no current consumption during standby (No switching activity hence no Vaux voltage).

It has to be mentioned that product version with brown−out feature activated will not operate with this circuitry. Everything else will work exactly the same as already described when the power MOSFET drain voltage is used for ZCD.

CSZCD Resistor Design Guideline

When the R_{CS} resistor bridge totals a resistance in the MΩ range at drain sensing circuit like Figure 3, it is very sensitive to parasitic capacitances as low as few hundreds of fF. Parasitic capacitances can be made from R_{CS} resistors nodes to GND or power MOSFET drain. These parasitic capacitances effect can lead to permanent false fault detection events: OCP, OVS or OVP2 triggering, making the controller unable to operate properly.

One easy way to avoid the effect of parasitic capacitors is to reduce the value of the resistors, while keeping the dividing ratio K_{CS} around 133. Reducing the CS/ZCD bridge resistors value ($R_{CS1} + R_{CS2}$) is at the expense of high standby power consumption.

If the $R_{CS1a} + R_{CS1b} + R_{CS1c}$ in Figure 3 should be above 5 MΩ, it is advised to have one 500−V SMD high−value resistor on the drain side (e.g. R_{CS1a} = 5.1 MΩ) with two low value (e.g. $R_{CS1b} = R_{CS1c}$ = 240 kΩ) 200−V SMD resistors in series. This is to avoid inter−resistor capacitance to GND to have difficulties to be discharged before the FET turn−on cycle. Experience shows that it is not recommended to use 3 equal value resistors to balance the drain voltage.

Bench experiments have proven SMD1206 & 0805 superiority, parasitic capacitance wise, over trough hole resistors.

R_{CS1} and R_{CS2} must be placed as close as possible to CS/ZCD pin. PCB traces connecting the R_{CS} resistors must be kept as short as possible, the width of the trace being as small as possible (minimum parasitic capacitance). It is wise to keep a safety distance of 1 cm between R_{CS} resistors and DRV, V_{IN}, V_{DRAIN} copper traces to avoid coupling.

Layout and Noise Immunity Considerations

The NCP1623 is not particularly sensitive to noise.

However, usual layout rules for power supply design apply. Among them, let us remind the following ones:

- The loop area of the power train must be minimized.
- Star configuration for the power ground that provide the current return path.
- Star configuration for the circuit ground.
- The circuit ground and the power ground should be connected by one single path, no loop is allowed.
- This path should preferably connect the circuit ground to the power ground at a place that is very near the grounded terminal of the current sense resistor (R_{SENSE}).
- A 100 or 220−nF capacitor should be placed between the circuit VCC and GND pins, with minimized connection length.
- R_{CS} resistors must be placed as close as possible to the CS/ZCD pin, and capacitance coupling with GND or any other signal must be avoided.
- It is recommended to place a filtering capacitor on the FB pin to protect the pin from possible surrounding noise. It must be small however not to distort the voltage sensed by the FB pin.

SUMMARY

Table 1. MAIN EQUATIONS

Step	Components	Formula	Comments
Step 1: Key Specifications	f_{line}: Line frequency. It is generally specified in a range of 47 – 63 Hz for 50 Hz/60 Hz applications. $\left(V_{line,rms}\right)_{HL}$: Lowest Level of the line voltage, e.g., 90 V. $\left(V_{line,rms}\right)_{LL}$: Level for the line voltage, e.g., 264 V. $V_{out,nom}$: Nominal Output Voltage at high−line, e.g., 390 V. $V_{out,LL}$: Output voltage at low−line (by follower boost) , e.g., 250 V. $\left(\delta V_{out}\right)_{pk-pk}$: Peak−to−Peak output voltage ripple in the line frequency $t_{HOLD-UP}$: Hold−up Time that is the amount of time the output will remain valid during line drop−out, e.g., 10 ms. $V_{out,min}$: Minimum output voltage allowing for operation of the downstream converter, e.g., 180 V. $P_{out,max}$: Maximum output power consumed by the PFC load, e.g., 100 W. η: System efficiency, e.g., 95%. $\left(P_{in,avg}\right)_{max}$: Maximum input power from the mains line at full load and low−line, e.g., 105 W assuming η = 95%.		
Step 2: Power Stage Design	PFC Inductor	$L \le \frac{\left(V_{line,rms}\right)_{LL}^{2}}{2 \cdot \left(P_{in,avg}\right)_{max}} \cdot T_{on,max}$	Maximum inductance $T_{on,max}$: max turn−on time
		$\left(I_{L,pk}\right)_{max} = 2\sqrt{2}\frac{\left(P_{in,avg}\right)_{max}}{\left(V_{line,rms}\right)_{LL}}$	Maximum peak current
		$\left(I_{L,rms}\right)_{max} = 2\sqrt{2}\frac{\left(I_{L,pk}\right)_{max}}{\sqrt{6}}$	Maximum rms current
	Bridge Diode	$\left(P_{bridge}\right)_{max} \approx \frac{1.8 \cdot V_f \cdot P_{out,max}}{\left(V_{line,rms}\right)_{LL} \cdot \eta}$	Maximum power loss V_f: bridge diode forward voltage
	MOSFET	$(P_{on})_{max} = \frac{4}{3} \cdot R_{DS(on)} \cdot \left(\frac{P_{out,max}}{\eta \cdot \left(V_{line,rms}\right)_{LL}}\right)^{2} \cdot \left(1 - \frac{8\sqrt{2} \cdot \left(V_{line,rms}\right)_{LL}}{3\pi \cdot V_{out,LL}}\right)$	Maximum conduction loss $R_{DS(on)}$: FET on−state resistance
	Boost Diode	$\left(P_{diode}\right)_{max} = V_f \cdot \frac{P_{out,max}}{V_{out,LL}}$	Maximum conduction loss
	Bulk Capacitor	$C_{BULK} \ge \frac{P_{out,max}}{\left(\delta V_{out}\right)_{pk-pk} \cdot \omega \cdot V_{out,LL}}$	Minimum capacitance to meet output ripple spec
		$C_{BULK} \ge \frac{2 \cdot P_{out,max} \cdot t_{HOLD-UP}}{V_{out,LL}^{2} - V_{out,min}^{2}}$	Minimum capacitance to meet hold−up time spec
		$\left(I_{c,rms}\right)_{max} \cong \sqrt{\frac{32\sqrt{2}}{9\pi} \cdot \frac{\left(P_{in,avg}\right)_{max}^{2}}{\left(V_{line,rms}\right)_{LL} \cdot V_{out,LL}} - \left(\frac{P_{out,max}}{V_{out,LL}}\right)^{2}}$	Maximum rms current

Table 1. MAIN EQUATIONS (continued)

Step	Components	Formula	Comments
Step 3: IC Control Circuit Design	FB Pin Circuit	$R_{FB1} = \frac{V_{out,nom} - V_{out,LL}}{I_{FB(LL)}}$	FB1 resistor $I_{FB(LL)}$: Follower boost FB current
		$R_{FB2} = \frac{R_{FB1} \cdot V_{REF}}{V_{out,nom} - V_{REF}}$	FB2 resistor V_{REF}: FB reference voltage, 2.5 V.
		$C_{FB} \leq \frac{1}{150 \cdot (R_{FB1} \parallel R_{FB2}) \cdot f_{line}}$	Maximum FB capacitor
	VCTRL Pin Circuit	$R_0 = \frac{V_{out,nom}}{V_{REF} \cdot G_{EA}}$	$v_{out}t/i_{ctrl}$ resistance i_{CTRL}: OTA output current G_{EA}: OTA gain
		$R_{load} = \frac{V_{out,nom}^2}{P_{out,max}}$	Load resistance at full load and high−line
		$G_0 = \frac{(V_{line,rms})_{HL}^2 \cdot T_{on.max} \cdot R_{load}}{16 \cdot L \cdot V_{out}}$	DC gain in the control to output transfer function
		$C_Z = \frac{G_0}{2\pi f_C \cdot R_0}$	Zero capacitor f_C: cross−over frequency
		$R_Z = \frac{R_{load} \cdot C_{BULK}}{2 \cdot C_Z}$	Zero resistor
		$C_P = \frac{\tan\left(\frac{\pi}{2} - \phi_m\right)}{2\pi f_C \cdot R_Z}$	Pole capacitor ϕ_m: phase margin in radians
	CS/ZCD Pin Circuit	$R_{SENSE} = \frac{0.5\ V}{(I_{L,pk})_{max}}$	Sensing resistor
		$(P_{RSENSE})_{max} = \frac{4}{3} \cdot R_{SENSE} \cdot \left(\frac{P_{out,max}}{\eta \cdot (V_{line,rms})_{LL}}\right)^2 \cdot \left(1 - \frac{8\sqrt{2} \cdot (V_{line,rms})_{LL}}{3\pi \cdot V_{out,LL}}\right)$	Maximum conduction loss
		$K_{CS} = \frac{N_{PRI}}{N_{AUX}} \cdot \frac{R_{CS1} + R_{CS2}}{R_{CS2}} = 133$	CS resistor ratio N_{PRI}/N_{AUX} = 1 (Figure 3), 10 (Figure 4) R_{CS2} = 62 kΩ (Figure 3), 22 kΩ (Figure 4)
		$R_{CS1} = R_{CS2} \cdot \left(133 \cdot \frac{N_{AUX}}{N_{PRI}} - 1\right)$	CS1 resistor N_{PRI}/N_{AUX} = 1 (Figure 3), 10 (Figure 4) R_{CS2} = 62 kΩ (Figure 3), 22 kΩ (Figure 4)

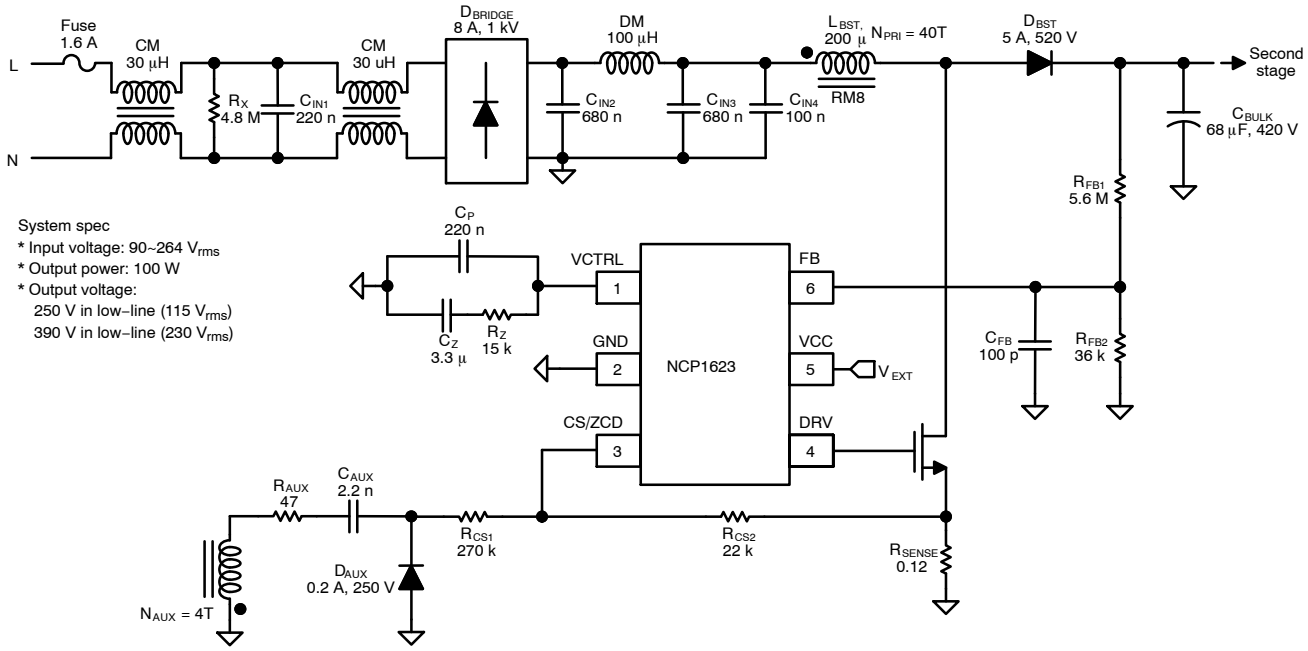

Figure 5. System Schematic of 100 W Design

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