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Application Note AN-8033

Design Guideline for Primary Side Regulated (PSR) Flyback Converter Using FAN103 and FSEZ13X7

1. Introduction

More than half of the external power supplies are used for portable electronics such as laptops, cellular phones, and MP3 players and; therefore, have output voltage and output current regulation capabilities for battery charging. In applications where precise output current regulation is required, current sensing in the secondary side is always necessary, which results in additional sensing loss. For power supply designers struggling in an environment of increasing regulatory pressures, the output current sensing is a daunting design challenge.

Primary-side regulation (PSR) for power supplies can be an optimal solution for alleviating the burden of achieving international energy efficiency regulations (California Energy Commission (CEC) and Energy Star) in charger designs. The primary-side regulation controls the output voltage and current precisely with the information in the primary side of the power supply only, not only removing the output current sensing loss, but also eliminating all secondary-feedback circuitry. This facilitates a higher efficiency power supply design without incurring

tremendous costs. Fairchild Semiconductor PWM PSR controller FAN103 and Fairchild Power Switch (FPS) (MOSFET + Controller, EZ-PSR) FSEZ13X7 significantly simplify the challenge of meeting tighter efficiency requirements while eliminating external components. FAN103 and FSEZ13x7 also have an integrated output cable voltage drop compensation and external component temperature variation compensation circuit, which allows high accuracy even at the end of the output cable for charger applications.

This application note presents practical design considerations for battery chargers employing Fairchild Semiconductor PWM PSR controller FAN103 and Power Switch (MOSFET + Controller, EZ-PSR) FSEZ13X7. It includes designing the transformer and output filter, selecting the components, and implementing constant-current / constant-voltage control. The step-by-step design procedure described helps engineers design a power supply more easily. The design procedure is verified through an experimental prototype converter using FSEZ1317. Figure 1 shows the typical application circuit of primary-side controlled flyback converter using FSEZ1317.
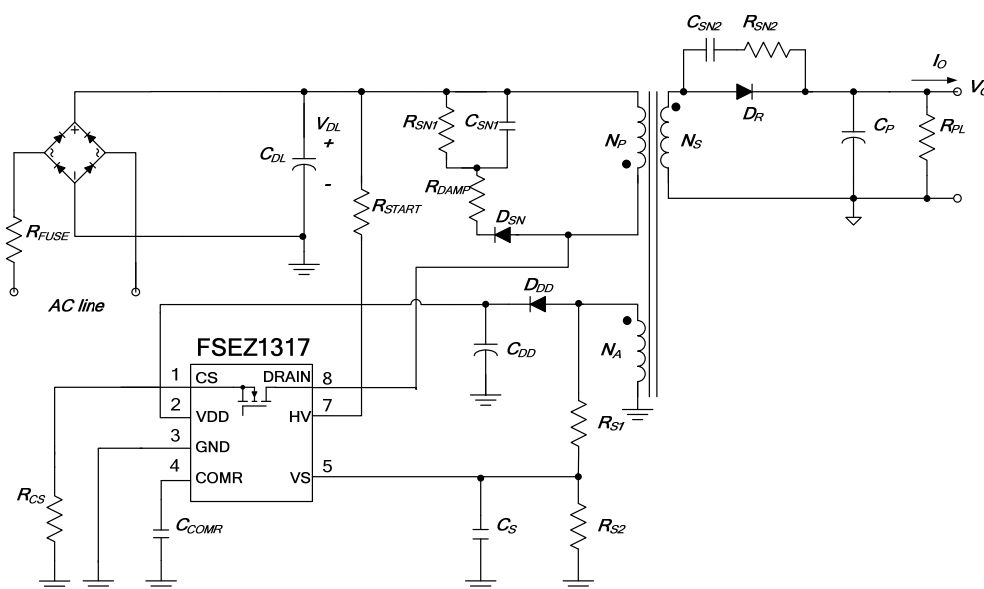

Figure 1. Typical Application Circuit of FSEZ1317

2. Operation Principle of Primary-Side Regulation

Figure 2 shows the simplified circuit diagram of a primary-side regulated flyback converter and its typical waveforms are shown in Figure 3. Generally, discontinuous conduction mode (DCM) operation is preferred for primary-side regulation since it allows better output regulation. The key of primary-side regulation is how to obtain output voltage and current information without directly sensing them. Once these values are obtained, the control can be accomplished by the conventional feedback compensation method.

The operation principles of DCM flyback converter are as follows:

- During the MOSFET ON time (t_{ON}), input voltage (V_{DL}) is applied across the primary-side inductor (L_m). Then, MOSFET current (I_{ds}) increases linearly from zero to the peak value (I_{pk}). During this time, the energy is drawn from the input and stored in the inductor.

- When the MOSFET is turned off, the energy stored in the inductor forces the rectifier diode (D) to be turned on. During the diode conduction time (t_D), the output voltage (V_o), together with diode forward-voltage drop (V_F), are applied across the secondary-side inductor ($L_m \times N_s^2 / N_p^2$) and the diode current (I_D) decreases linearly from the peak value ($I_{pk} \times N_p/N_s$) to zero. At the end of t_D, all the energy stored in the inductor has been delivered to the output.

- When the diode current reaches zero, the transformer auxiliary winding voltage (V_w) begins to oscillate by the resonance between the primary-side inductor (L_m) and the MOSFET output capacitor.

During the diode conduction time, the sum of output voltage and diode forward-voltage drop is reflected to the auxiliary winding side as $(V_o+V_F) \times N_a/N_s$. Since the diode forward-voltage drop decreases as current decreases, the auxiliary winding voltage reflects the output voltage best at the end of diode conduction time where the diode current diminishes to zero. By sampling the winding voltage at the end of the diode conduction time, the output voltage information can be obtained. The internal error amplifier for output voltage regulation (EA_V) compares the sampled voltage with internal precise reference to generate an error voltage (V_{COMV}), which determines the duty cycle of the MOSFET, as shown in Figure 2.

Meanwhile, the output current can be estimated through calculation. Assuming that output current is same as the average of the diode current in steady state, the output current can be estimated as:

$$I_O = I_{PK} \frac{N_P}{N_S} \bullet \frac{t_D}{2t_S} \qquad (1)$$

The output current estimator picks up the peak value of the drain current with a peak detection circuit and calculates the output current using the diode conduction time (t_D) and switching period (t_s). These output information is compared with internal precise reference to generate error voltage (V_{COMI}), which determines the duty cycle of the MOSFET, as shown in the block diagram of Figure 2.

Among the two error voltages, V_{COMV} and V_{COMI}, the smaller one actually determines the duty cycle. Therefore, during constant voltage regulation mode, V_{COMV} determines the duty cycle while V_{COMI} is saturated to HIGH. During constant current regulation mode, V_{COMI} determines the duty cycle while V_{COMV} is saturated to HIGH.
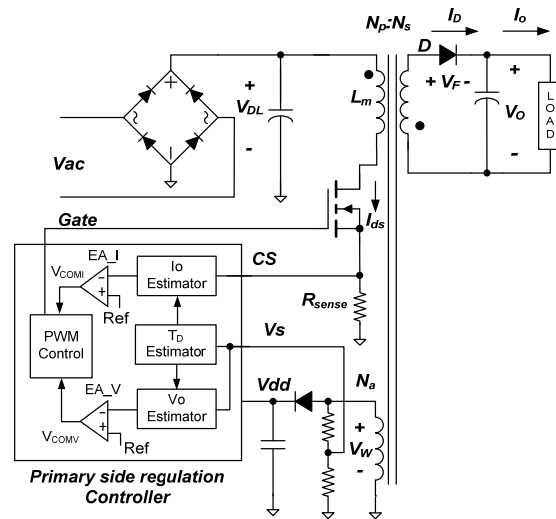
Figure 2.   Primary-Side Regulated Flyback Converter
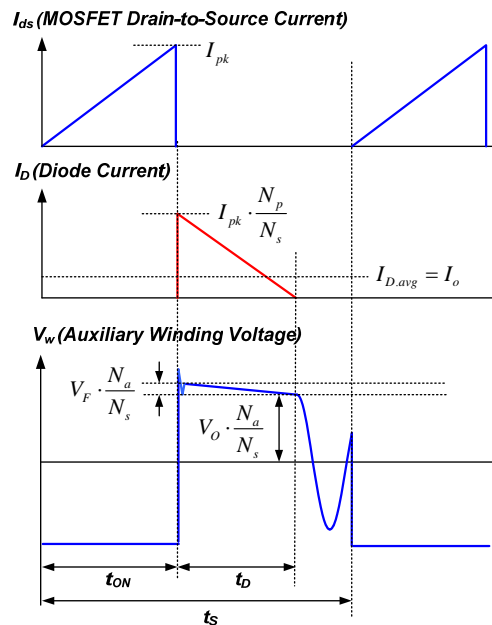
Figure 3. Key Waveforms of Primary-Side Regulated Flyback Converter

3. Design Consideration

Converters with Constant Current (CC) output require more design consideration than the conventional power supply design with a fixed output voltage. In CC operation, the voltage for control IC (V_{DD}), which is usually obtained with an auxiliary winding of the transformer, changes with the output voltage. Thus, the V_{DD} operation range determines the constant current control range. FAN103 and FSEZ13X7 have a wide supply voltage (V_{DD}) operation range from 5V up to 24V, which allows stable CC regulation even with output voltage lower than a quarter of its nominal value.

Another important design consideration for CC operation is that the transformer should be designed to guarantee DCM operation in all operation range since the output information is properly obtained only in DCM operation, as described in Section 2. As seen in Figure 4, the MOSFET conduction time (t_{ON}) decreases as output voltage decreases in CC mode. Meanwhile, the diode conduction time (t_D) increases as the output voltage decreases. Since the increase of t_{ON} is dominant to the decrease of t_{ON} in determining the sum of t_{ON} and t_D, the converter tends to enter CCM as output voltage decreases.

FAN103 and FSEZ13X7 have a frequency reduction function to prevent CCM operation by extending the switching period, which is activated when the output voltage drops below 70% of its nominal value, as depicted in Figure 5. Therefore, 70% of output voltage and minimum output voltage are the two worst cases for the transformer design.

The transformer should be designed for DCM both at 70% of nominal output voltage and minimum output voltage. Once the converter is designed to operate in DCM at 70% of nominal output voltage and minimum output voltage, DCM operation is guaranteed for entire load range.

$$V_O^{CC} = V_O / k$$

$$T_{ON}^{CC} = T_{ON} / \sqrt{k}$$
$$T_D^{CC} = T_D \cdot k$$
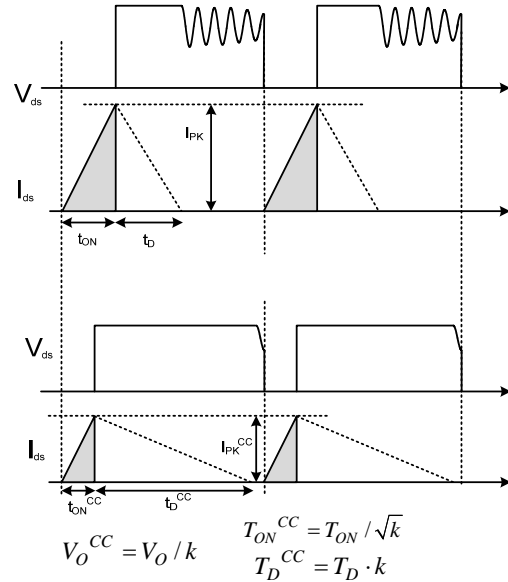
Figure 4. t_{ON} and t_D Change as Output Voltage Decreases
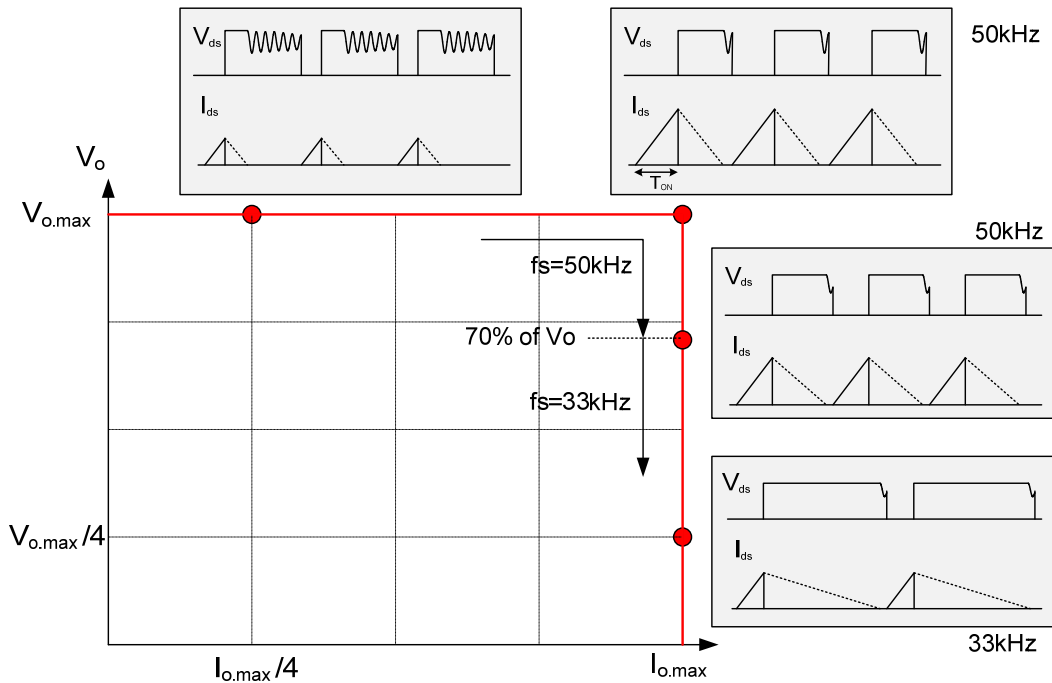
Figure 5.   Operation Range of Charger with CC/CV

4. Design Procedure

In this section, a design procedure is presented using the schematic of Figure 6 as a reference. An offline charger with 3.75W/5V output has been selected as a design example. The design specifications are as follows:

- Line voltage range: 90~264V_{AC} and 60Hz
- Nominal output voltage and current: 5V/0.75A
- Output voltage ripple: less than 150mV
- Minimum output voltage in CC mode: 25% of nominal output (1.25V)

Figure 6.   Output Voltage and Current Operating Area

[STEP-1] Estimate the Efficiencies

A charger application has output voltage and current that change over wide range as shown in Figure 6. To optimize the power stage design, the efficiencies and input powers should be specified for operating point A (nominal output voltage and current), B (70% of nominal output voltage), and C (minimum output voltage), respectively.
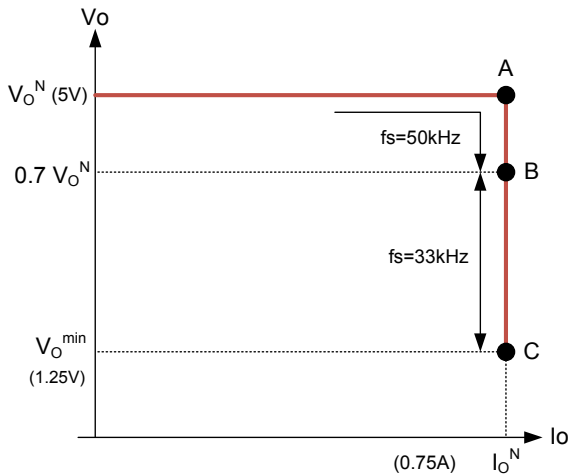
- Estimated overall efficiency (η) for operating points A, B, and C: The overall power conversion efficiency should be estimated to calculate the input power. If no reference data is available, use the typical efficiency in Table 1.

- Estimated primary-side efficiency (η_P) and secondary-side efficiency (η_S) for operating points A, B, and C. Figure 7 shows the definition of primary-side and secondary-side efficiencies, where the primary-side efficiency is for the power transfer from AC line input to the transformer primary side, while the secondary-side efficiency is for the power transfer from the transformer primary side to the power supply output.

    The typical values for the primary-side and secondary-side efficiencies are given as:

$$\eta_P \cong \eta^{\frac{1}{3}}, \eta_S \cong \eta^{\frac{2}{3}} \text{ : output voltage} < 10V \tag{2}$$

$$\eta_P \cong \eta^{\frac{2}{3}}, \eta_S \cong \eta^{\frac{1}{3}} \text{ : output voltage} > 10V \tag{3}$$

Table 1.Typical Efficiency of Flyback Converter

Output Voltage	Typical Efficiency for Universal Input	Typical Efficiency for European Input
3.3~6V	65~70%	67~72%
6~12V	70~77%	72~79%
12~24V	77~82%	79~84%
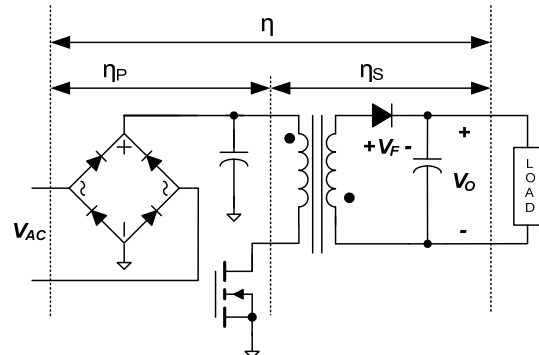
Figure 7.   Definition of Primary- and Secondary-Side Efficiency

With the estimated overall efficiency, the input power at nominal output is given as:

$$P_{IN} = \frac{V_O^N I_O^N}{\eta} \tag{4}$$

where V_O^N and I_O^N are the nominal output voltage and current, respectively.

Then, the input power of transformer at nominal output is given as:

$$P_{IN.T} = \frac{V_O^N I_O^N}{\eta_S} \tag{5}$$

As mentioned in previous section, when the output voltage drops below 70% of its nominal value, the frequency is reduced to 33kHz to prevent CCM operation. Thus, the transformer should be designed for DCM both at 70% of nominal output voltage and minimum output voltage.

As output voltage reduces in CC mode, the efficiency also drops. To optimize the transformer design, it is required to estimate the efficiencies properly at 70% of nominal output voltage and minimum output voltage conditions.

The overall efficiency at 70% of nominal output voltage (operating point B) can be approximated as:

$$\eta_{@B} \cong \eta \cdot \frac{0.7 \cdot V_O^N}{0.7 \cdot V_O^N + V_F} \cdot \frac{V_O^N + V_F}{V_O^N} \tag{6}$$

where V_F is diode forward-voltage drop.

The secondary-side efficiency at 70% of nominal output voltage (operating point B) can be approximated as:

$$\eta_{S@B} \cong \eta_S \cdot \frac{0.7 \cdot V_O^N}{0.7 \cdot V_O^N + V_F} \cdot \frac{V_O^N + V_F}{V_O^N} \tag{7}$$

Then, the power supply input power and transformer input power at 70% nominal output voltage (operating point B) are given as:

$$P_{IN@B} = \frac{0.7 \cdot V_O{}^N \cdot I_O{}^N}{\eta_{@B}} \tag{8}$$

$$P_{IN.T@B} = \frac{0.7 \cdot V_O{}^N \cdot I_O{}^N}{\eta_{S@B}} \tag{9}$$

The overall efficiency at the minimum output voltage (operating point C) can be approximated as:

$$\eta_{@C} \cong \eta \cdot \frac{V_O{}^{min}}{V_O{}^{min} + V_F} \cdot \frac{V_O{}^N + V_F}{V_O{}^N} \tag{10}$$

where $V_O{}^{min}$ is the minimum output voltage.

The secondary-side efficiency at minimum output voltage (operating point C) can be approximated as:

$$\eta_{S@C} \cong \eta_S \cdot \frac{V_O{}^{min}}{V_O{}^{min} + V_F} \cdot \frac{V_O{}^N + V_F}{V_O{}^N} \tag{11}$$

Then, the power supply input power and transformer input power at the minimum output voltage (operating point C) are given as:

$$P_{IN@C} = \frac{V_O{}^{min} \cdot I_O{}^N}{\eta_{@C}} \tag{12}$$

$$P_{IN.T@C} = \frac{V_O{}^{min} \cdot I_O{}^N}{\eta_{S@C}} \tag{13}$$

(Design Example)

Assuming the overall efficiency is 70% at operating point A (nominal output voltage and current), the secondary-side efficiency is obtained as:

$$\eta_S \cong \eta^{\frac{2}{3}} = 0.7^{\frac{2}{3}} = 0.788$$

Then, the input powers of the power supply and transformer are obtained as:

$$P_{IN} = \frac{V_O{}^N I_O{}^N}{\eta} = \frac{3.75}{0.7} = 5.36W$$

$$P_{IN.T} = \frac{P_{OUT}}{\eta_S} = \frac{3.75}{0.7^{2/3}} = 4.76W$$

The efficiencies at 70% of nominal output voltage are:

$$\eta_{@B} \cong \eta \cdot \frac{0.7 \cdot V_O{}^N}{0.7 \cdot V_O{}^N + V_F} \cdot \frac{V_O{}^N + V_F}{V_O{}^N} = 0.67$$

$$\eta_{S@B} \cong \eta_S \cdot \frac{0.7 \cdot V_O{}^N}{0.7 \cdot V_O{}^N + V_F} \cdot \frac{V_O{}^N + V_F}{V_O{}^N} = 0.756$$

Then, the input powers of the power supply and transformer at 70% of nominal output voltage are obtained as:

$$P_{IN@B} = \frac{0.7 \cdot V_O{}^N I_O{}^N}{\eta_{@B}} = 3.91W$$

$$P_{IN.T@B} = \frac{0.7 \cdot V_O{}^N I_O{}^N}{\eta_{S@B}} = 3.47W$$

The efficiencies at the minimum output voltage are:

$$\eta_{@C} \cong \eta \cdot \frac{V_O{}^{min}}{V_O{}^{min} + V_F} \cdot \frac{V_O{}^N + V_F}{V_O{}^N} = 0.540$$

$$\eta_{S@C} \cong \eta_S \cdot \frac{V_O{}^{min}}{V_O{}^{min} + V_F} \cdot \frac{V_O{}^N + V_F}{V_O{}^N} = 0.608$$

The input powers of the power supply and transformer at the minimum output voltage are obtained as:

$$P_{IN@C} = \frac{V_O{}^{min} I_O{}^N}{\eta_{@C}} = 1.74W$$

$$P_{IN.T@C} = \frac{V_O{}^{min} I_O{}^N}{\eta_{S@C}} = 1.54W$$

[STEP-2] Determine the DC Link Capacitor (C_{DL}) and the DC Link Voltage Range

It is typical to select the DC link capacitor as 2-3µF per watt of input power for universal input range (90-265V_{RMS}) and 1µF per watt of input power for European input range (195V~265V_{RMS}). With the DC link capacitor chosen, the minimum DC link voltage is obtained as:

$$V_{DL}{}^{min} = \sqrt{2 \cdot (V_{LINE}{}^{min})^2 - \frac{P_{IN}(1 - D_{ch})}{C_{DL} \cdot f_L}} \tag{14}$$

where $V_{LINE}{}^{min}$ is the minimum line voltage, C_{DL} is the DC link capacitor, f_L is the line frequency, and D_{ch} is the DC link capacitor charging duty ratio defined as shown in Figure 8, which is typically about 0.2.

The maximum DC link voltage is given as:

$$V_{DL}{}^{max} = \sqrt{2} \cdot V_{LINE}{}^{max} \tag{15}$$

where $V_{LINE}{}^{max}$ is the maximum line voltage.

The minimum input DC link voltage at 70% nominal output voltage are given as:

$$V_{DL@B}{}^{min} = \sqrt{2 \cdot (V_{LINE}{}^{min})^2 - \frac{P_{IN@B}(1 - D_{ch})}{C_{DL} \cdot f_L}} \tag{16}$$

The minimum input DC link voltage at minimum output voltage are given as:

$$V_{DL@C}{}^{min} = \sqrt{2 \cdot (V_{LINE}{}^{min})^2 - \frac{P_{IN@C}(1 - D_{ch})}{C_{DL} \cdot f_L}} \tag{17}$$
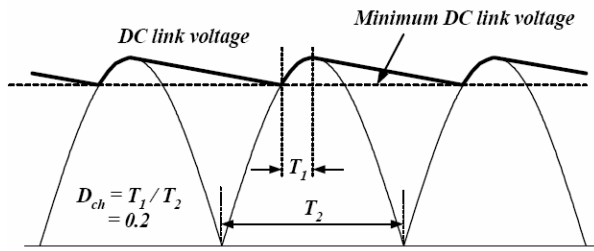
Figure 8. DC Link Voltage Waveforms

(Design Example) By choosing two 4.7μF capacitors in parallel for the DC link capacitor, the minimum and maximum DC link voltage for each condition are obtained as:

$$V_{DL}{}^{min} = \sqrt{2 \cdot (V_{LINE}{}^{min})^2 - \frac{P_{IN}(1-D_{ch})}{C_{DL} \cdot f_L}}$$

$$= \sqrt{2 \cdot (90)^2 - \frac{5.36(1-0.2)}{2 \cdot 4.7 \times 10^{-6} \cdot 60}} = 93V$$

$$V_{in}{}^{max} = \sqrt{2} \cdot 264 = 373V$$

$$V_{DL@B}{}^{min} = \sqrt{2 \cdot (V_{LINE}{}^{min})^2 - \frac{P_{IN@B}(1-D_{ch})}{C_{DL} \cdot f_L}}$$

$$= \sqrt{2 \cdot (90)^2 - \frac{3.91(1-0.2)}{2 \cdot 4.7 \times 10^{-6} \cdot 60}} = 103V$$

$$V_{DL@C}{}^{min} = \sqrt{2 \cdot (V_{LINE}{}^{min})^2 - \frac{P_{IN@C}(1-D_{ch})}{C_{DL} \cdot f_L}}$$

$$= \sqrt{2 \cdot (90)^2 - \frac{1.74(1-0.2)}{2 \cdot 4.7 \times 10^{-6} \cdot 60}} = 117V$$

[STEP-3] Determine the Transformer Turns Ratio

Figure 9 shows the MOSFET drain-to-source voltage waveforms. When the MOSFET is turned off, the sum of the input voltage (V_{DL}) and the output voltage reflected to the primary is imposed across the MOSFET as:

$$V_{DS}{}^{nom} = V_{DL}{}^{max} + V_{RO} \tag{18}$$

where V_{RO} is reflected output voltage defined as:

$$V_{RO} = \frac{N_P}{N_s}(V_O + V_F) \tag{19}$$

where V_F is the diode forward voltage drop and N_P and N_S are number of turns for primary side and secondary side, respectively.

When the MOSFET is turned on, the output voltage, together with input voltage reflected to the secondary, are imposed across the diode as:

$$V_D{}^{nom} = \frac{N_S}{N_P}V_{DL}{}^{max} + V_O \tag{20}$$

As observed in Equations (6) and (7), increasing the transformer turns ratio (N_p/N_s) results in increased voltage of MOSFET, while it leads to reduced voltage stress of rectifier diode. Therefore, the transformer turns ratio (N_p/N_s) should be determined by the compromise between MOSFET and diode voltage stresses. When determining the transformer turns ratio, the voltage overshoot on drain voltage should be also considered. The maximum voltage stress of MOSFET is given as:

$$V_{DS}{}^{max} = V_{DL}{}^{max} + V_{RO} + V_{OS} \tag{21}$$

For reasonable snubber design, voltage overshoot (V_{OS}) is typically 1~1.5 times of the reflected output voltage. It is also typical to have a margin of 15~20% of breakdown voltage for maximum MOSFET voltage stress.
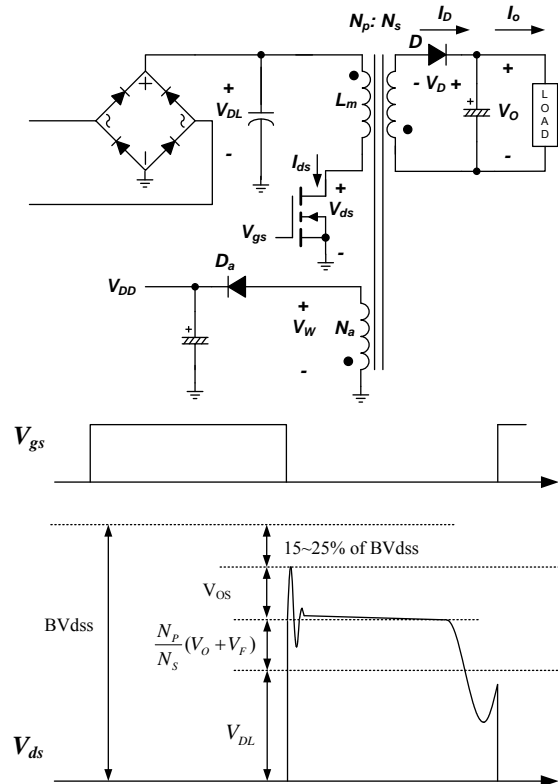

Figure 9. Transformer Turns Ratio and Voltage Stress on MOSFET and Diode

The transformer turns ratio between the auxiliary winding and secondary winding (N_a/N_s) should be determined by considering the permissible IC supply voltage (V_{DD}) range and minimum output voltage in CC mode. When the power supply operates in constant current (CC) mode, V_{DD} changes, together with the output voltage, as seen in Figure 10. The overshoot of auxiliary winding voltage caused by the leakage inductance also affects the V_{DD}. V_{DD} voltage at light-load condition, where the overshoot of auxiliary winding voltage is negligible, is given as:

$$V_{DD}^{min1} = \frac{N_a}{N_S}(V_o + V_F) - V_{Fa} \qquad (22)$$

The actual V_{DD} voltage at heavy load is higher than Equation (8) due to the overshoot by the leakage inductance, which is proportional to the voltage overshoot of MOSFET drain-to-source voltage shown in Figure 10. Considering the effect of voltage overshoot, the V_{DD} voltages for nominal output voltage and minimum output voltage are given as:

$$V_{DD}^{max} \cong \frac{N_a}{N_S}(V_O + V_F + \frac{N_S}{N_P}V_{OS}) - V_{Fa} \qquad (23)$$

$$V_{DD}^{min2} \cong \frac{N_a}{N_S}(V_O^{min} + V_F + \frac{N_S}{N_P}V_{OS}) - V_{Fa} \qquad (24)$$

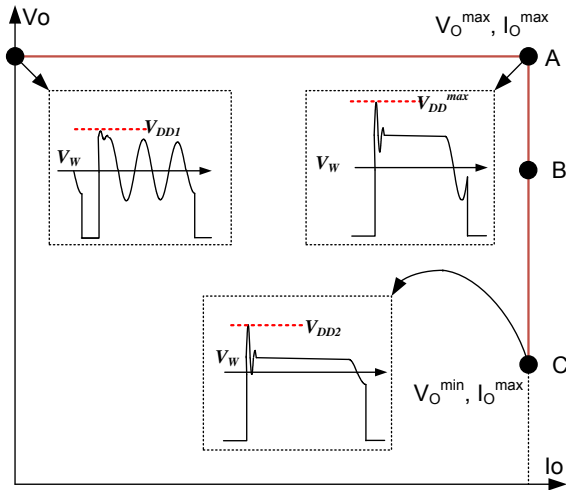where V_{Fa} is the diode forward-voltage drop of auxiliary winding diode.

Figure 10. V_{DD} and Winding Voltage

(Design Example) Assuming that drain voltage overshoot is same as the reflected output voltage, the maximum drain voltage is given as:

$$V_{DS}^{max} = V_{DL}^{max} + V_{RO} + V_{OS} = V_{DL}^{max} + 2V_{RO}$$

For 700V MOSFET with 25% margin, the reflected output voltage is obtained as:

$$V_{DS}^{max} = 0.75 \times 700 > 373 + 2V_{RO}$$

$$\therefore V_{RO} < 76V$$

Setting V_{RO}=72 and V_F=0.55, the turns ratio N_P/N_S is obtained as:

$$\frac{N_P}{N_S} = \frac{V_{RO}}{(V_o + V_F)} = \frac{72}{5.55} = 13$$

The allowable V_{DD} range is from 5.5 to 24V, considering the tolerance. Considering voltage ripple on V_{DD} caused by burst operation at no load condition, 3V margin is added for V_{DD} voltage calculation at no-load condition as:

$$V_{DD}^{min1} = \frac{N_a}{N_S}(5 + 0.55) - 0.7 > 5.5 + 3$$

$$\therefore \frac{N_a}{N_S} > 1.66$$

$$V_{DD}^{max} = \frac{N_a}{N_S}(5 + 0.55 + \frac{1}{13}72) - 0.7 < 24$$

$$\therefore \frac{N_a}{N_S} < 2.23$$

$$V_{DD}^{min2} = \frac{N_a}{N_S}(1.25 + 0.55 + \frac{1}{13}72) - 0.7 > 5.5$$

$$\therefore \frac{N_a}{N_S} > 0.84$$

To minimize the power consumption of PWM IC, it is required to keep V_{DD} as low as possible. Therefore, N_a/N_S is determined as 1.66.

[STEP-4] Design the Transformer

Figure 11 shows the definition of MOSFET conduction time (t_{ON}), diode conduction time (t_D) and non-conduction time (t_{OFF}). The sum of MOSFET conduction time and diode conduction time at 70% of nominal output voltage is obtained as:

$$T_{ON} + T_D = T_{ON}(1 + \frac{N_S}{N_P} \cdot \frac{V_{DL@B}^{min}}{0.7 \cdot V_O + V_F}) \qquad (25)$$

The first step to design the transformer is to determine how much non-conduction time (t_{OFF}) is allowed in DCM operation.

Once the t_{OFF} is determined by considering the frequency variation caused by frequency hopping and its own tolerance, the MOSFET conduction time is obtained as:

$$T_{ON@B} = \frac{1/f_S - T_{OFF}}{(1 + \frac{N_S}{N_P} \cdot \frac{V_{DL@B}^{min}}{0.7 \cdot V_O^N + V_F})} \qquad (26)$$
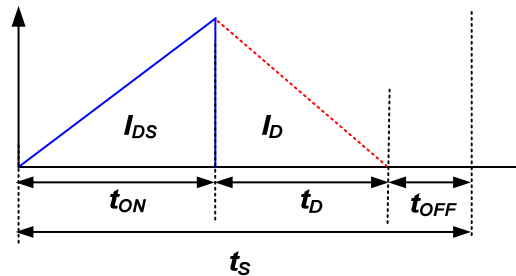

Figure 11. Definition of t_{ON}, t_D, and t_{OFF}

The transformer primary-side inductance can be calculated as:

$$L_m = \frac{(V_{DL@B}^{min} \cdot T_{ON@B})^2}{2P_{IN.T@B}} \cdot f_S \qquad (27)$$

The maximum peak drain current can be obtained at the nominal output condition as:

$$I_{DS}{}^{PK} = \sqrt{\frac{2P_{IN.T}}{L_m \cdot f_S}} \qquad (28)$$

The MOSFET conduction time at the nominal output condition is obtained as:

$$T_{ON} = I_{DS}{}^{PK} \frac{L_m}{V_{DL}{}^{min}} \qquad (29)$$

The minimum number of turns for the transformer primary side to avoid the core saturation is given by:

$$N_P{}^{min} = \frac{L_m I_{DS}{}^{PK}}{B_{sat} A_e} \qquad (30)$$

where A_e is the cross-sectional area of the core in m^2 and B_{sat} is the saturation flux density in Tesla. Figure 12 shows the typical characteristics of ferrite core from TDK (PC40). Since the saturation flux density (B_{sat}) decreases as the temperature rises, the high-temperature characteristics should be considered when it comes to charger in enclosed case. If there is no reference data, use B_{sat} =0.25~0.3 T. Table 2 shows the commonly used cores for battery chargers with output power under 10W. The cores recommended in Table 2 are typical for the universal input range and 50kHz switching frequency.

Once the turns ratio is obtained, determine the proper integer for N_s so that the resulting N_p is larger than $N_p{}^{min}$ obtained from Equation (30).
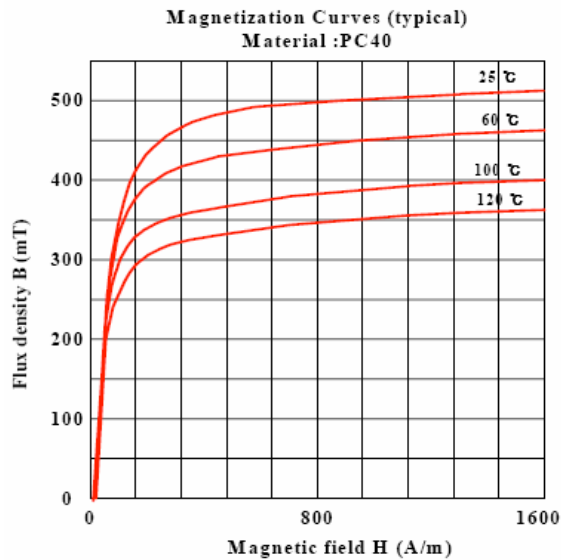

Figure 12. Typical B-H Curves of Ferrite Core (TDK/PC40)

DCM operation at minimum output voltage should be also checked. The MOSFET conduction time at minimum output voltage is given as:

$$T_{ON@C} = \frac{1}{V_{DL@C}{}^{min}} \sqrt{\frac{2P_{IN.T@C}L_m}{f_{SR}}} \qquad (31)$$

where f_{SR} is the reduced switching frequency to prevent CCM operation.

Then, the non-conduction time at minimum output voltage is given as:

$$T_{OFF@C} = \frac{1}{f_{SR}} - T_{ON@C}(1 + \frac{N_S}{N_P} \cdot \frac{V_{DL@C}{}^{min}}{V_O{}^{min} + V_F}) \qquad (33)$$

The non-conduction time should be larger than 3μs (10% of switching period), considering the tolerance of switching frequency.

Table 2. Typical Cores for Battery Charger Application (for Universal Input Range, DCM Operation, and fs=50kHz)

Core	Cross-sectional Area	Rated Input Power
EE13-Z	17.1mm^2	4~7W
EI16-Z	19.8mm^2	4~7W
EE16-Z	19.0mm^2	7~14W
EI19-Z	24.0mm^2	7~14W

(Design Example) Setting the non-conduction time at 70% of nominal output voltage as 4μs, the MOSFET conduction time is obtained as:

$$T_{ON@B} = \frac{1/f_S - T_{OFF}}{(1 + \frac{N_S}{N_P} \cdot \frac{V_{DL@B}{}^{min}}{0.7 \cdot V_O + V_F})} = 5.4 \mu s$$

The transformer primary-side inductance is calculated as:

$$L_m = \frac{(V_{DL@B}{}^{min} \cdot T_{ON@B})^2}{2P_{IN.T@B}} \cdot f_S = 2.24mH$$

Then, the peak drain current at maximum output power condition is given as:

$$I_{DS}{}^{PK} = \sqrt{\frac{2P_{IN.T}}{L_m \cdot f_S}} = 292mA$$

The MOSFET conduction time at the nominal output condition is obtained as:

$$T_{ON} = I_{DS}{}^{PK} \frac{L_m}{V_{DL}{}^{min}} = 0.292 \frac{2.24 \times 10^{-3}}{93} = 7.03 \mu s$$

EE16 core is selected for the transformer and the minimum number of turns for the transformer primary side to avoid the core saturation is given by:

$$N_P{}^{min} = \frac{L_m I_{ds}{}^{PK}}{B_{sat} A_e}$$

$$= \frac{2.24 \times 10^{-3} \cdot 0.292}{0.3 \cdot 19 \times 10^{-6}} = 114$$

Then, determine the proper integer for N_s so that the resulting N_p is larger than $N_p{}^{min}$

$$N_P = 13 \times N_S$$

$$= 13 \times 9 = 117 > N_P{}^{min}$$

The auxiliary winding turns, N_a is given as:

$$N_a = \frac{N_a}{N_S} \times N_S = 1.65 \times 9 = 15$$

The MOSFET conduction time at minimum output voltage is obtained as:

$$T_{ON@C} = \frac{1}{V_{DL@C}^{min}} \sqrt{\frac{2P_{IN.T@C}L_m}{f_{SR}}} = 3.9\mu s$$

The non-conduction time at minimum output voltage:

$$T_{OFF@C} = \frac{1}{f_{SR}} - T_{ON@C}(1 + \frac{N_S}{N_P} \cdot \frac{V_{DL@C}^{min}}{V_O^{min} + V_F})$$
$$= 6.82\mu s > 3\mu s$$

[STEP-5] Calculate the Voltage and Current of the Switching Devices

Primary-Side MOSFET: The voltage stress of the MOSFET was discussed when determining the transformer turns ratio in STEP-3. Assuming that drain voltage overshoot is the same as the reflected output voltage, the maximum drain voltage is given as:

$$V_{DS}^{max} = V_{DL}^{max} + V_{RO} + V_{OS} \qquad (33)$$

The rms current though the MOSFET is given as:

$$I_{DS}^{rms} = I_{DS}^{PK} \sqrt{\frac{T_{ON}f_s}{3}} \qquad (34)$$

Secondary-Side diode: The maximum reverse voltage and the rms current of the rectifier diode are obtained respectively, as:

$$V_D = V_O^N + \frac{N_S}{N_P}V_{DL}^{max} \qquad (35)$$

$$I_D^{rms} = I_{DS}^{rms} \sqrt{\frac{V_{DL}^{min}}{V_{RO}} \cdot \frac{N_P}{N_S}} \qquad (36)$$

(Design Example) Assuming voltage overshoot of drain-to-source is same as reflected output voltage, the maximum voltage across the MOSFET is calculated as
$$V_{ds}^{max} = V_{DL}^{max} + 2V_{RO} = 517V$$

The rms current though the MOSFET is

$$I_{DS}^{rms} = I_{DS}^{PK} \sqrt{\frac{T_{ON}f_s}{3}} = 0.1A$$

The diode voltage and current are obtained as

$$V_D = V_O + \frac{N_S}{N_P}V_{DL}^{max} = 5 + \frac{9}{117} \cdot 373 = 33.8V$$

$$I_D^{rms} = I_{DS}^{rms} \sqrt{\frac{V_{DL}^{min}}{V_{RO}} \cdot \frac{N_P}{N_S}} = 0.10\sqrt{\frac{93}{72}} \cdot \frac{132}{9} = 1.47A$$

Scokttky diode SB240 (2A/40V) is selected.

[STEP-6] Output Voltage and Current Setting

The nominal output current is determined by the sensing resistor value and transformer turns ratio as:

$$R_{SENSE} = \frac{N_P}{N_S I_O^N \times 8.5} \qquad (37)$$

The voltage divider R_{S1} and R_{S2} should be determined so that V_S is 2.5V at the end of diode current conduction time, as shown in Figure 9.

$$\frac{R_{S1}}{R_{S2}} = (\frac{N_a}{N_S}\frac{V_O}{2.5} - 1) \qquad (38)$$

Select 1% tolerance resistor for better output regulation.

(Design Example) The sensing resistor is obtained as:

$$R_{SENSE} = \frac{N_P}{N_S I_O^N \times 8.5} = \frac{117}{9 \cdot 0.75 \times 8.5} = 2.0\Omega$$

The voltage divider network is determined as:
$$\frac{R_{S1}}{R_{S2}} = (\frac{N_a}{N_S} \cdot \frac{V_O}{2.5} - 1) = (\frac{15}{9} \cdot \frac{5}{2.5} - 1) = 2.33$$

By setting R_{S1}=34.8kΩ, R_{S2} is obtained as 82kΩ.

It is recommended to place a bypass capacitor of 22~68pF closely between the V_S pin and the GND pin to bypass the switching noise and keep the accuracy of the sampled voltage for CV regulation. The value of the capacitor affects the load regulation and constant current regulation. Figure 13 illustrates the measured waveform on the V_S pin with a different V_S capacitor. If a higher value V_S capacitor is used, the charging time becomes longer and the sampled voltage is higher than the actual value.
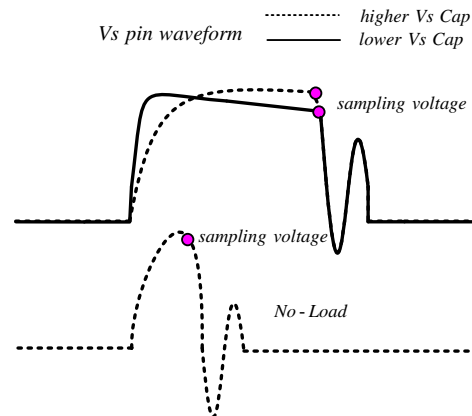

Figure 13. Effect on Sampling Voltage with Different V_S Capacitor

[STEP-7] Determine the Output Filter Stage

The peak to peak ripple of capacitor current is given as:

$$\Delta I_{CAP} = \frac{N_P}{N_S} I_{DS}{}^{PK} \tag{39}$$

The voltage ripple on the output is given by:

$$\Delta V_O = \frac{\Delta I_C \cdot T_D}{2C_O} \cdot \left(\frac{\Delta I_C - I_O{}^N}{\Delta I_C}\right)^2 + \Delta I_C \cdot R_C \tag{40}$$

Sometimes it is impossible to meet the ripple specification with a single output capacitor due to the high ESR of the electrolytic capacitor. Then, additional LC filter stages (post filter) can be used. When using the post filters, be careful not to place the corner frequency too low. Too low a corner frequency may make the system unstable or limit the control bandwidth. It is typical to set the corner frequency of the post filter at around 1/10~1/5 of the switching frequency.

> **(Design Example)** Assuming 470μF electrolytic capacitor with 30mΩ ESR for output capacitor, the voltage ripple on the output is:
>
> $$\Delta V_O = \frac{\Delta I_C \cdot T_D}{2C_O} \cdot \left(\frac{\Delta I_C - I_O{}^N}{\Delta I_C}\right)^2 + \Delta I_C \cdot R_C = 137mV$$

[STEP-8] Cable Voltage Drop Compensation

When it comes to cellular phone charger application, the actual battery is located at the end of cable, which causes typically several percentage of voltage drop on the actual battery voltage. FAN103 and FSEZ13X7 have cable voltage drop compensation that can be programmed by a resistor on the COMR pin, as shown in Table 3. The resistances of the standard 1.8m cable for different AWG are summarized in Table 4.

Table 3.   Cable Compensation

Percentage of Voltage Drop Compensation	COMR Resistor
7%	Infinite (Open)
6%	900kΩ
5%	380kΩ
4%	230kΩ
3%	380kΩ
2%	145kΩ
1%	100kΩ
0%	45kΩ

Table 4.   Resistance of 1.8M Cable for Different AWG

AWG	Ω/m	Resistance for 1.8m Cable
24	0.084	0.30Ω
25	0.106	0.38Ω
26	0.134	0.48Ω

> **(Design Example)** Assuming 26AWG/1.8m cable is used, the voltage drop at maximum output current is:
>
> $$\Delta V_O = R_{CABLE} \cdot I_O = 0.48 \cdot 0.75 = 0.36V$$
>
> $$\frac{\Delta V_O}{V_O} = \frac{0.36}{5} = 7.2\%$$
>
> The default setting can be used without any resistor on COMR pin. To improve the noise immunity of COMR pin, it is typical to connect a 1μF bypass capacitor on the COMR pin.

[STEP-9] Design RCD Snubber in Primary Side

When the power MOSFET is turned off, there is a high-voltage spike on the drain due to the transformer leakage inductance. This excessive voltage on the MOSFET may lead to an avalanche breakdown and eventually failure of the device. Therefore, it is necessary to use an additional network to clamp the voltage. The RCD snubber circuit and MOSFET drain voltage waveform are shown in Figure 14. The RCD snubber network absorbs the current in the leakage inductance by turning on the snubber diode (D_{sn}) once the MOSFET drain voltage exceeds the voltage of node X as depicted in Figure 14. In the analysis of snubber network, it is assumed that the snubber capacitor is large enough that its voltage does not change significantly during one switching cycle. The snubber capacitor should be ceramic or a material that offers low ESR. Electrolytic or tantalum capacitors are unacceptable due to these reasons.
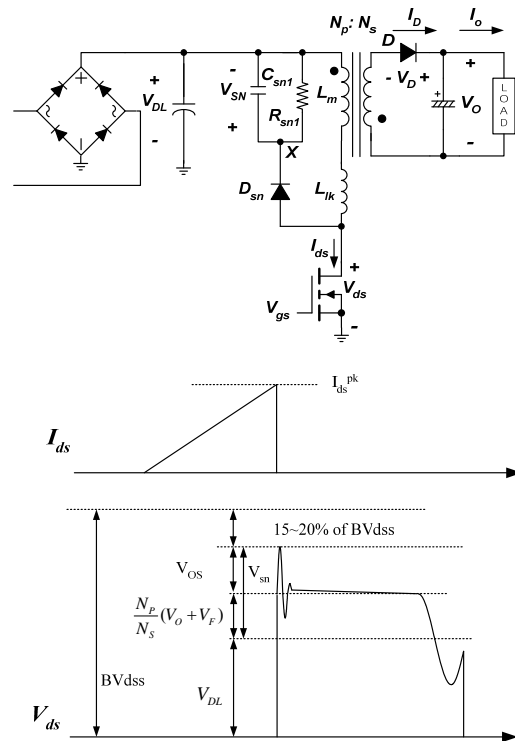
Figure 14. Snubber Circuit and its Waveforms

The snubber capacitor voltage at full load condition (V_{SN}) is given as:

$$V_{SN} = V_{RO} + V_{OS} \tag{41}$$

The power dissipated in the snubber network is obtained as:

$$P_{SN} = \frac{V_{SN}^{\ 2}}{R_{SN}} = \frac{1}{2} f_S L_{LK} (I_{DS}^{\ PK})^2 \frac{V_{SN}}{V_{SN} - V_{RO}} \tag{42}$$

where $I_{DS}^{\ PK}$ is peak drain current at full load, L_{LK} is the leakage inductance, V_{SN} is the snubber capacitor voltage at full load and R_{SN} is the snubber resistor.

The leakage inductance is measured at the switching frequency on the primary winding with all other windings shorted. Then, the snubber resistor with proper rated wattage should be chosen based on the power loss. The maximum ripple of the snubber capacitor voltage is obtained as:

$$\Delta V_{sn} = \frac{V_{SN}}{C_{SN} R_{SN} f_s} \tag{43}$$

In general, 5~20% ripple of the selected capacitor voltage is reasonable.

In the snubber design in this section, neither the lossy discharge of the inductor nor stray capacitance is considered. In the actual converter, the loss in the snubber network is less than the designed value due to this effect.

(Design Example) Since the voltage overshoot of drain voltage has been determined same as the reflected output voltage, The snubber voltage is:

$$V_{SN} = V_{RO} + V_{OS} = 144V$$

The leakage inductance is measured as 48μH. Then the loss in snubber network is given as:

$$P_{SN} = \frac{1}{2} f_S L_{LK} (I_{DS}^{\ PK})^2 \frac{V_{SN}}{V_{SN} - V_{RO}} = 0.20W$$

$$R_{SN} = \frac{V_{SN}^{\ 2}}{P_{SN}} = 99k\Omega$$

To allow 20% ripple on the snubber voltage (29V).

$$C_{SN} = \frac{V_{SN}}{\Delta V_{sn} R_{SN} f_s} = \frac{142}{28 \cdot 99 \times 10^3 \cdot 50 \times 10^3} = 1.0nF$$

5. Print Circuit Board Layout

Print circuit board layout and design are very important for switching power supply where the voltage and current change with high dv/dt and di/dt. Good PCB layout minimizes excessive EMI and prevents the power supply from being disrupted during surge/ESD tests

Guidelines:

- The numbers in the following guidelines refer to Figure 15 and Figure 16.
- To improve EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to capacitors C_{DL2} and C_{DL1} first, then to the primary switching circuits.
- The primary high-frequency current loop is in **C_{DL1} – Transformer – MOSFET – R_{CS} – C_{DL1}**. The area enclosed by this current loop should be kept as short as possible.
- Place R_{START} for protect the inrush spike (100kΩ is recommended).
- **R_{CS}** should be connected C_{DL1}'s ground directly. Keep it short and wide (Trace **4→1**) and place it close the CS pin for reducing switching noise. High-voltage traces related to the drain of MOSFET and RCD snubber should be kept far way from control circuits to prevent unnecessary interference. If a heat sink is used for the MOSFET, connect this heat sink to ground.

- As indicated by **2**, the area enclosed by the **transformer aux winding, D_{DD} and C_{DD}**, should also be kept short path.
- Place C_{DD}, C_S, R_{S2}, and C_{COMR} close to each pin of PSR controller for good decoupling and to reduce the switching noise.
- As indicated by **3**, the ground of the control circuits should be connected first, then to other circuitry.
- GND **3→2→4→1**: May make it possible to avoid common impedance interference for the sense signal.
- Regarding the ESD discharge path, put in the shortcut pad between AC line and DC output (which is the best way). The other method is to discharge the ESD energy to AC line through the primary main ground **1**. Because ESD energy is delivered from secondary to primary though the transformer stray capacitor, the controller circuit should not be placed on the discharge path. **5** shows places where the point-discharge route can be placed to bypass the static electricity energy. it is suggested to map out this discharge route in Figure 15 and Figure 16.
- For the surge path, select fusible resistor type with wire wound type to reduce inrush current and surge energy, use π input filter (two bulk capacitor and one inductance) to share the surge energy.
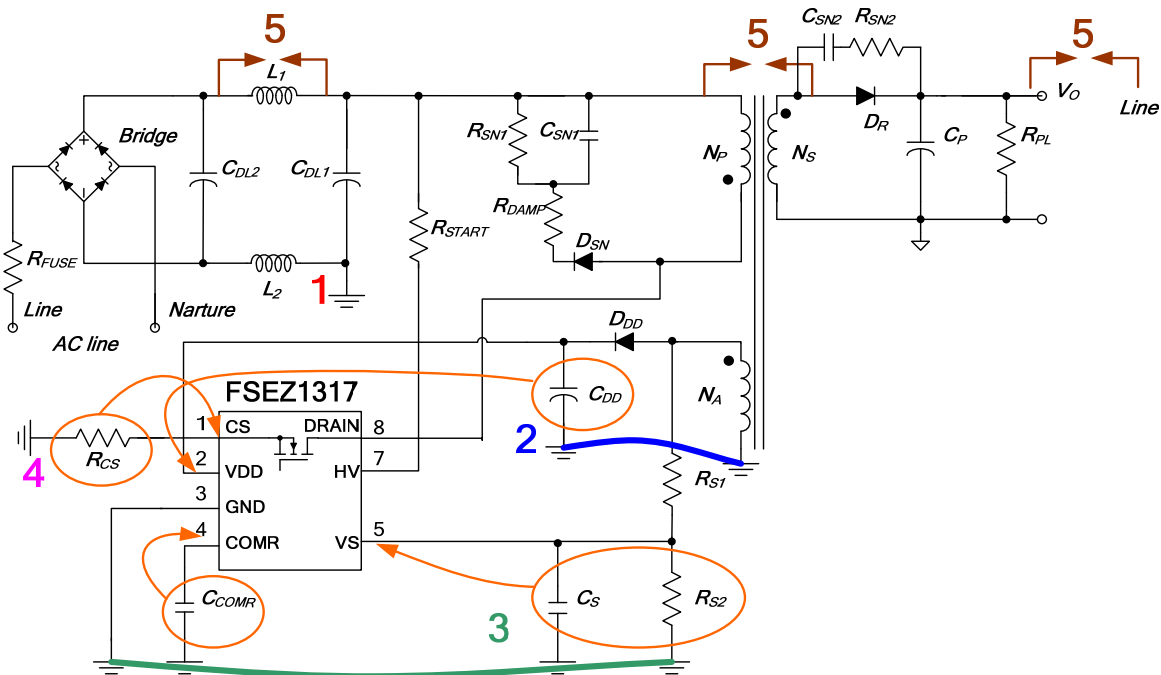
Figure 15. EZ-PSR FSEZ13X7 Layout Consideration
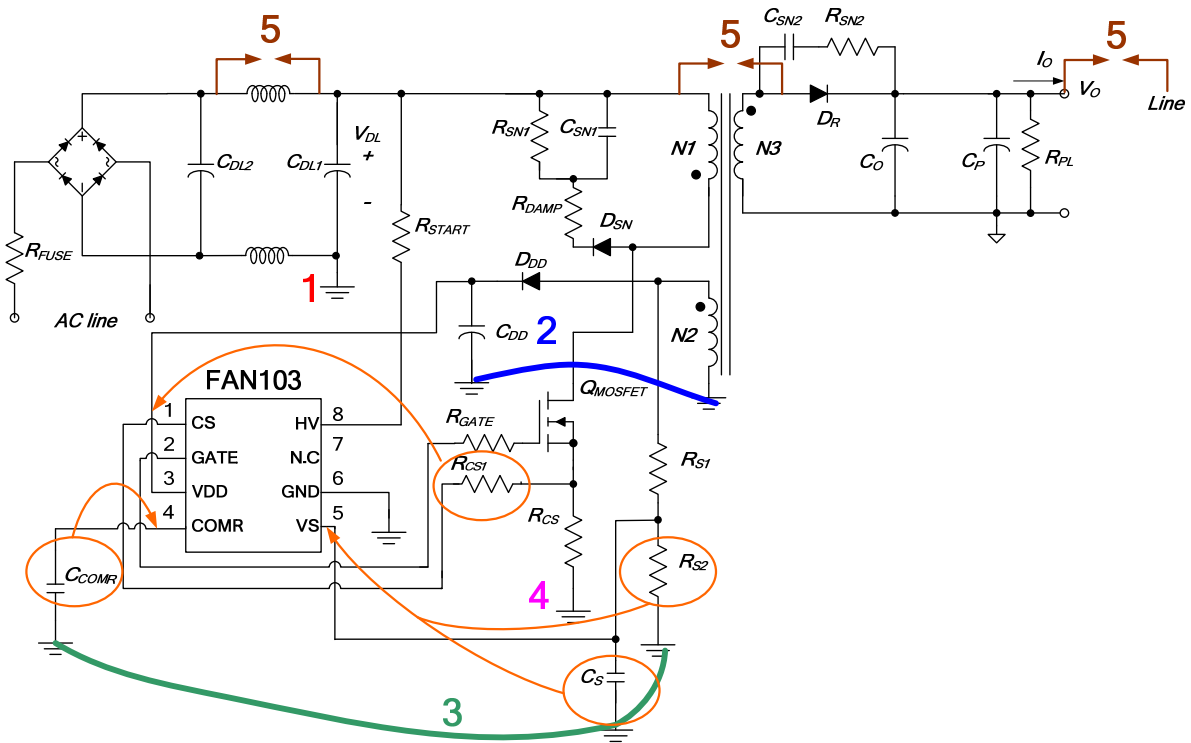
Figure 16. PSR PWM FAN103 Layout Consideration

6. Final Schematic of Design Example

Figure 17 shows the final schematic of the 3.75W charger design example. EE16core is used for the transformer. Figure 18 shows the transformer information.
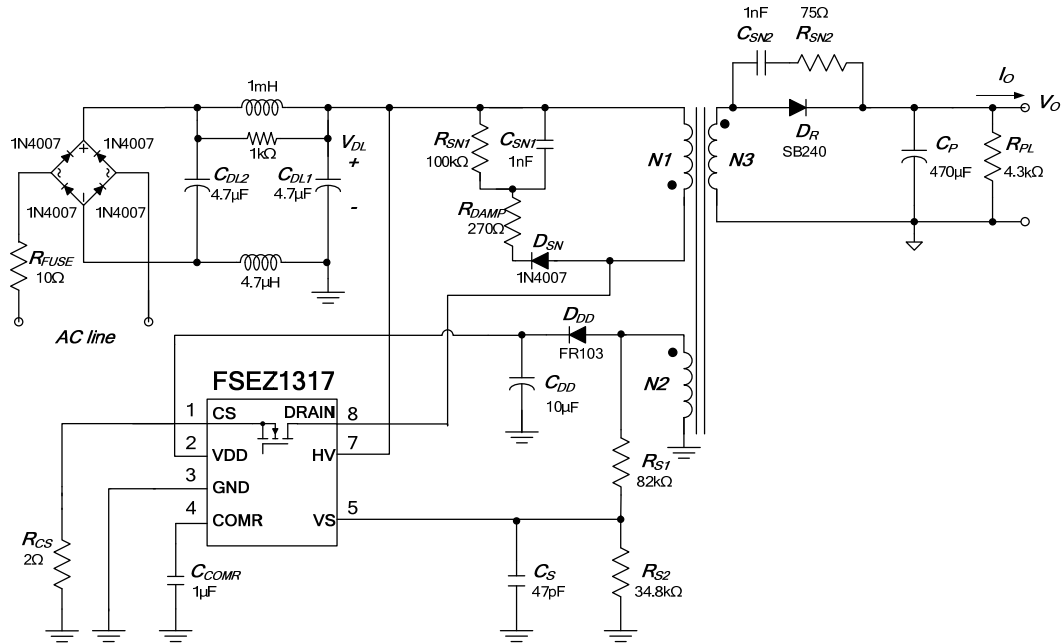
Figure 17. Final Schematic of the EZ-PSR FSEZ1317 3.75W Design Example

Core: EE16 PC40
Bobbin: EE16 (10 pins) Horizontal type
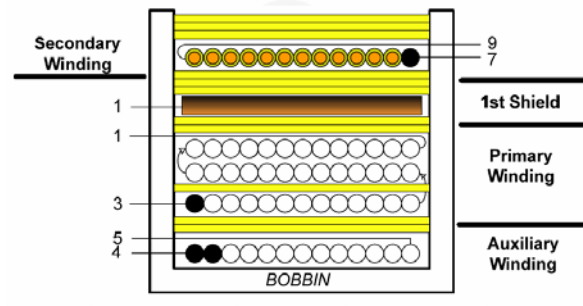
Figure 18. Transformer Structure

Notes:
1. When W4R's winding is reversed winding, it must wind one layer.
2. When W2 is winding, it must wind three layers and put one layer of tape after winding the first layer.

| NO | TERMINAL | | WIRE | t_s | INSULATION | BARRIER TAPE | |
	S	F			t_s	Primary	Seconds
W1	4	5	2UEW 0.23*1	15	2		
W2	3	1	2UEW 0.18*1	41	1		
				39	0		
				37	2		
W3	1		COPPER SHIELD	1.2	3		
W4	7	9	TEX-E 0.55*1	9	3		
			CORE ROUNDING TAPE		3		

	Pin	Specification	Remark
Primary-Side Inductance	1−3	2.25mH ± 5%	100kHz, 1V
Primary-Side Leakage Inductance	1−3	80μH Maximum	Short One of the Secondary Windings

7. Test Result of Design Example

To show the validity of the design procedure presented in this application note, the converter of the design example has been built and tested. All the circuit components are used as designed in the design example.

Figure 19 shows the operation waveforms at 70% of nominal output voltage and minimum line voltage condition. As designed in STEP-4, the non-conduction time is 4μs before frequency reduction occurs, which guarantees DCM operation. Figure 20 shows the operation waveforms at minimum output voltage and minimum line voltage condition. As designed in STEP-4, the non-conduction time is about 6.8μs, which guarantees DCM operation.

Figure 21 shows the measured efficiency for different load conditions. The average efficiencies at $115V_{AC}$ and $230V_{AC}$ condition are higher than 68%. Figure 22 shows the measured no-load power consumption at different line voltage. As can be seen in the figures, even in the $264V_{AC}$ AC line, the no-load standby power consumption is still less than 30mW, meeting the five-star level of new power consumption regulation for charger.

Figure 23 shows the measured output voltage and output current curve. CV regulation achieves 1.38% for entire line and load condition. The CC regulation can achieve 3.6% with a fold-back voltage of 1.5V.
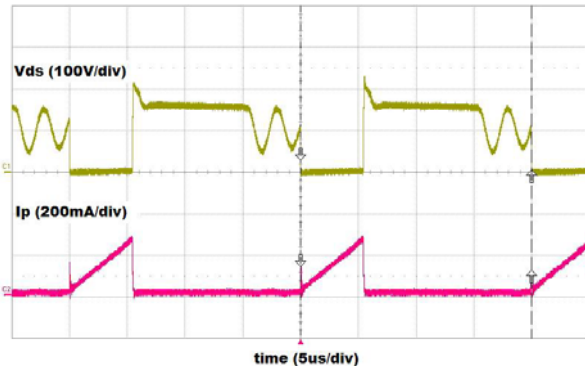
Figure 19. Operation Waveforms at 70% of Nominal Output Voltage and Minimum Line Voltage Condition
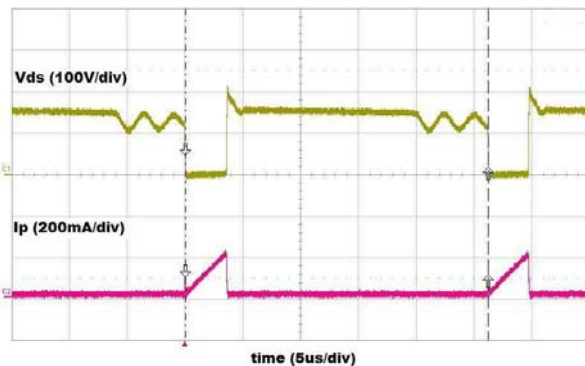
Figure 20. Operation Waveforms at Minimum Output Voltage and Minimum Line Voltage Condition
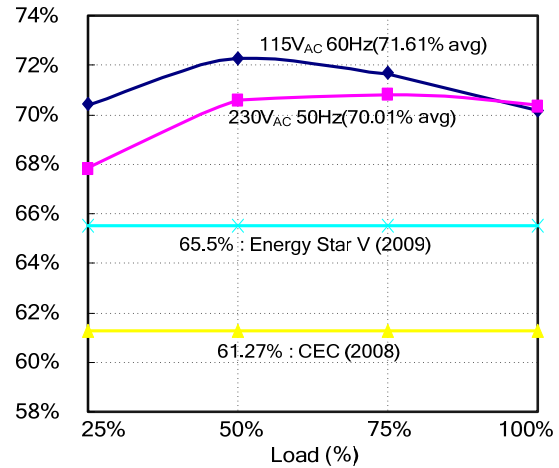
Figure 21. Measured Efficiency
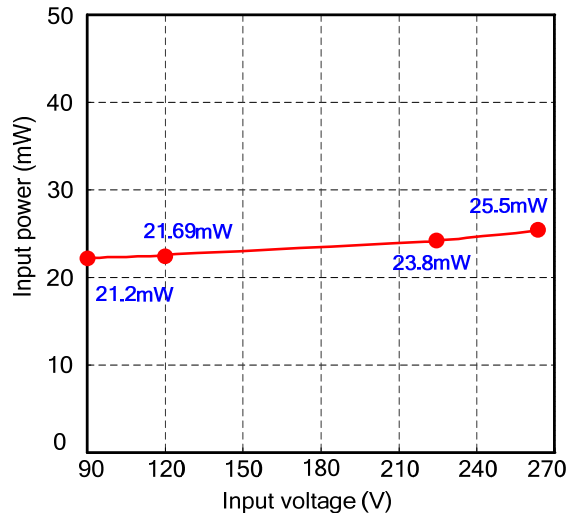
Figure 22. Measured No-Load Power Consumption
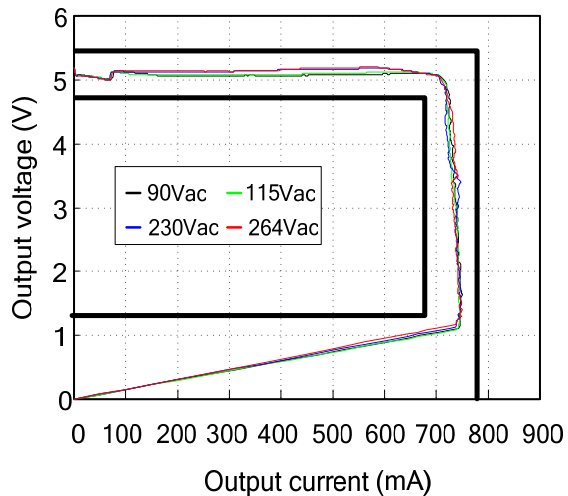
Figure 23. Measured Output Voltage and Output Current Curve

8 Related Resources

FSEZ1317 — Primary- Side Regulation PWM with Power MOSFET Integrated Datasheet

FAN103 — Primary-Side Regulation PWM Controller Datasheet

AN-6067 — Design and Application of Primary-Side Regulation (PSR) PWM Controller

Fairchild Power Supply WebDesigner — Flyback Design & Simulation - In Minutes at No Expense

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