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Touch Screen EMI/ESD Protection

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TECHNICAL NOTE

Introduction

Touch screen revolutionized the computing industry user interfaces and user experiences especially after the perfection of multi-touch technology. A major force to the resurrection of the once sleepy touch screen industry is the spread of touch panels are the benefits they offer in the way of intuitive operation. Since they can be used for input through direct contact with icons and buttons, they're easy for unaccustomed user to comprehend and the ease of usage. Touch panels also allow permit miniaturization and simplification of devices by combining display and input into a single piece hardware. Since touch panel buttons are software, not hardware, their interfaces can be integrated throughout the usage cycle.

Projected capacitive touch screens like those first featured by leading smartphone and tablet manufacturers is as high as 54% of the touch market in 2011. They also will remain the dominant implementation for the space in the years to come, ahead of other touch-sensor technologies like infrared, optical, resistive and surface acoustic wave.

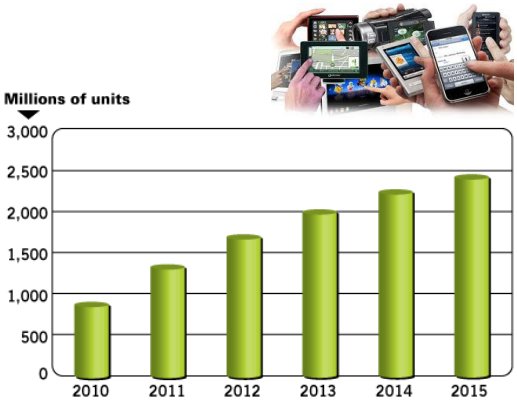

Figure 1. Worldwide Shipment Forecast of Touch-Screen Controller
(SOURCE: IHS iSuppli Research, March 2012)

TRENDS IN TOUCH SCREENS

There are five main touch screen technologies: resistive, surface capacitive, projected capacitive, surface acoustic wave, and infrared. In terms of cost and size, the first three suit mobile products. In all cases, the system consists of a sensing mechanism, a control circuit, and an interface to the control circuit. For the purpose of this paper only Projected Capacitive and Resistive Touch Screen EMI/ESD is discussed.

Projected Capacitive Touch Panels

Leading smartphone and tablet manufacturers adopt this method to achieve high-precision multi-touch functionality and high response speed. Projected capacitive touch panels are often used for smaller screen sizes than surface capacitive touch panels. The internal structure of these touch panels consists of a substrate incorporating an IC chip for processing computations, over which is a layer of numerous transparent electrodes is positioned in specific patterns. The surface is covered with an insulating glass or plastic cover. When a finger approaches the surface, electrostatic capacity among multiple electrodes changes simultaneously, and the position were contact occurs can be identified precisely by measuring the ratios between these electrical currents as shown in Figure 2.

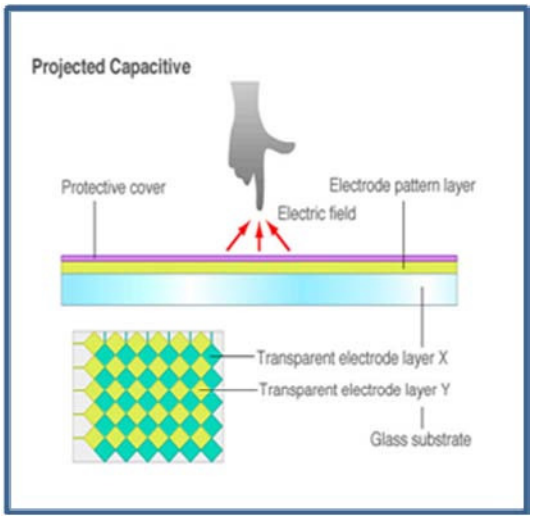

Figure 2. Projected Capacitive Touch Screen

A unique characteristic of a projected capacitive touch panel is the fact that the large number of electrodes enables accurate detection of contact at multiple points (multi-touch). However, the projected capacitive touch panels featuring indium-tin-oxide (ITO) found in smart

phones and similar devices are poorly suited for use in large screens, since increased screen size results in increased resistance (i.e., slower transmission of electrical current), increasing the amount of error and noise in detecting the points touched.

Larger touch panels use center-wire projected capacitive touch panels in which very thin electrical wires are laid out in a grid as a transparent electrode layer. While lower resistance makes center-wire projected capacitive touch panels highly sensitive, they are less suited to mass production than ITO etching.

Resistive Touch Panels

A resistive touch screen works by applying a voltage across a resistor network and measuring the change in resistance at a given point on the matrix where a screen is touched by an input stylus, pen, or finger. The change in the resistance ratio marks the location on the touch screen. The two most popular resistive architectures use 4-wire or 5-wire configurations as shown in Figure 3.

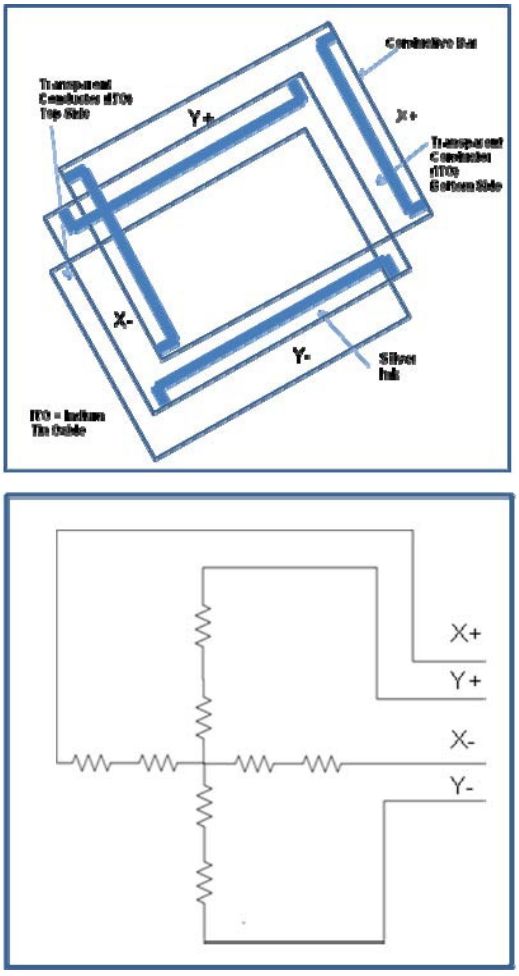

Figure 3. 4-wire Touch Screen Construction

A 4-wire touch screen is constructed as shown in Figure 3. It consists of two transparent resistive layers. The 4-wire touch screen panel works by applying a voltage across the vertical or horizontal resistive network. The A/D converts the voltage measured at the point the panel is touched. A measurement of the Y position of the pointing device is made by connecting the X+ input to a data converter chip, turning on the Y+ and Y− drivers, and digitizing the voltage seen at the X+ input. The voltage measured is determined by the voltage divider developed at the point of touch. For this measurement, the horizontal panel resistance in the X+ lead doesn't affect the conversion due to the high input impedance of the A/D converter. Voltage is then applied to the other axis, and the A/D converts the voltage representing the X position on the screen through the Y+ input. This provides the X and Y coordinates to the associated processor as shown in Figure 4.

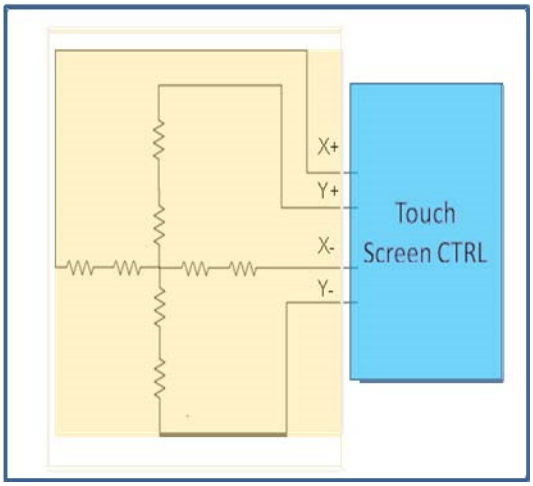

Figure 4. Wire Simplified Schematic

The benefits of this design is unparallel than other touch screen design; include the low-cost manufacture, due to the simplicity of structure. This design consume less power and is strongly resistant to external impurity such as dust and water since the surface is covered in film. In addition, input relies on pressure being applied to the film, it can be used for input not just with bare fingers, but even when wearing gloves or using a stylus. These screens can also be used to input handwritten text.

Drawbacks include lower light transmittance (reduced display quality) due to the film and two electrode layers; relatively lower durability and shock resistance; and reduced precision of detection with larger screen sizes. (Precision can be maintained in other ways − for example, splitting the screen into multiple areas for detection.)

EMI/ESD ISSUES

The market trend continues to produce thinner mobile devices. This means projected and capacitive touch screens are the design choices, as they allow direct lamination of capacitive touch sensors to the display, migration of the sensor inside the display, and so comes with many other challenges of EMI/ESD with antennas, charger and ground loading.

Unwanted EMI/ESD is one of the biggest concerns related to capacitive touch screens. This is noise that is physically coupled into the sensor through the mobile device during the touch event.. It can be seen as degraded accuracy or linearity of touch, false or phantom touches, or just simply erratic behavior. The culprits include marginal layouts, poor antenna designs, and poor peripherals. These prove to be significant sources of EMI/ESD. With PCB real estate continuing to be at a premium within the mobile device, layouts and designs can sometimes be compromised: components are literally being placed on top of each other. This sometimes leads to antennas being placed in extremely closes proximity to the touch sensors, and can create problems with the radios falsely activating the touch sensor. Common mechanical countermeasures such as metal shields no longer are effective solutions for resolving the EMI problems.

On chip protection solutions for CMOS ICs often include high-voltage suppression circuits on input and output pins. These are active RC shunts which turn on whenever the pad voltage goes outside of the normal operating range. However, the effectiveness is limited gate oxide thickness and size: as they dissipate high-voltage energy, some of that energy is converted to heat can cause a thermal event within the chip itself. In addition, these internal ESD circuits have a maximum allowable current density proportional to their size. In an ESD event, as maximum current density is reached, the forward voltage potential across the circuit begins to rise. A highly-energetic ESD event can cause this potential to rise above the circuit's maximum allowable forward voltage, causing damage, the IC's internal ESD protection circuits melt or break down (primary failure), and high energy is passed without attenuation to the device's internal circuits, damaging them as well (secondary failure). Because of the speed of the ESD event (most last less than a microsecond), the damage from heating will tend to stay within the local region of the IC's ESD protection circuit. Also, the amount of energy any single protection circuit can carry is directly proportional to its size. ESD immunity tests introduce a single, measured amount of energy to the IC. As a result, if that energy can be spread between several protection circuits both internally and external ESD protection circuits the likelihood of damage is greatly reduced. To do this, additional external ESD protection devices are implemented shown in Figures 5 and 6.

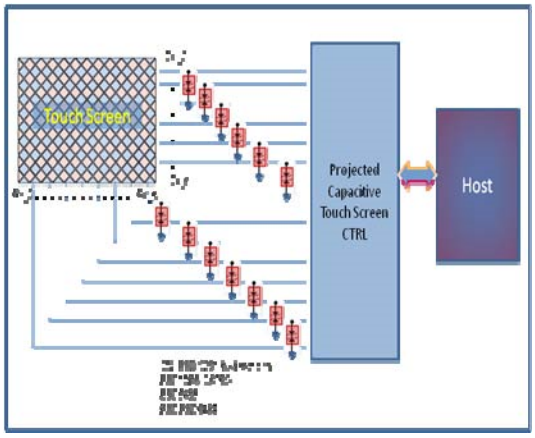

Figure 5. Projected Capacitive Touch Screen with External ESD Protection

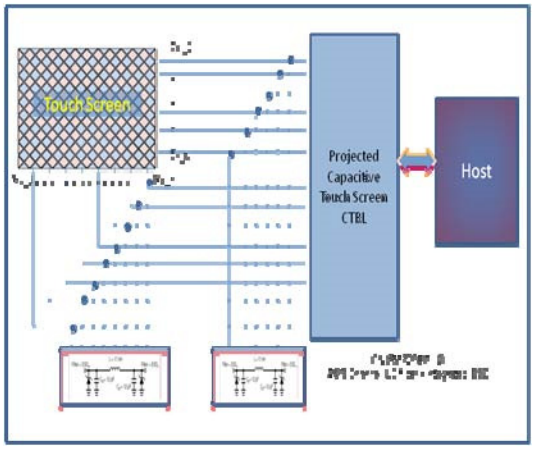

Figure 6. Projected Capacitive Touch Screen with External LC Filer + Integrated ESD Protection

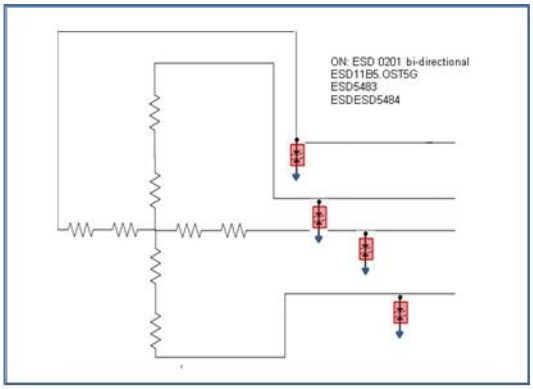

Figure 7. 4-wired Touch Screen with External ESD Protection

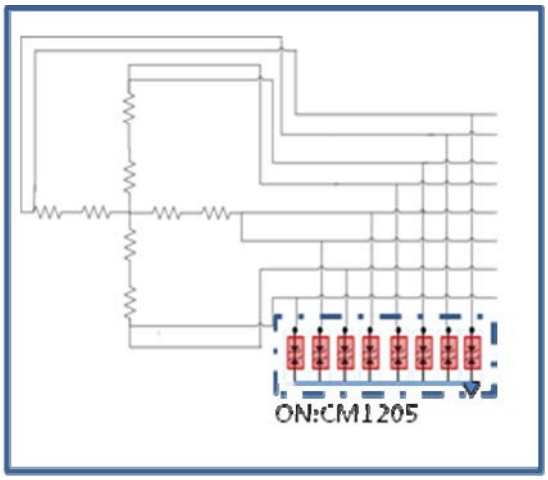

Figure 8. 8-wired Touch Screen with External ESD Protection

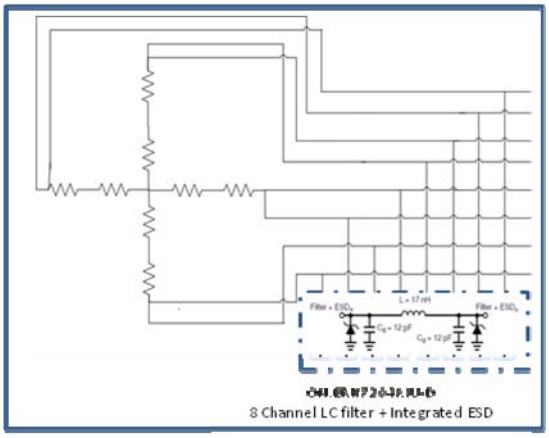

Figure 9. 8-wired Touch Screen with LC Filter + Integrated ESD Protection

CONCLUSIONS

Projected capacitive touch screens like those first featured by smartphones will remain the dominant implementation for the space in the years to come, ahead of other touch-sensor technologies like infrared, optical, resistive and surface acoustic wave.

Design considered trade-off: a direct function of the die area (and thus product cost) devoted to the internal protection circuits versus the cost of adding extra protection devices outside the capacitive sensing controller for those lines in the system which may be more vulnerable to ESD events. Impedance of the integrated circuit's pin is a significant factor in the usefulness of external ESD protection circuits.

External circuits can be designed to work synergistically with the complex impedance of the IC's pad circuitry and its packaging. The combination can *provide an effective level of ESD control* that is hard to achieve by using only on-chip, integrated protection circuitry. Levels of ESD protection for CMOS circuits are based on a balance between product cost and expected requirements for protection in production and end-use. For applications requiring high ESD immunity on some lines, additional external protection can be provided using inexpensive methods by employing single channel ESD protection or low pass filer couple with ESD circuit si plastic package.

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[3] Solid State Technology December 11, 2012, IHS iSuppli Research, March 2012.

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