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## The Changing ESD Landscape

### ESD Protection Architecture Design Considerations for Next Generation Devices



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#### TECHNICAL NOTE

#### Executive Summary

This paper is intended to eliminate the confusion around ESD protection architectures so that you can confidently take the next step toward designing more reliable systems. Main topics include ESD protection device fundamentals, important considerations for choosing an ESD protection device, and shortcomings of traditional ESD protection architectures. Lastly, this paper introduces an innovative, breakthrough ESD protection architecture created by ON Semiconductor.

#### Introduction

Two important trends are leading to fundamental changes in ESD protection strategies at the system design level: increased susceptibility of system ICs to ESD as they migrate to more advanced process technology nodes, and increasingly stringent signal integrity requirements as data rates continue to climb.

The traditional approach to dealing with higher data rates has been to reduce the capacitance of the ESD protection device, but doing this tends to reduce the ESD protection capabilities of the device. As a result, system designers are forced to make tradeoffs between system reliability and signal integrity.

Traditional ESD architectures fail to provide suitable protection because they were not designed to protect these increasing levels of susceptibility of these new system ICs. Clamping voltages and residual current levels that were acceptable for previous generations of ASICs can destroy modern semiconductor devices. Additionally, the increasing adoption of high speed data interfaces such as USB 2.0, HDMI®, and Display Port, adds to the complexity of maintaining a high level of signal integrity while ensuring robust ESD protection.

The changing application environment also contributes to increased ESD vulnerability. A proliferation of laptop computers and handheld devices such as cell phones, MP3 players, digital cameras, and other mobile devices are being used in uncontrolled environments (i.e., no wrist-grounding straps or conductive and grounded table surfaces). In these environments, people touch I/O connector pins during the connecting and disconnecting of cables. In addition, a portable device can build up a charge during normal usage,

such as being carried in a purse, and discharge that energy when connected to another device, such as a computer or a TV.

With traditional ESD architectures, an inverse relationship exists between robust ESD protection and low capacitance levels. More robust ESD protection has typically meant higher levels of capacitance. In turn, this negatively impacts signal integrity, forcing designers to carefully balance ESD protection with signal integrity. With the advent of high speed serial data interfaces, this delicate balance has become increasingly difficult to maintain.

#### *Confusing Specifications, Standards, and Testing Criteria*

Determining which ESD protection device provides the greatest protection is increasingly difficult. Many designers don't know which factors are most important when choosing an ESD device to ensure reliability. Often, the answers are not provided or are not obvious in many ESD protection device datasheet specifications. In addition to the confusion of critical ESD electrical specifications, there is confusion around interpretation of industry standards, and what constitutes adequate protection and the acceptable testing criteria. Today's designer must also pay considerable attention to voltage level (clamping voltage) and how much current (residual current) will be seen by the ASIC. While low capacitance for signal integrity is certainly important, other crucial considerations for signal integrity must be made in regards to layout, capacitance matching, and impedance matching issues.

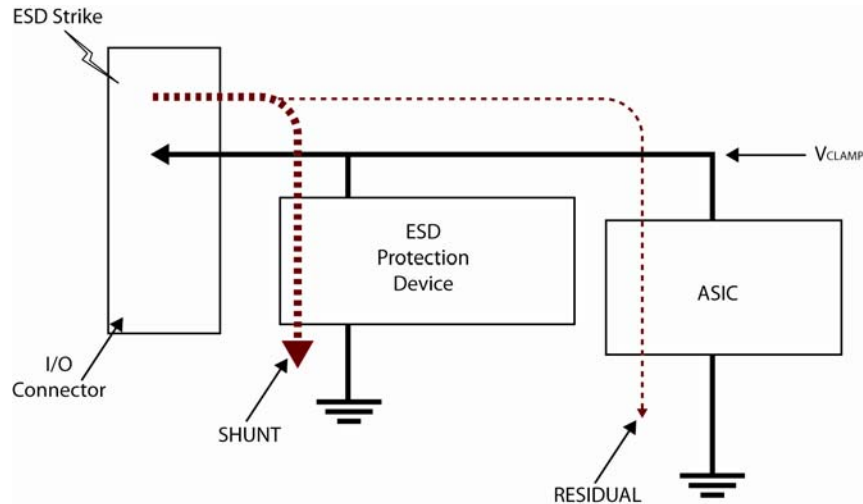
#### **How ESD Protection Devices Work**

An ESD event is the transfer of energy between two bodies at different electrostatic potentials. This transfer occurs through contact or via an ionized ambient discharge (a spark). This transfer is modeled in various standard circuit models for testing the compliance of device targets. Typically, these models use a capacitor charged to a given voltage, and then some form of current-limiting resistor (or ambient air condition) to transfer the energy pulse to the target. ESD protection devices attempt to divert this potentially damaging charge away from sensitive circuitry and protect the system from permanent damage (see Figure 1).

As shown in Figure 1, a traditional, single stage ESD protection device performs the following actions when an ESD strike occurs:

1. The voltage is “clamped” to a lower voltage to minimize the voltage seen at the ASIC.
2. The protection device shunts current to ground and away from the protected ASIC.

3. Once the ESD strike is fully dissipated, the ESD protection device attempts to return to a high impedance state. Some types of devices can take over twenty-four hours to return to this state so it is important to understand this characteristic.



**Figure 1. ESD Protection Devices Attempt to Divert a Potentially Damaging Charge Away from Sensitive Circuitry and Protect the System from Permanent Damage**

The clamping voltage and residual current seen at the ASIC are a function of the breakdown voltage and the dynamic resistance of the protection device. The  $V_{CLAMP}$  can be approximated by multiplying the dynamic resistance of the ESD circuit by the current in the strike (30 A for an 8 kV ESD strike) and adding it to the breakdown voltage. Some ESD devices have a high resistance, resulting in very high clamping voltages. In addition, high dynamic resistance also results in less current being shunted to ground and more reaching the ASIC. Residual current, the current reaching the ASIC, is inversely proportional to the ratio of the  $R_{dyn}$  of the ESD device and the  $R_{dyn}$  of the ASIC, so it is critical to minimize the dynamic resistance of the ESD protection circuit.

#### **Fundamentals of ESD Damage: Why Smaller Geometry Circuits are More Vulnerable to ESD**

As IC manufacturers move to smaller geometries, they continue to scale the dimensions of the transistors, interconnections, and the silicon layers in their devices. This decrease results in smaller architectures for higher-speed devices that are more susceptible to breakdown damage at lower energy levels. Silicon layers are more likely to rupture, and metal traces are more likely to open or bridge during an ESD event.

Traditionally, ESD energy has been shunted away from the ICs using devices with moderate capacitances of 10 to 100 pF. Now with higher signal frequencies, these devices cannot be used without distorting the signal beyond

recognition or detection. Most high speed data ports now require ESD protection devices to add no more than 1–2 pF of capacitance to the line.

Most ICs are designed with limited internal ESD protection that allows them to tolerate from 1 to 2 kV pulses per the human body model (HBM). While this is sufficient to protect the ICs during PCB assembly, it is not intended to protect the ICs when the systems are shipped to end users.

#### **Limitations of Existing ESD Architectures**

There are several types of ESD protection devices available today, but the most common are divided into three categories: polymers, varistors/suppressors, and diodes. The most difficult task in determining which ESD protection device to choose is one that should be the easiest – that is, figuring out which device will provide the greatest protection. Often, system vendors compare ESD protection devices using data sheet ESD level ratings. In reality, these ratings say nothing about how well the device will protect the system. For example, device X may say 8 kV, device Y says 15 kV, so device Y is better – or is it? ESD ratings for protection devices say only what the device itself will survive, not what the system will survive. In many cases, an 8 kV device can offer more protection than the 15 kV device depending on other diode characteristics.

In addition to the ESD rating level of the protection device, voltage level (clamping voltage) and how much current (residual current) will be seen by the ASIC are critical considerations. ESD protection devices function by

shunting most of the current to ground and “clamping” the voltage seen at the ASIC to a lower value than the strike voltage.

Determining the clamping voltage and residual current is not an easy task. The clamping voltage quoted in most ESD protection datasheets – if it is there at all – is often misleading. The residual current is never quoted, because it is a product of the system layout rather than of the device itself. As a proxy, using the protection circuit’s dynamic resistance ( $R_{dyn}$ ) can help compare devices, since a device with lower resistance will shunt a higher proportion of the current. Unfortunately, this value is usually not even mentioned in protection datasheets.

#### *Polymer Devices*

While polymers seem attractive for high-frequency applications due to their sub-picofarad capacitance of 0.05–1.0 pF, this low capacitance comes with some not-so-attractive side effects.

Unlike diodes, a polymer device does not break down until it reaches a trigger voltage that is much higher than the clamping voltage. A typical polymeric ESD device does not break down until as much as 500 V is reached. Then it snaps back to a clamping voltage of up to 150 V. After the charge is dissipated, the polymer is supposed to return to its high-impedance state. However, this can take time, from several hours to a day, which makes them unattractive for consumer applications. These devices are difficult to accurately characterize in manufacturing and data sheets often contain only typical specifications without guaranteed minimums and maximums. Additionally, because these are physically elastic devices, their performance degrades based on the number of ESD pulses they receive.

#### *Varistors and Suppressors*

Varistors and suppressors are non-linear variable resistors. Although they are relatively inexpensive, suppressors typically suffer from high trigger voltages, high clamping voltages, and high resistance, which cause most of the energy to reach the protected device instead of being shunted to ground. Typical low capacitance suppressors have clamping voltages that range from 150 to 500 V. Low capacitance suppressors typically have a dynamic resistance of 20 to 40  $\Omega$ . Due to this high resistance, almost all ESD strike current is passed through to the “protected” device rather than being shunted to ground.

Another disadvantage of suppressors is that they degrade with use. Changes in electrical properties have been observed after a single ESD strike, including changes in capacitance. Most varistors and suppressors fail after 10 to 20 ESD strikes.

#### *Semiconductor Diodes*

Another method used for ESD protection is the semiconductor diode. ESD protection diodes are characterized by low clamping voltages, low resistance, fast turn-on times, and better reliability. Generally, semiconductor diodes offer the best ESD protection, and are now available with capacitance below 1 pF, making them the best choice for reliable ESD protection and good signal integrity.

#### **Comparing Clamping Voltages**

Current industry practice is to publish clamping voltages based on a pulse with an 8  $\mu$ s rise time and a duration of 20  $\mu$ s. Most datasheets document clamping voltage using a 1 A pulse and sometimes a higher current pulse as well. It is important to note that this pulse is not equivalent to an ESD pulse, which has a 1 ns rise time and a duration of 60 ns. In addition, the clamping voltage seen during a level 4 IEC 61000–4–2 strike with a peak current of 30 A is much different than seen during a 1 A pulse. However, because this is often the only data available when looking at datasheets, it provides a good starting point for comparing different ESD protection devices.

In general, semiconductor diodes have the lowest peak clamping voltages, while suppressors and polymers have clamping voltages significantly higher. Using the standard 1 A pulse described above, most semiconductor ESD protection diodes are rated to clamp between 8 and 15 V. When confronted with an 8 kV IEC 61000–4–2 strike, these diodes typically show peak clamping voltages of 50 to 100 V, depending on other diode characteristics such as dynamic resistance.

In contrast, suppressors can be several times higher – typical low capacitance suppressors can have clamping voltages that range from 150 to 500 V. Polymer devices suffer from even higher clamping voltages, due to a need for a “trigger” voltage. Common polymer protection devices can have a trigger voltage as high as 500 V. This requirement for a higher trigger voltage inhibits the turn-on time of the polymer, increasing the likelihood of damage to the protected device. In general, because of their lower clamping voltages and faster turn-on times, semiconductor diodes provide better ESD protection than either polymer or varistor solutions.

#### *Residual Current and Dynamic Resistance*

The amount of current flowing through to the ASIC is dependent on the dynamic resistance through the protection circuit versus the dynamic resistance through the ASIC. As the resistance through the protection circuit increases, the amount of current flowing through the protected device increases proportionally, increasing the likelihood of ESD damage.

The system designer should choose an ESD protection device that will shunt as much current as possible and minimize the residual current seen at the ASIC. Because residual current is system dependent, it is not typically specified in ESD protection datasheets. Unfortunately, very few ESD protection vendors specify their dynamic resistance either, but there are ways to approximate these values.

Most diode vendors provide graphs of current vs. voltage. Although these graphs usually use 8/20  $\mu$ s pulses rather than IEC 61000-4-2 pulses, they can be used as general indicators of the resistance of the circuit. For 8/20  $\mu$ s pulses, the relationship between current and voltage is fairly linear, and the slope of the line is the dynamic resistance ( $R_{dyn}$ ).

Typical ESD diodes have  $R_{dyn}$  that ranges from  $< 1$  to  $3 \Omega$ . Polymer devices also have very low resistance once they trigger.

In contrast, low capacitance varistors and suppressors, which are similar in electrical properties and ESD performance, typically have very high dynamic resistance in the range of  $20 \Omega$  or more, which results in much higher current levels seen at the protected ASIC. Figure 2 shows the results from a system test comparing the levels of residual current seen at a specific HDMI ASIC when protected by a low capacitance varistor or suppressor vs. a low capacitance diode. The test was performed with a 4 kV IEC 61000-4-2 pulse, and shows the current that flowed through the ASIC device over the duration of the pulse.

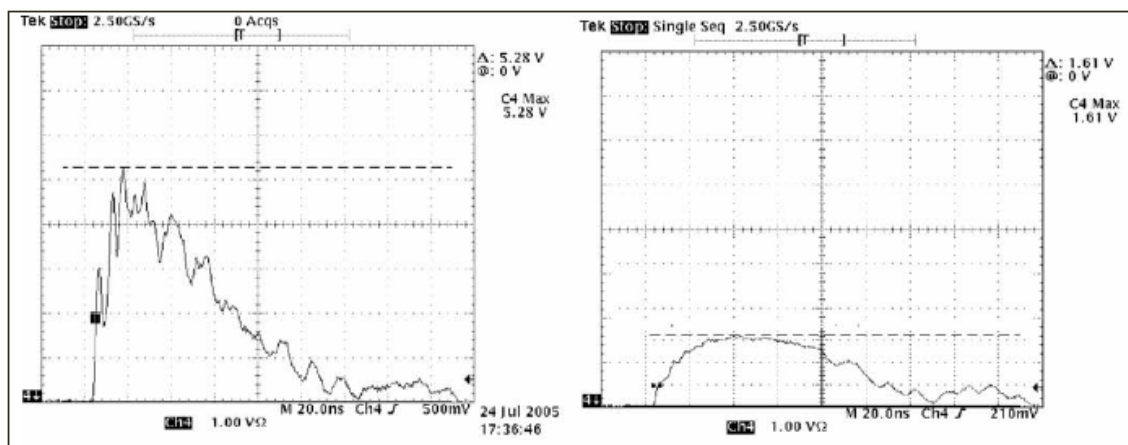


Figure 2. Residual Current in Suppressor vs Diode

In this test, the peak residual current was 10.6 A when protected by a varistor (left), versus 3.2 A when protected by semiconductor diodes (right). A 4 kV IEC 61000-4-2 strike has a maximum peak current of 15.0 A, demonstrating that the varistor/suppressor was unable to shunt even 1/3 of the current during the ESD strike! Also, just as importantly, the current seen at the ASIC during the entire duration of the strike was significantly higher in the varistor-based circuit. This illustrates the importance of comparing dynamic resistance when choosing ESD protection devices.

ESD protection is increasingly critical as semiconductor geometries shrink and consumer usage of mobile electronics continues to increase. Traditional protection methods and testing methodologies are reaching their limits and are not adequate for the latest generation of ASICs. Higher data rates are requiring lower capacitance circuits. Generally, as capacitance goes down,  $R_{dyn}$  increases, resulting in degraded ESD protection performance with higher clamping voltages and higher residual current. As

semiconductor geometries continue to shrink and data rates continue to increase, new methods of ESD protection must be developed to provide required protection levels even without interfering with high speed signals.

#### XtremeESD Protection: Superior Protection and Outstanding Signal Integrity

Recognizing that a radically new approach is required to meet today's ESD requirements, ON Semiconductor has introduced the PicoGuard XP architecture, the first member of its XtremeESD family of ESD protection devices. PicoGuard XP offers significantly better ESD performance than traditional ESD protection devices and will be followed by the PicoGuard XS architecture, which is designed to provide outstanding signal integrity for high speed data interfaces along with improved ESD protection. With these new options, designers can ensure their systems meet both their reliability and signal integrity goals without compromise.

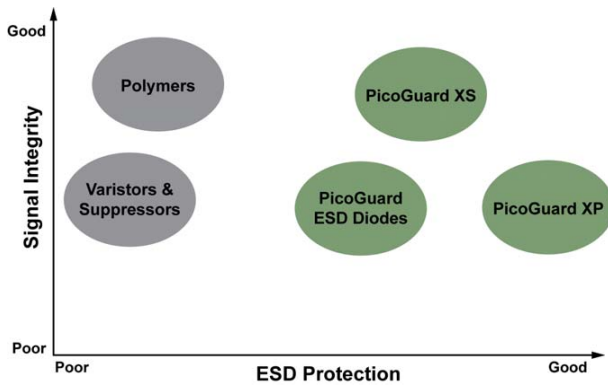



Figure 3. ESD Protection vs Signal Integrity

**Ensuring ESD Protection Reliability with PicoGuard XP**

ON Semiconductor introduced a fundamentally new approach to ESD protection with PicoGuard XP. Using a revolutionary double-clamp architecture, PicoGuard XP provides a superior level of ESD protection for digital consumer electronics and computing devices while offering low capacitance and excellent signal integrity. PicoGuard XP offers the industry’s highest level of ESD protection with excellent signal integrity in a compact footprint.

When an ESD strike occurs, PicoGuard XP dramatically reduces clamping voltage and residual current, resulting in more than a 65 percent reduction in I<sup>2</sup>R power reaching the protected chip as compared to traditional ESD protection diodes. Designed for high speed applications such as USB, HDMI 1.3, and DisplayPort devices, PicoGuard XP performs significantly better than the best ESD diode arrays on the market.

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