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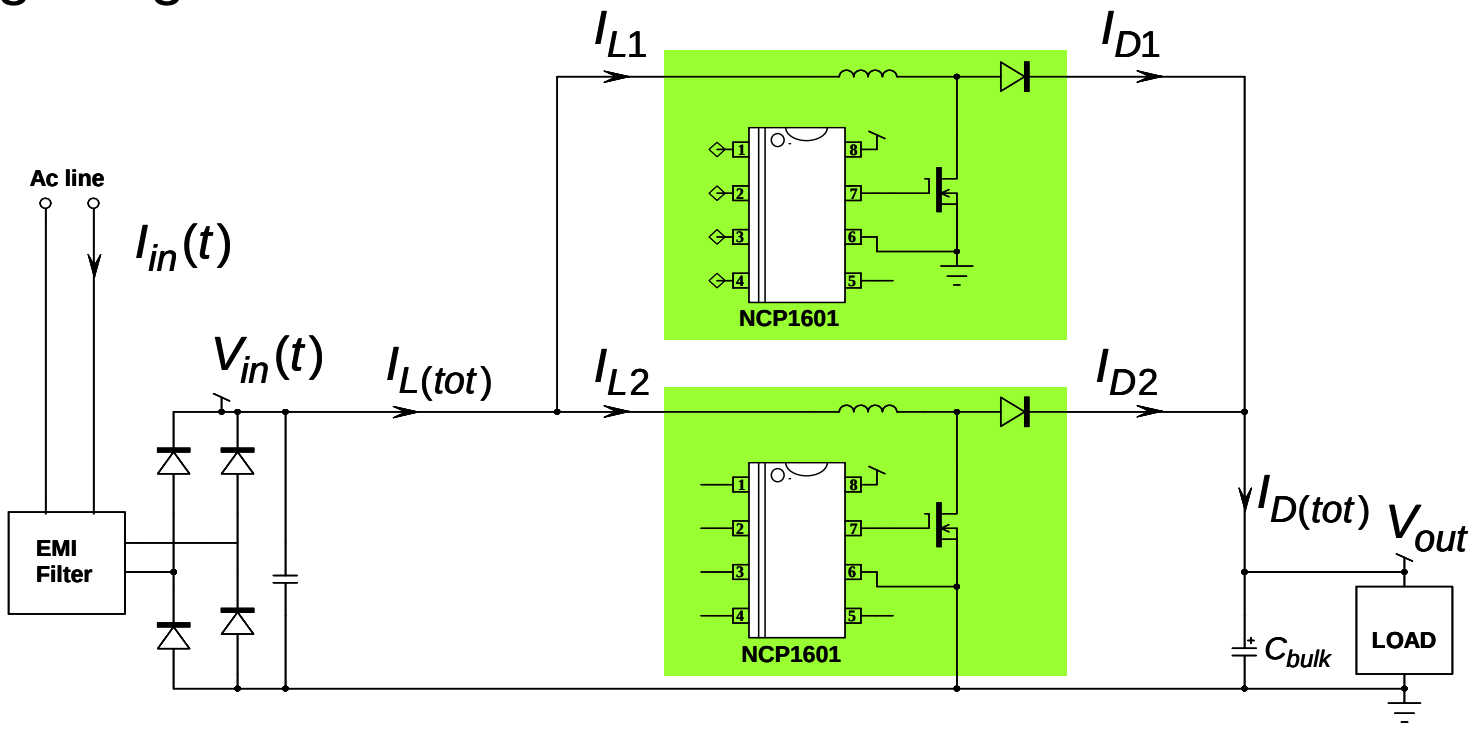
Interleaved PFC

Agenda

- Introduction:
  - Basics of interleaving
  - Main benefits
- NCP1631: a novel controller for interleaved PFC
  - Out-of-phase management
  - The NCP1631 allows the use of smaller inductors
  - Main functions
- Experimental results and performance
  - General waveforms
  - Efficiency
- Conclusion

Interleaved PFC

- Two small PFC stages delivering ($P_{in(avg)}$ / 2) in lieu of a single big one



- If the two phases are out-of-phase, the resulting currents ($I_{L(tot)}$) and ($I_{D(tot)}$) exhibit a dramatically reduced ripple.

Interleaved Benefits

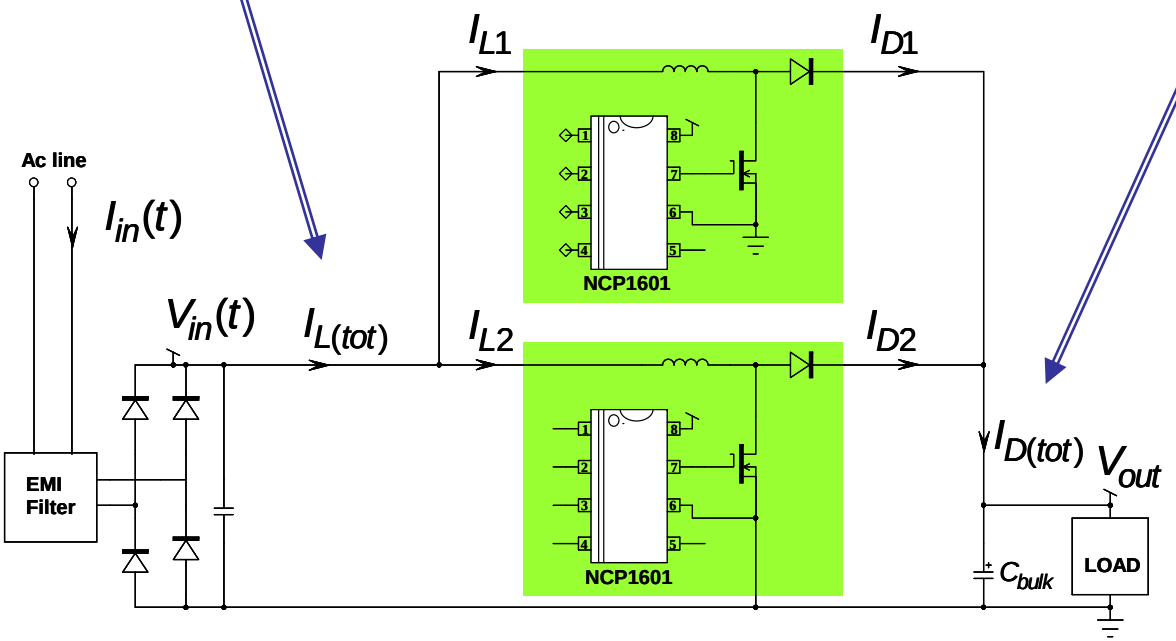
- More components but:
  - A 150 W PFC is easier to design than a 300 W one
  - Modular approach
  - Better heating distribution
  - Extended range for Critical Conduction Mode (CrM)
  - Smaller components

  (help meet strict form factor needs – e.g., flat panels)
  - **Two DCM PFCs look like a CCM PFC converter…**
    - Eases EMI filtering and reduces the output rms current

Input and Output Current

What is the ripple of the $I_{L(tot)}$ total input current?

What is the ripple of the $I_{D(tot)}$ total output current?



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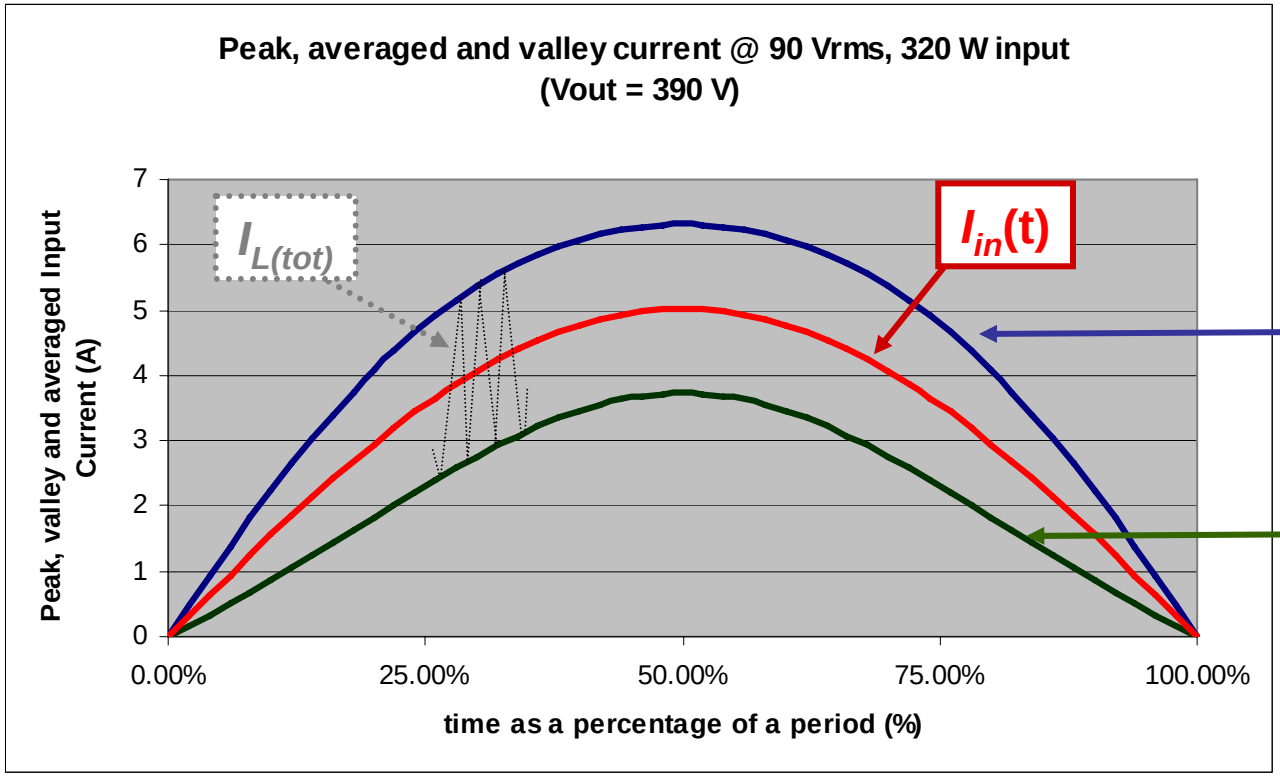
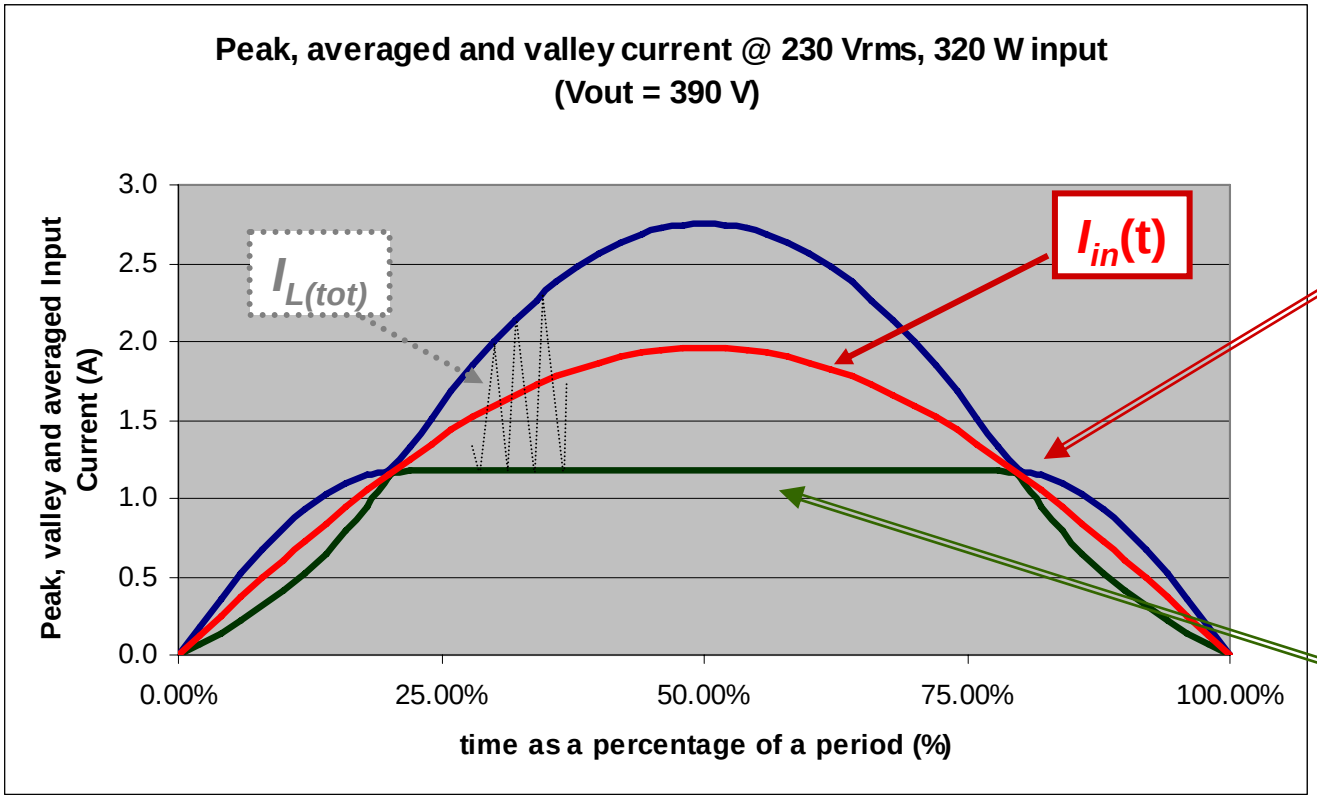
Input Current Ripple at Low Line

- When V_{in} remains lower than $V_{out}/2$, the input current looks like that of a CCM, hysteretic PFC
- ($I_{L(tot)}$) swings between two nearly sinusoidal envelops



Input Current Ripple at High Lline

- When V_{in} exceeds (V_{out} /2), the valley current is constant!
- It equates $\left(\frac{V_{out}}{2 \cdot R_{in}}\right)$ where R_{in} is the PFC input impedance



No ripple when $V_{in} = V_{out} / 2$

$$\frac{P_{in(avg)} \cdot V_{out}}{2 \cdot V_{in(rms)}^{2}} = \frac{V_{out}}{2 \cdot R_{in}}$$

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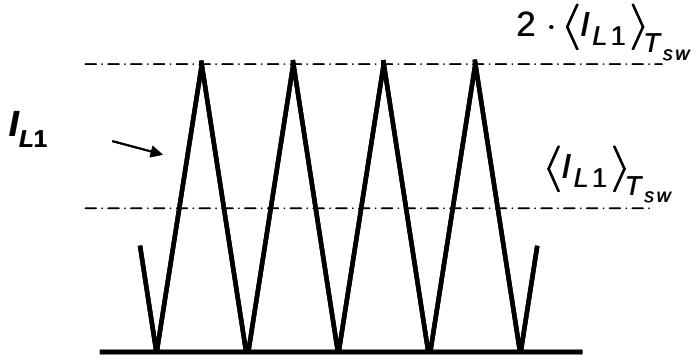
Line Input Current

- For each branch, somewhere within the sinusoid:



- The sum of the two averaged, sinusoidal phases currents gives the total line current:

$$I_{in} = \left\langle I_{L(tot)} \right\rangle_{\frac{T_{sw}}{2}} = \langle I_{L1} \rangle_{T_{sw}} + \langle I_{L2} \rangle_{T_{sw}}$$

- Assuming a perfect current balacing:

$$2 \cdot \langle I_{L1} \rangle_{T_{sw}} = 2 \cdot \langle I_{L2} \rangle_{T_{sw}} = I_{in}$$

- **The peak current in each branch is $I_{in}(t)$**

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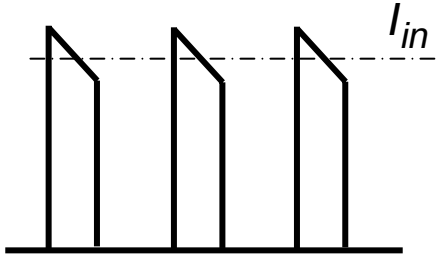
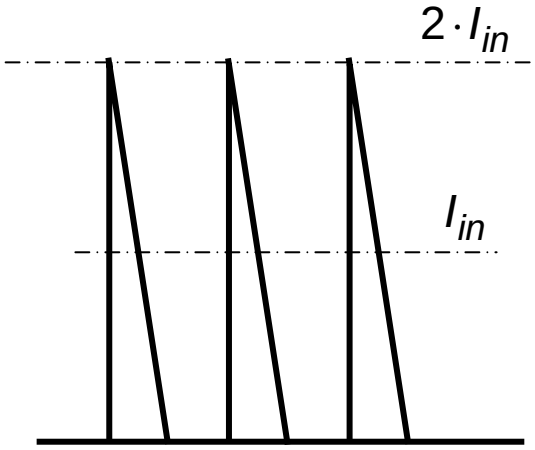
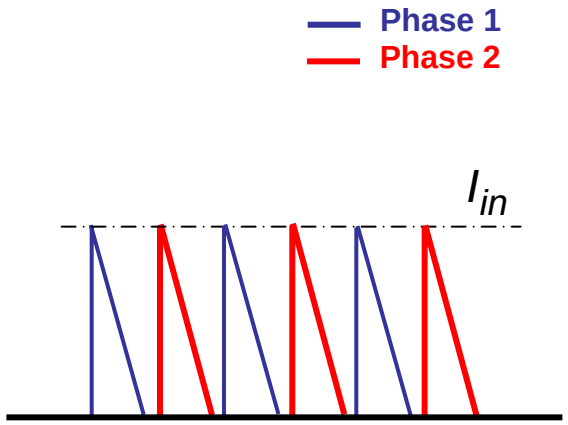
Ac Component of the Refueling Current

- The refueling current (output diode(s) current) depends on the mode:







Single phase CCM

rms value over T_{sw}

$$I_{in} \cdot \sqrt{\frac{V_{in}}{V_{out}}}$$

Single phase CrM

rms value over T_{sw}

$$\frac{2}{\sqrt{3}} \cdot I_{in} \sqrt{\frac{V_{in}}{V_{out}}}$$

Interleaved CrM

rms value over T_{sw}

$$\sqrt{\frac{2}{3}} \cdot I_{in} \sqrt{\frac{V_{in}}{V_{out}}}$$

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A Reduced Rms Current in the Bulk Capacitor

- Integration over the sinusoid leads to (resistive load):

	Single phase CCM PFC	Single phase CrM or FCCrM* PFC	Interleaved CrM or FCCrM* PFC
Diode(s) rms current ($I_{D(rms)}$)	$\sqrt{\frac{8\sqrt{2}\cdot\left(\frac{P_{out}}{\eta}\right)^2}{3\pi\cdot V_{in(rms)}\cdot V_{out}}}$	$\frac{2}{\sqrt{3}}\cdot\sqrt{\frac{8\sqrt{2}\cdot\left(\frac{P_{out}}{\eta}\right)^2}{3\pi\cdot V_{in(rms)}\cdot V_{out}}}$	$\sqrt{\frac{2}{3}}\cdot\sqrt{\frac{8\sqrt{2}\cdot\left(\frac{P_{out}}{\eta}\right)^2}{3\pi\cdot V_{in(rms)}\cdot V_{out}}}$
Capacitor rms current ($I_{C(rms)}$)	$\sqrt{\frac{8\sqrt{2}\cdot\left(\frac{P_{out}}{\eta}\right)^2}{3\pi\cdot V_{in(rms)}\cdot V_{out}}-\left(\frac{P_{out}}{V_{out}}\right)^2}$	$\sqrt{\frac{32\sqrt{2}\cdot\left(\frac{P_{out}}{\eta}\right)^2}{9\pi\cdot V_{in(rms)}\cdot V_{out}}-\left(\frac{P_{out}}{V_{out}}\right)^2}$	$\sqrt{\frac{16\sqrt{2}\cdot\left(\frac{P_{out}}{\eta}\right)^2}{9\pi\cdot V_{in(rms)}\cdot V_{out}}-\left(\frac{P_{out}}{V_{out}}\right)^2}$
300 W, V_{out}=390 V $V_{in(rms)}$=90 V	$I_{D(rms)}$ = 1.9 A $I_{C(rms)}$ = 1.7 A	$I_{D(rms)}$ = 2.2 A $I_{C(rms)}$ = 2.1 A	$I_{D(tot)(rms)}$ = 1.5 A $I_{C(rms)}$ = 1.3 A

- Interleaving dramatically reduces the rms currents

  ➔ **reduced losses, lower heating, increased reliability**

*** Frequency Clamped CrM**

Finally…

- Interleaved PFC combines:
  - The advantages of CrM operations
    - No need for low t_{rr} diode
    - High efficiency
  - A reduced input current ripple and a minimized rms current in the bulk capacitor
  - A better distribution of heating
- More components but “small” ones
- Well adapted to slim form factor applications such as notebook adapters and LCD TVs
- Refer to application note AND8355 for more details

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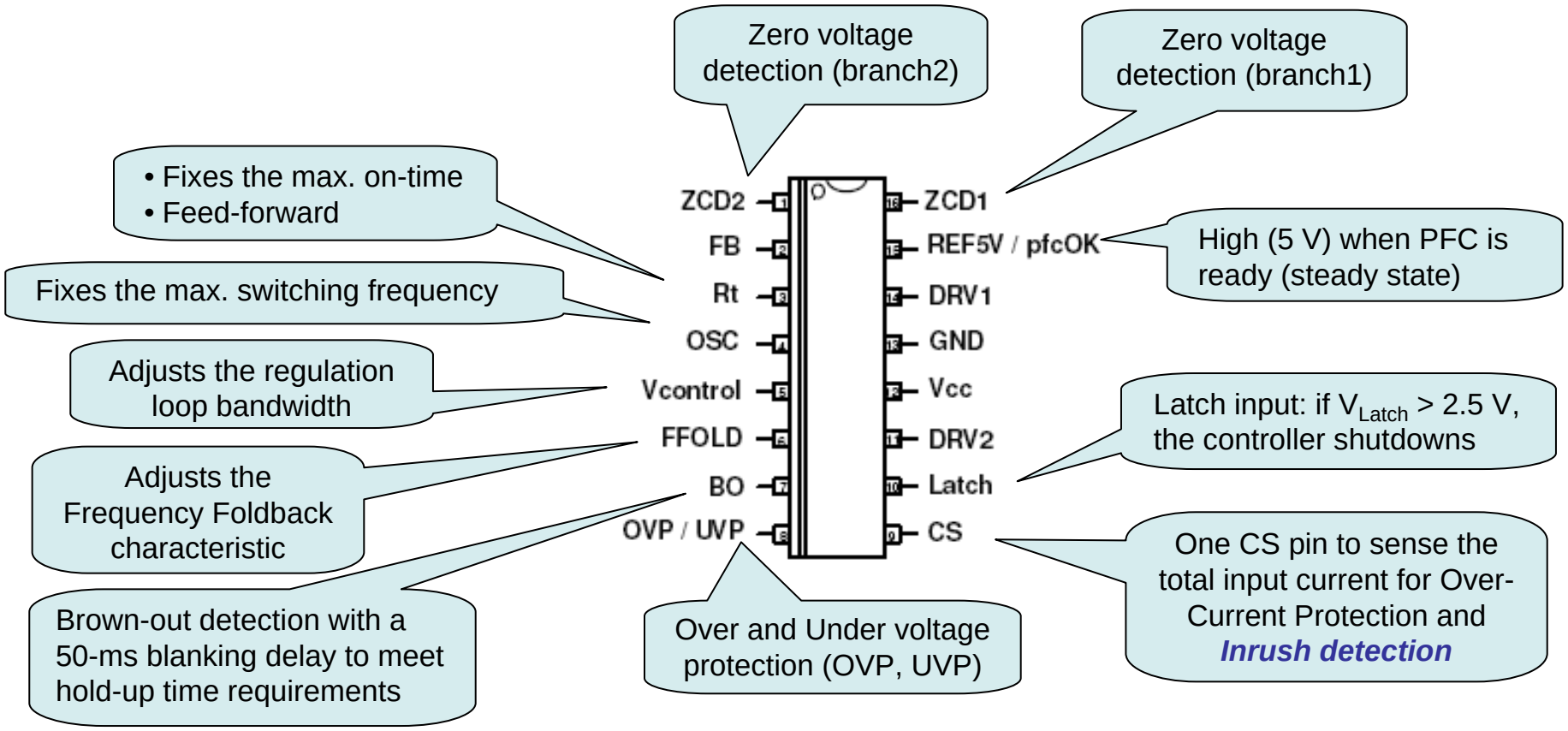
NCP1631 Overview

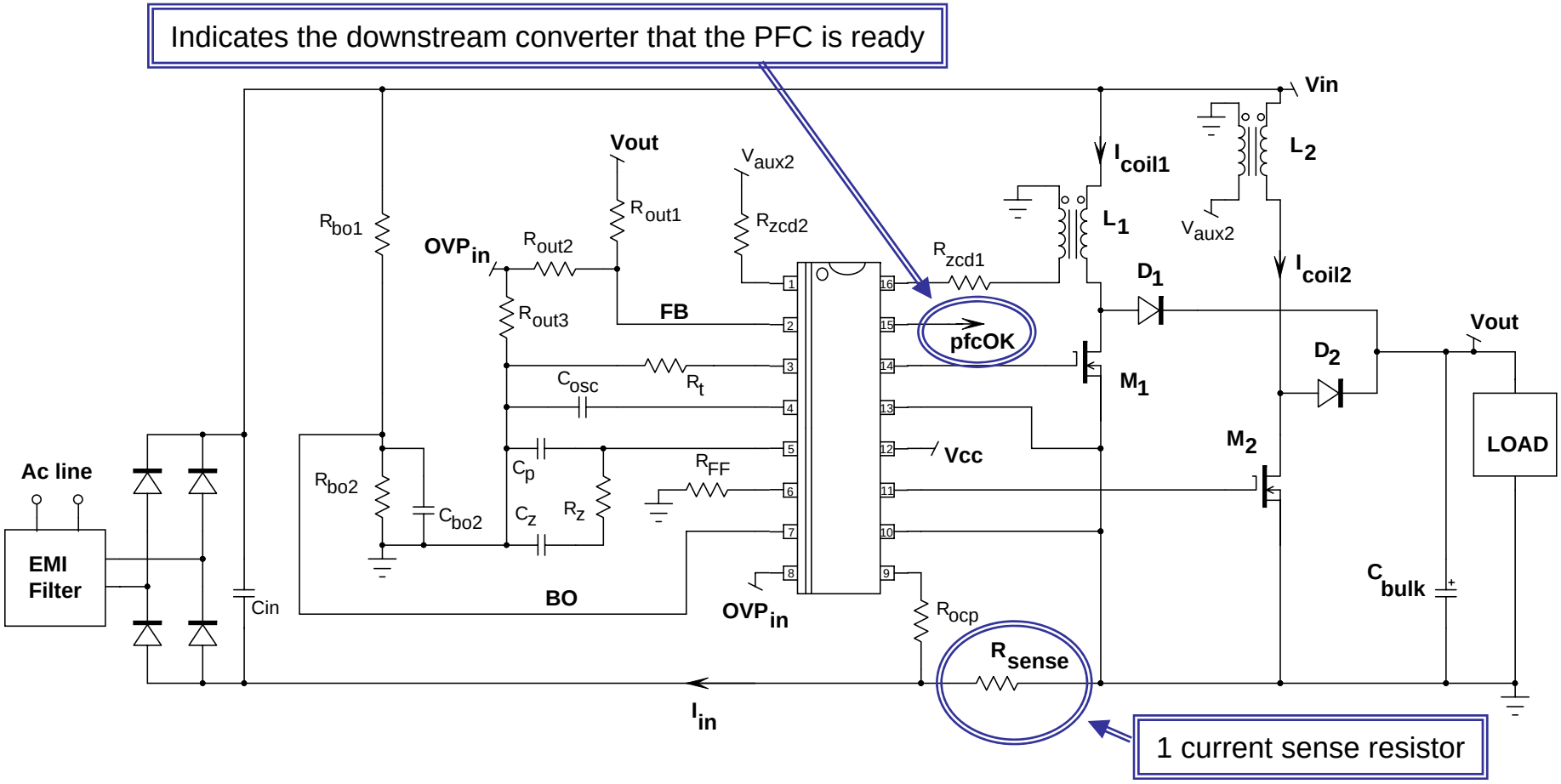
- Interleaved, 2-phase PFC controller
- **F**requency **C**lamped **Cr**itical conduction **M**ode (**FCCrM**) to optimize the efficiency over the load range.
- Substantial out-of-phase operation in all conditions including start-up, OCP or transient sequences.
- Feedforward for improved loop compensation
- Eased design of the downstream converter:
  - pfcOK, dynamic response enhancer, standby management
- High protection level:
  - Brown-out protection, accurate 1-pin current limitation, in-rush currents detection, separate pin for (programmable) OVP…

NCP1631 Overview

- Interleaved, 2-phase PFC controller



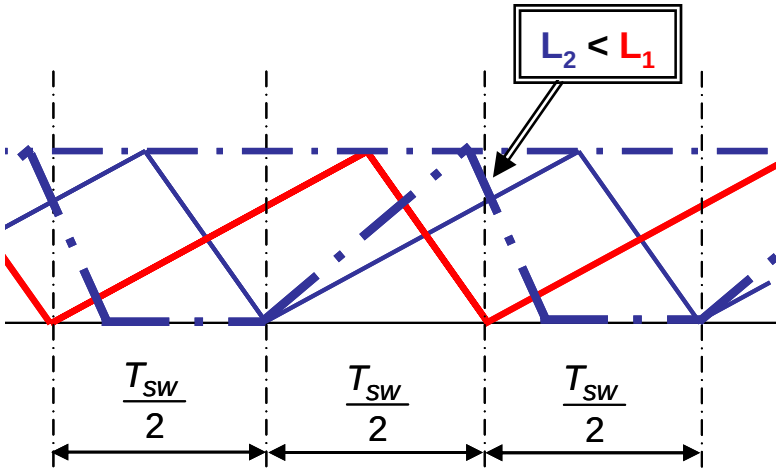
NCP1631 Typical Application



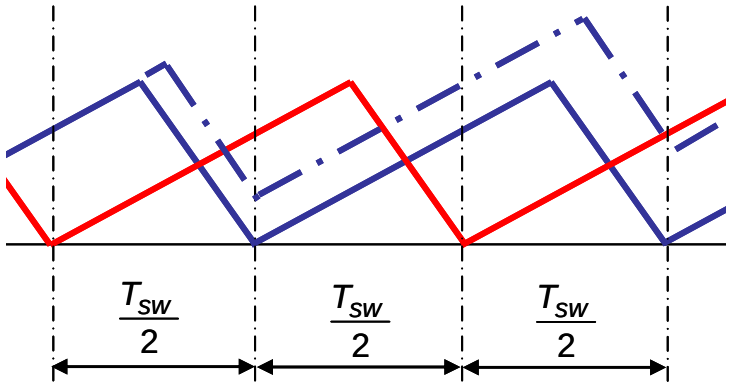
Synchronization of phases is completely internal

Interleaving: Master / Slave Approach…

- The master branch operates freely
- The slave follows with a 180° phase shift
- Main challenge: maintaining the CrM operation (no CCM, no dead-time)



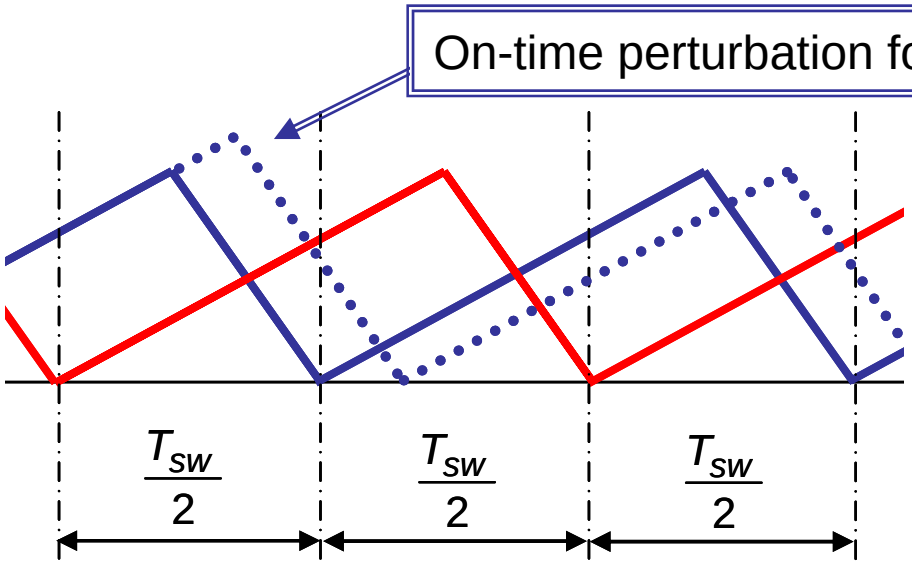
Current mode: inductor unbalance



Voltage mode: on-time shift

Interleaving: Interactive-Phase Approach…

- Each phase properly operates in CrM
- The two branches interact to set the 180° phase shift
- Main challenge: to keep the proper phase shift



CrM operation is maintained but a perturbation of the on-time may degrade the 180° phase shift

- **We selected this approach**

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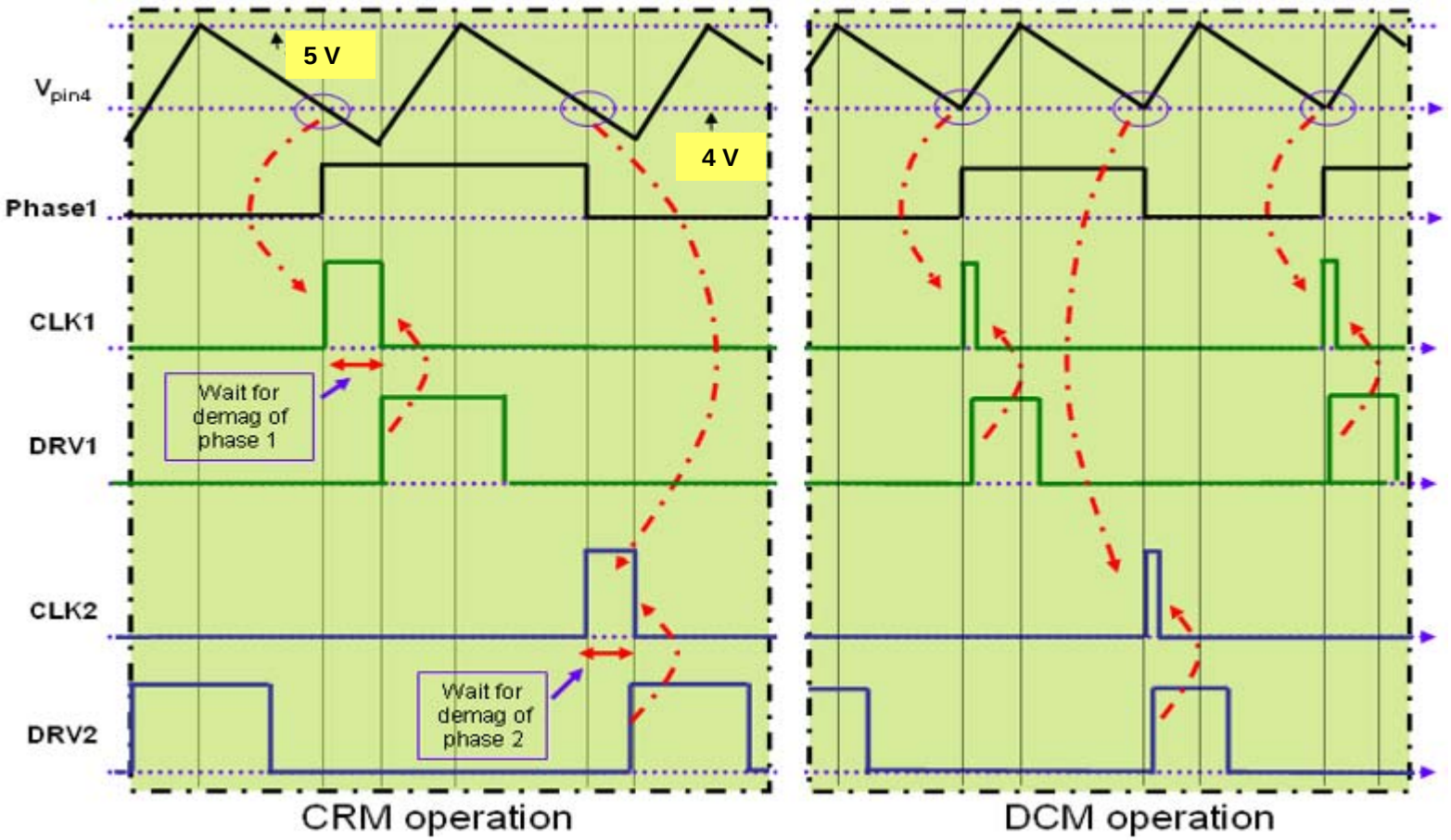
Interleaving Management

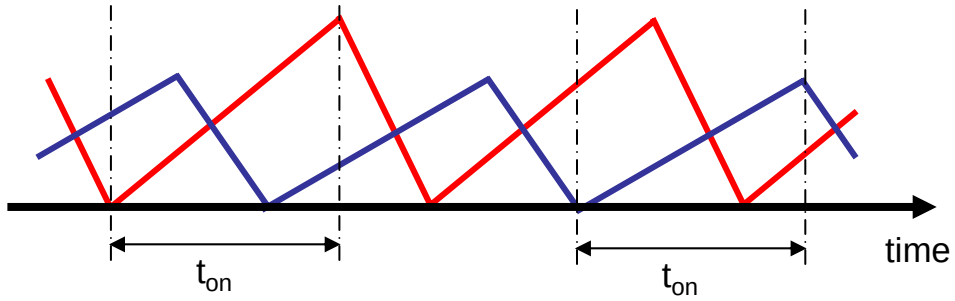
- The oscillator manages the out-of-phase operation
- It acts as the ***interleaved clocks generator***



Current Balancing between the 2 Branches

- The NCP1631 operates in voltage mode
- Same on-time and hence switching period in the two branches
- An imbalance in the inductors:
  - Does not affect the switching period
  - "Only" causes a difference in the power amount conveyed by each branch

$$\frac{I_{in(1)}}{I_{in(2)}} = \frac{L_2}{L_1}$$



$L_1 > L_2$

Phase 1
Phase 2

- The two branches remains synchronized
- CrM operation is kept (or FCCrM)
- No alteration of the 180 degree phase shift

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Artificial Unbalancing

- In this test, the 150 µH inductor of branch 1 is replaced by a 300 µH coil !!!!
- Hence, more current is drawn by branch2 and MOSFET of branch2 is (normally) hotter
- The following plots show how the PFC stage behaves in these extreme conditions and full load

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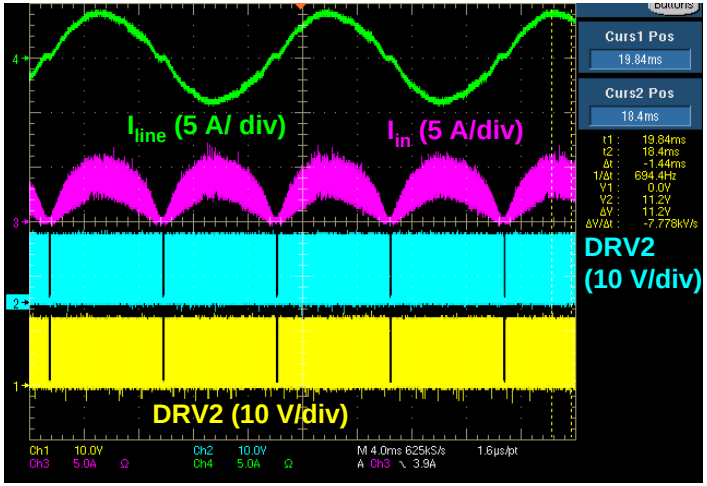
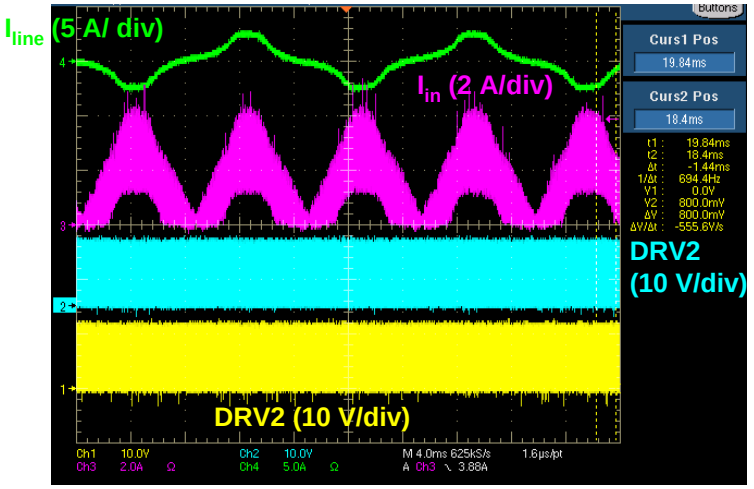
Still Operates in a Robust Manner…

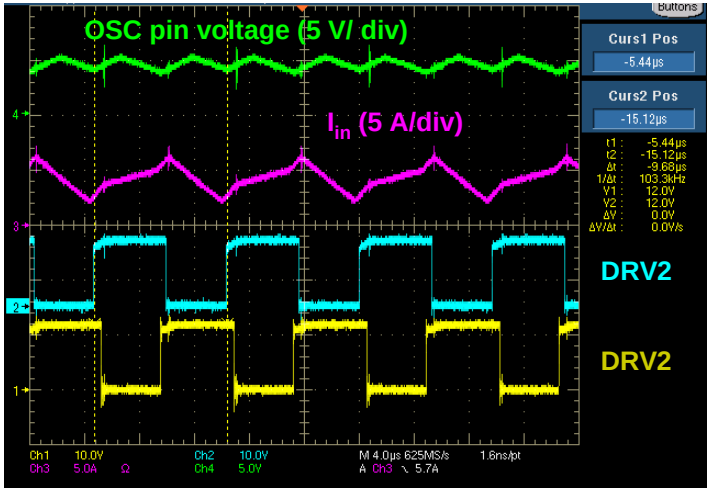
120 Vrms, 0.8 A
(PF = 0.997, THD = 6%)

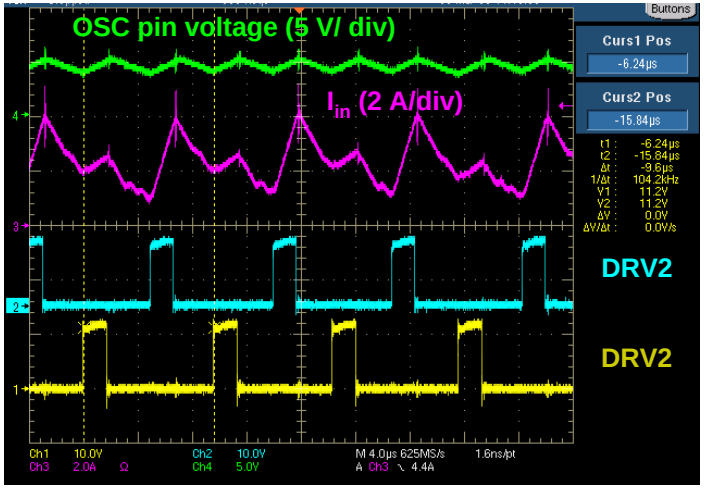


230 Vrms, 0.8 A
(PF = 0.980, THD = 11%)

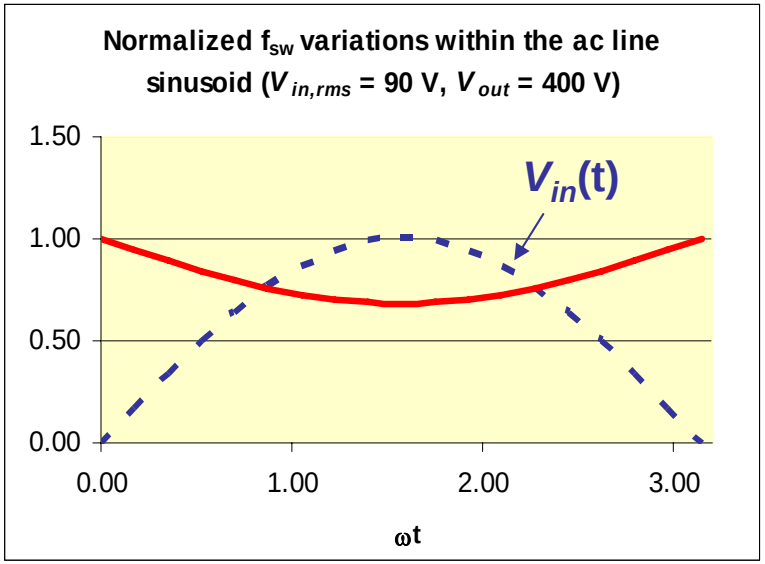


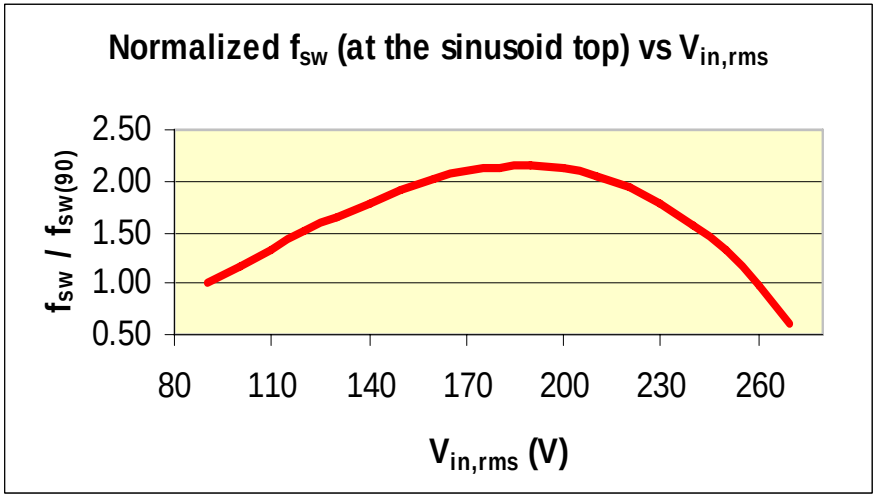
Zoom

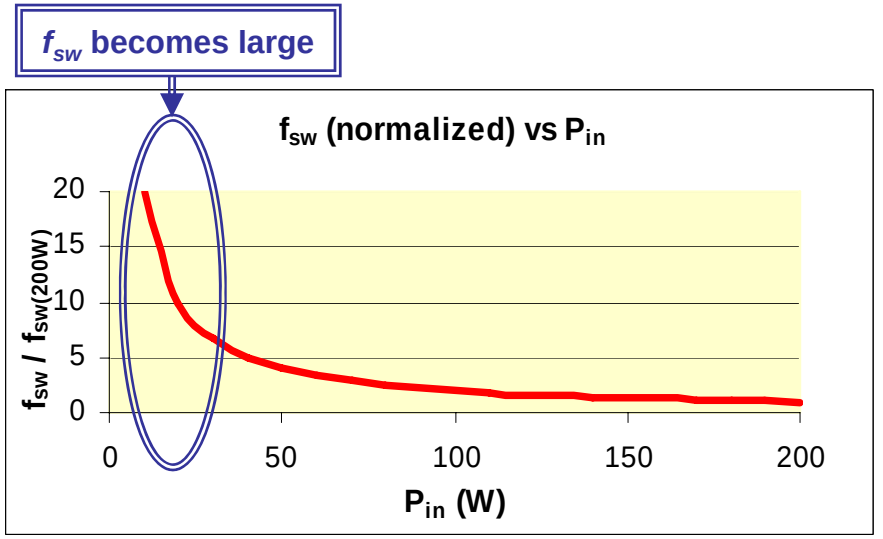




Switching Frequency Variations in CrM







- The switching frequency varies versus the input power, the ac line amplitude and within the sinusoid
- f_{sw} becomes high at light load, leading to large switching losses
- f_{sw} should be limited

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Limiting f_{sw} to Optimize the Efficiency

- At the top of the sinusoid:

$$f_{sw} = \frac{\left(V_{in,pk}\right)^2}{4 \cdot L \cdot P_{in,avg}} \left(1 - \frac{V_{in,pk}}{V_{out}}\right)$$

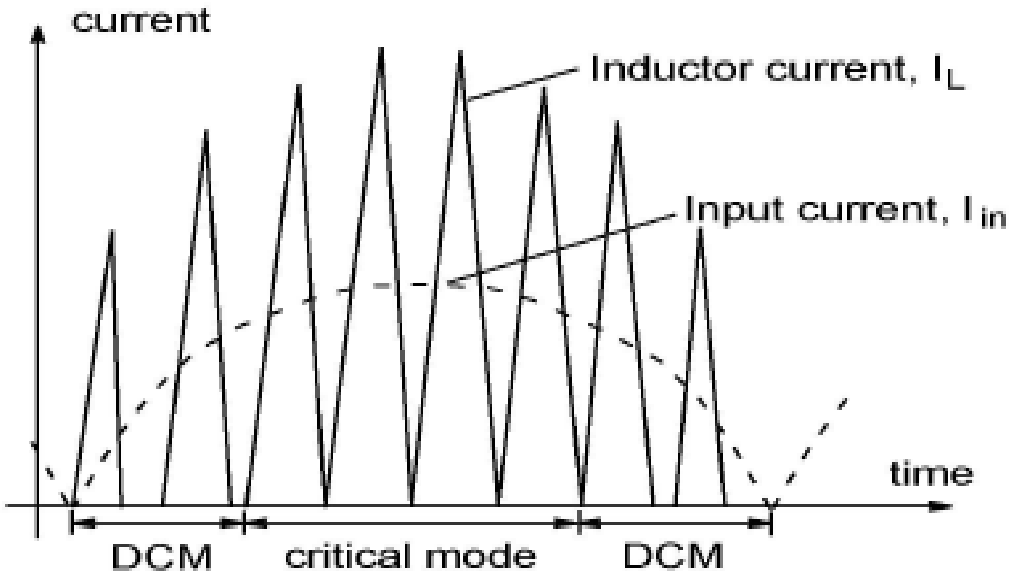
- CrM operation requires large inductors to limit the switching losses at light load

- Can't we clamp f_{sw} not to over-dimension L?

➔ **F**requency **C**lamped **Cr**itical conduction **M**ode **(FCCrM)**

Frequency Clamped Critical Conduction Mode

- At light load, the current cycle is short
- When shorter than the oscillator period, no new cycle until the oscillator period is elapsed ➔ dead-times (DCM)
- On-times are increased to compensate the dead-times ➔ **no PF degradation** (ON proprietary)



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NCP1631 Operation - FCCrM

- In FCCrM, the switching frequency is clamped:
  - Fixed frequency in light load mode and near the line zero crossing
  - Critical conduction mode (CrM) achieved at full load.
- FCCrM optimizes the efficiency over the load range.
- FCCrM reduces the range of frequencies to be filtered (EMI)
- **FCCrM allows the use of smaller inductors**
  - No need for large inductances to limit the frequency range!
  - E.g., 150 µH (PQ2620) for a wide mains 300-W application
- Frequency Foldback reduces the clamp fequency at light load to further improve the efficiency

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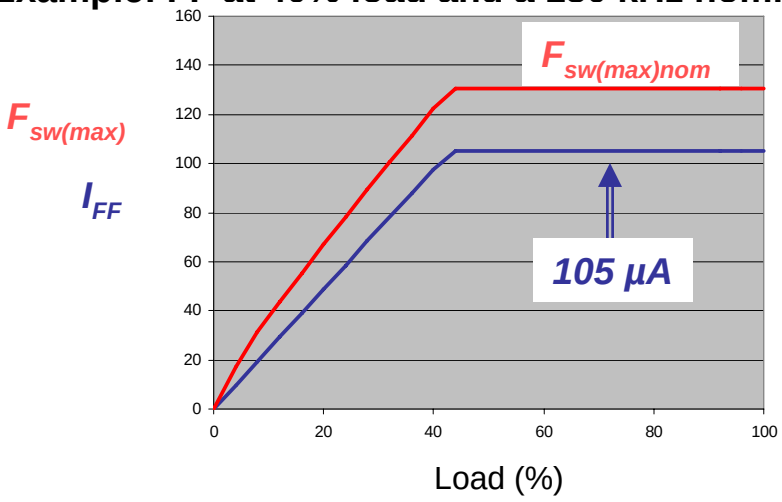
NCP1631 Frequency Foldback

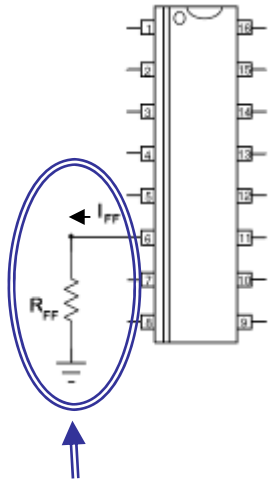
- The clamp frequency ***linearly*** decays when P_{in} goes below a preset level ($\mathbf{P_{LL}}$)
- $\mathbf{P_{LL}}$ is programmed by the pin6 resistor

$$\frac{(P_{in})_{FF}}{(P_{in})_{HL}} = \frac{R_{pin6} \cdot 105\mu A}{1.66} \cong \frac{R_{pin6}}{15810}$$

$(P_{in})_{HL}$ is the max. power deliverable by the PFC stage

Example: FF at 40% load and a 130 kHz nominal frequency

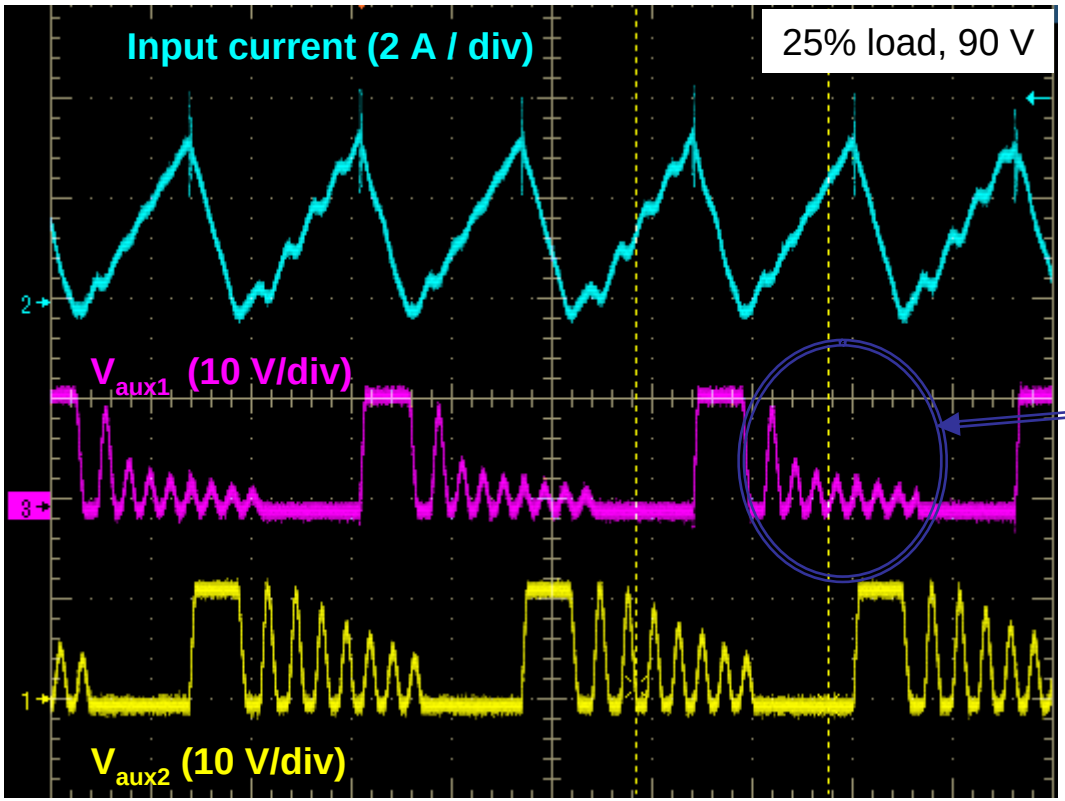




Pin 6 pins out a voltage proportional to the power. The I_{FF} current is clamped to 105µA and used to charge and discharge the oscillator capacitor

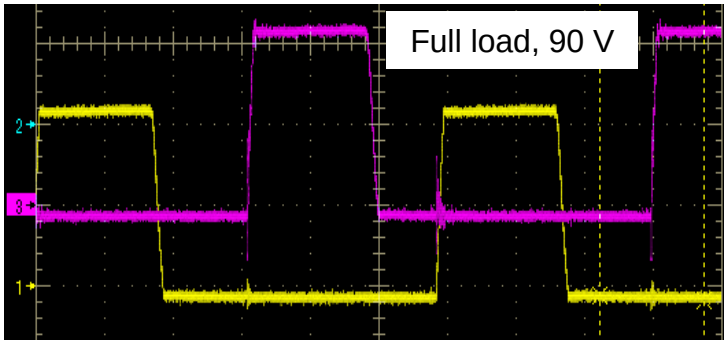
- Gradual decay of the clamp frequency
- **No discontinuity in the operation**
- A resistor across the oscillator capacitor sets a minimum clamp frequency
  (e.g., 20 kHz - see application note AND8407)

Light Load Operation



Frequency is reduced at light load
➔ Heavy DCM operation to reduce the switching losses

Dead-time



CrM at heavy load conditions

No Load Consumption

Conditions	Line Voltage (V)	Input Power (mW)
❑ No Frequency Foldback (pin6 grounded) ❑ 2 separate V_{out} sensing networks for FB and OVP for a total 185-µA leakage on the V_{out} rail	115	107
	230	138
❑ Frequency Foldback (R_{FF} = 4.7 kΩ) ❑ 2 separate V_{out} sensing networks for FB and OVP for a total 185-µA leakage on the V_{out} rail (*)	115	96
	230	134
❑ Frequency Foldback (R_{FF} = 4.7 kΩ) ❑ one V_{out} sensing network for FB and OVP for a total 48-µA leakage on the V_{out} rail	115	38
	230	82

- ❑ Measured on the 300 W NCP1631 demoboard
- ❑ External $\mathbf{V_{cc}}$, 3 * 680 kΩ resistors to discharge the X2 capacitors
- ❑ Frequency Foldback improves the efficiency in light load but also in no-load conditions

(*) Default demoboard configuration

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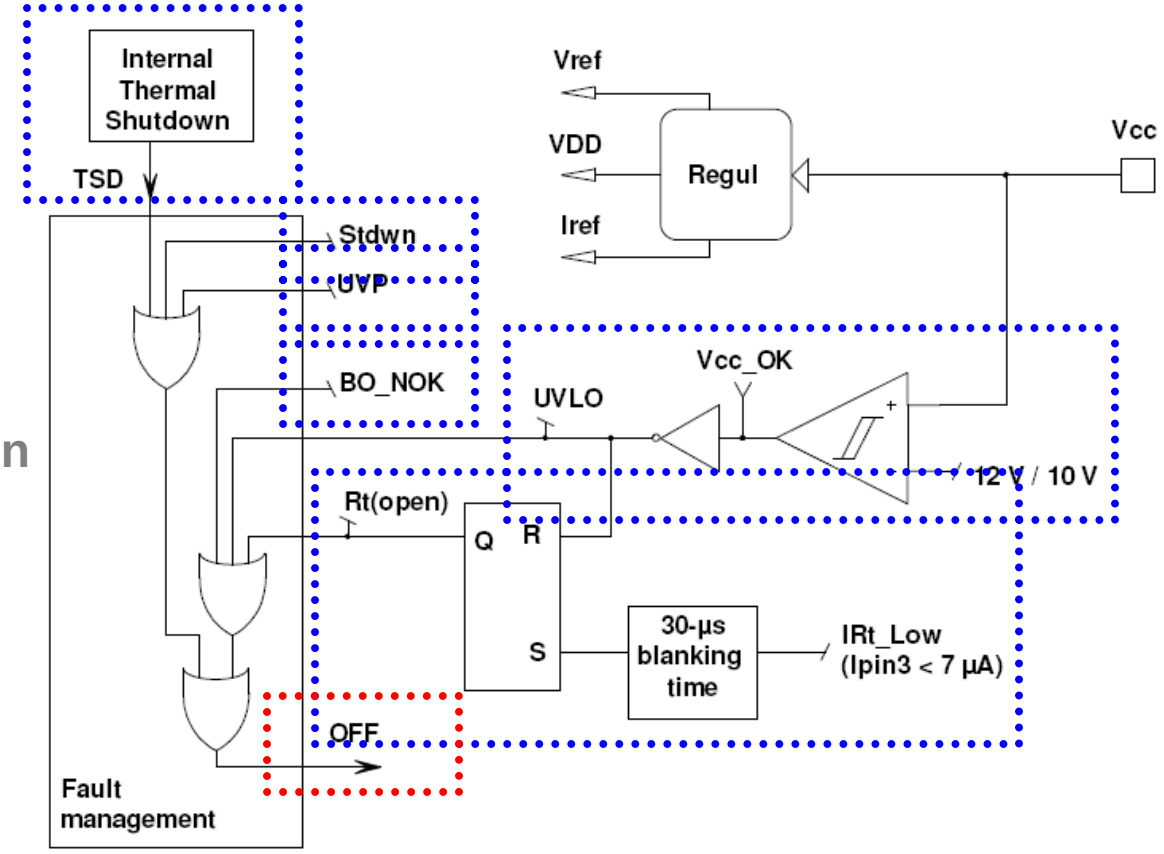
NCP1631 Fault Management

- Brown-out
- Undervoltage protection
- Latch-off condition
- Die overtemperature
- Improper Vcc level for operation
- Too low current sourced by the Rt pin



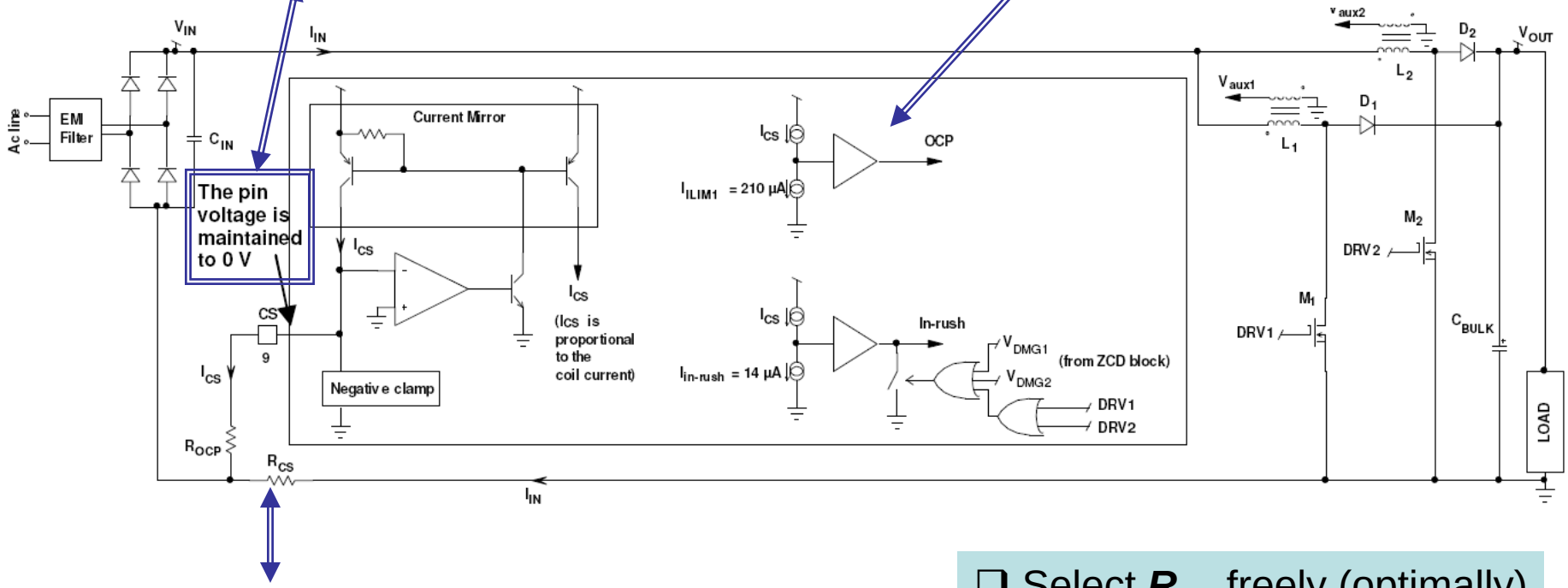
In OFF mode, the major part of the circuit sleeps and consumption is minimized to < 500 µA

NCP1631 Over Current Protection

2) I_{CS} current maintains 0 V on CS pin

$$-(R_{CS}\cdot I_{in})+(R_{OCP}\cdot I_{CS})=0 \;\Rightarrow\; I_{CS}=\frac{R_{CS}}{R_{OCP}}\cdot I_{in}$$

3) If I_{CS} exceeds 210uA, OCP is triggered



1) NCP1631 monitors a negative voltage, V_{CS}, proportional to the current drawn by both interleaved branches, I_{in}.

- ❑ Select R_{CS} freely (optimally)
- ❑ R_{OCP} sets the current limit
- ❑ Minimized losses in R_{CS}

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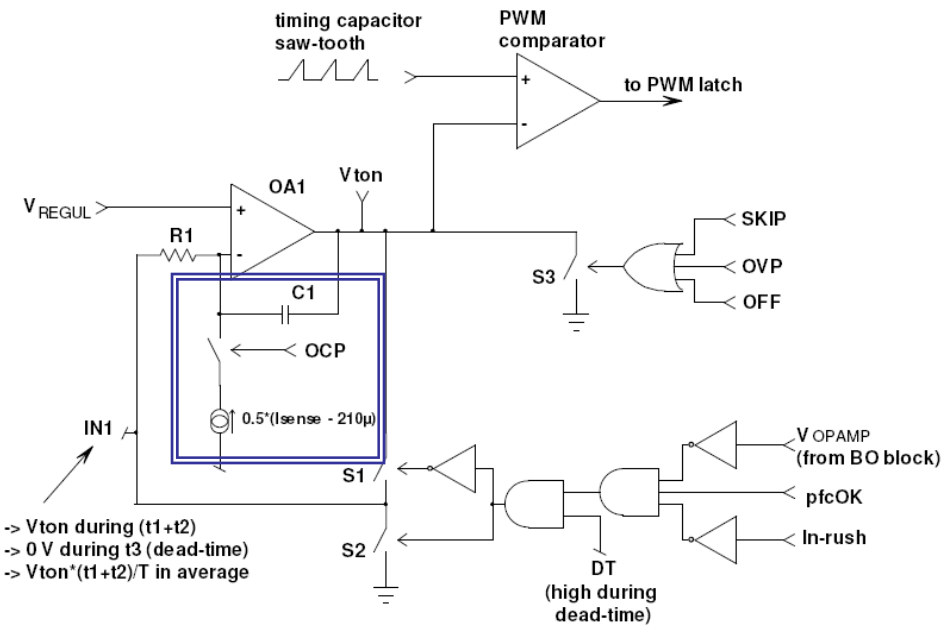
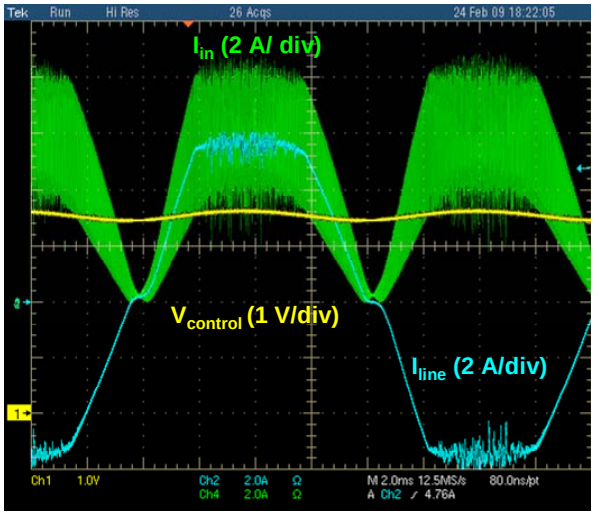
NCP1631 Overcurrent Protection



When I_{CS} > 210 µA, the OCP switch closes and a current equal to 0.5*(I_{CS} – 210 µA) is injected into the negative input of the V_{TON} processing opamp
➔ the on-time sharply reduces proportionally to the magnitude of the over-current event.



- **No discontinuity in the operation, out-of-phase operation is maintained**
- No need for preventing OCP from tripping during a normal transient
- **The current can be accurately limited**

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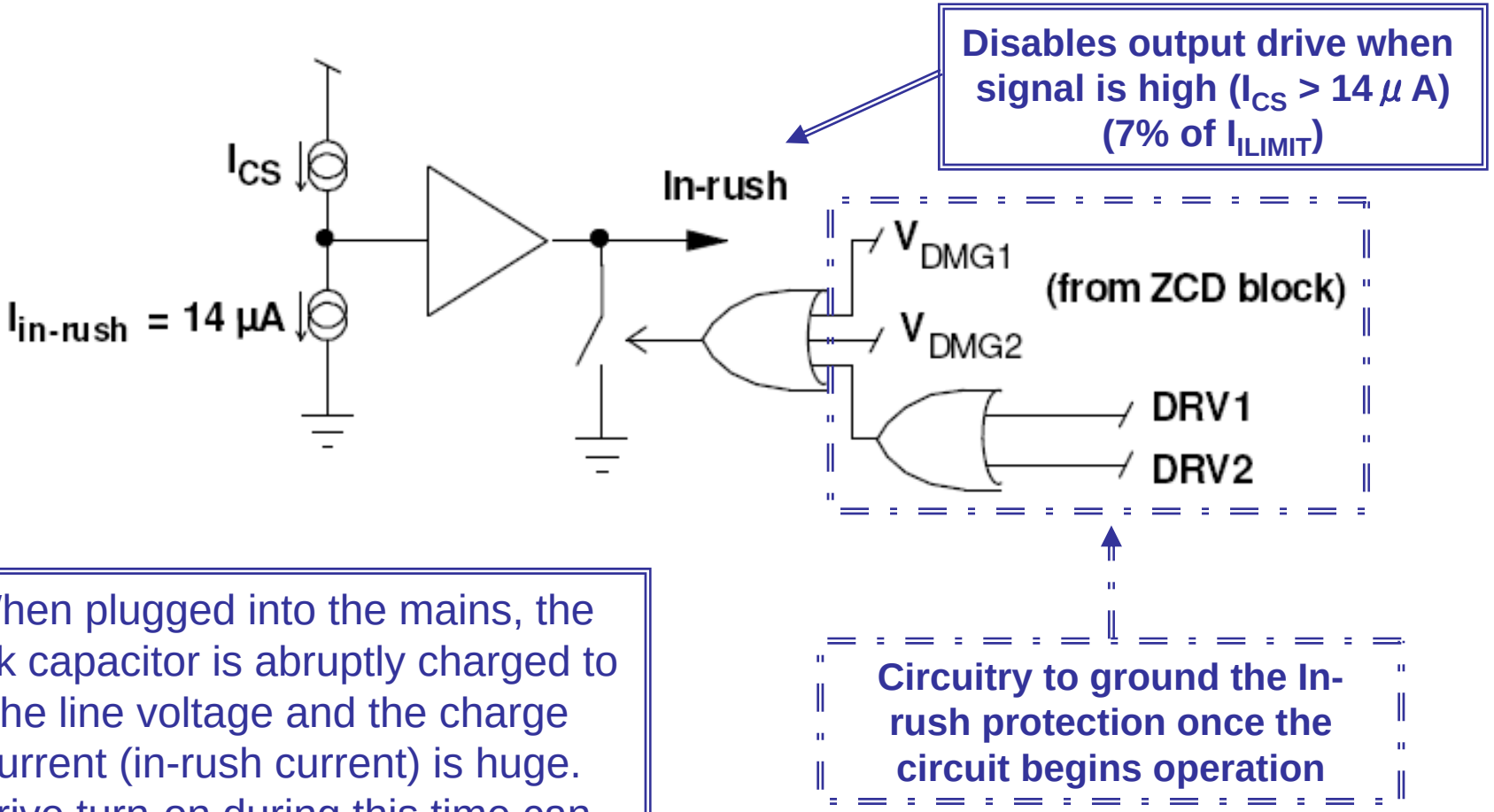
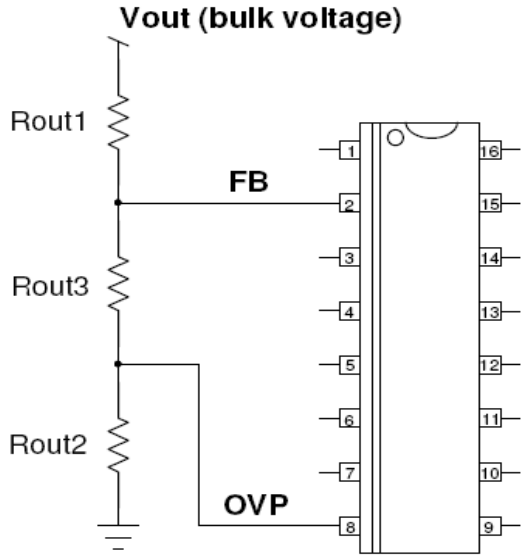
NCP1631 In-rush Current Detection



When plugged into the mains, the bulk capacitor is abruptly charged to the line voltage and the charge current (in-rush current) is huge. Drive turn-on during this time can damage the MOSFETs.

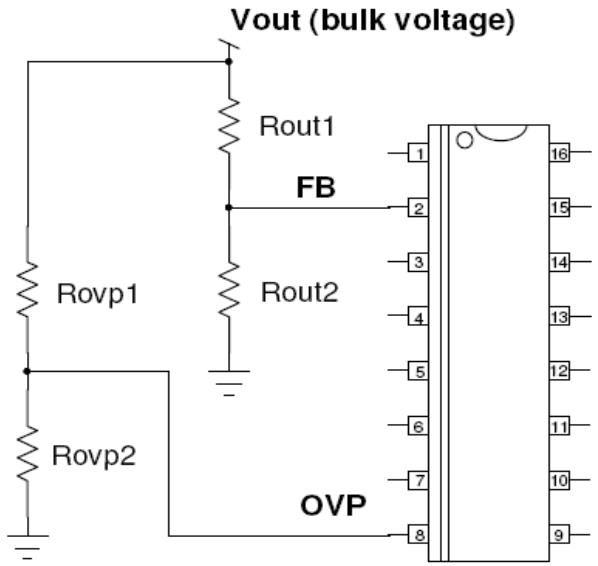
NCP1631 Over Voltage Protection

- Separate pins for FB and OVP (redundancy)
- The two functions share the same 2.5 V internal reference for an eased and accurate setting of the OVP level



Method 1: One feed-back network for OVP and FB

$$\frac{V_{out(ovp)}}{V_{out(nom)}} = 1 + \frac{R_{out3}}{R_{out2}}$$



Method 2: Two separate feed-back networks

$$\frac{V_{out(ovp)}}{V_{out(nom)}} = \frac{R_{ovp1} + R_{ovp2}}{R_{out1} + R_{out2}} \cdot \frac{R_{out2}}{R_{ovp2}}$$

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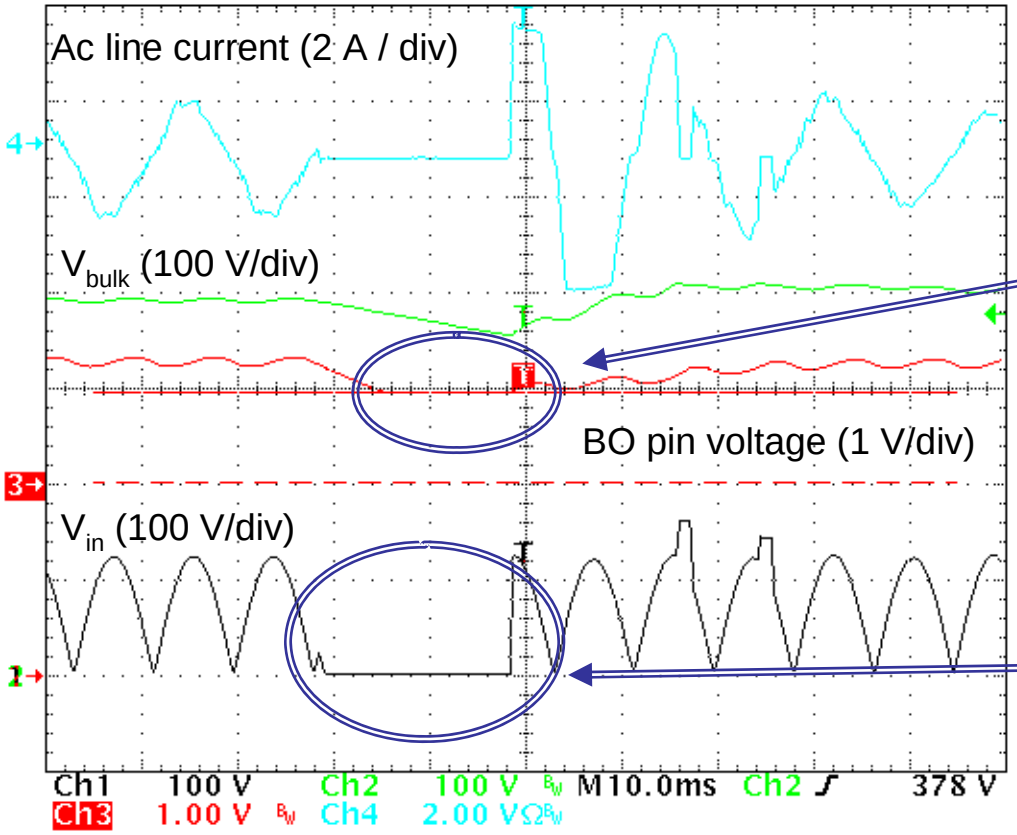
Brown-out Protection with a 50 ms Blanking Time



For the blanking time, the BO pin voltage is maintained around the BO threshold not to delay the circuit restart when the line has recovered

20-ms line interruption

- Mains interruptions shorter than 50 ms are ignored
- The blanking time helps meet hold-up time requirements
- The BO pin voltage serves for feedforward

NCP1631 PfcOK / REF5V Signal

- The pfcOK signal can be used to enable/disable the downstream converter.
- It is high (5 V) when the PFC stage is in normal operation and low otherwise.
- The pfcOK signal is low:
  - Any time the PFC is off because a major fault is detected

  (UVLO condition, thermal shutdown,UVP, Brown-out, Latch-off / shutdown, R_t pin open)
  - For the start-up phase of the PFC stage until the nominal bulk voltage is obtained
- The pfcOK pin can be used as a 5 V power source (5 mA capability)

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NCP1631 Excel Spreadsheet

J. Turchi / August 2009

Please enter your specification			
fac	(Hz)	60	Ac line frequency
VacLL	(V)	90	Ac line rms lowest level (generally 85 V or 90 V in wide mains applications)
VacHL	(V)	265	Ac line rms highest level (generally 265 V in wide or European mains applications)
Vout(nom)	(V)	390	Wished regulation level for the output voltage (generally 390 V or 400 V in wide mains apps)
Vovp	(V)	410	Over-Voltage Protection Level
eff	(%)	94	Expected efficiency at low line, full load - use 94 % as a default value if you don't know
Pout	(W)	300	Maximum output power
Pout(FF)	(W)	150	Output power below which the PFC stage should reduce the switching frequency (frequency Foldback)
Fosc	(kHz)	240	Oscillator frequency (The frequency in each branch of the interleaved PFC is **Fosc/2**)
Rds(on)	(Ω)	0.33	MOSFET on-time resistance @ 25 °C
Thold-up	(ms)	0	Hold-up time. Put 0 if no hold-up time is specified or if you don't know.
(Vout)min	(V)	330	Minimum output Voltage you can accept at the end of the hold-up time - Don't fill this cell or put any value if no hold-up time is specified
%DVpk-pk	(%)	7	Peak to peak low frequency ripple acceptable across the bulk capacitor as a percentage of "Vout(nom)". Choose 7% if you don't know.
Fc	(Hz)	20	Targeted Crossover Frequency

Cells to be filled
Proposed values

Power Components			
Cbulk(min)	(µF)	75	Minimum Cbulk capacitance meeting the low frequency ripple and hold-up time constraints (*)
Cbulk	(µF)	100	Your selection
Lcalc	(µH)	142	Proposed ***minimum*** L1 and L2 inductance not to have a permanent DCM operation in any branch (recommended)
L1, L2	(µH)	150	Your inductance choice. It is recommended to select it higher or equal to "Lcalc"
IL1(max), IL2(max)	(A)	5.0	Maximum current flowing through L1 and L2
IL1(rms), IL2(rms)	(A)	2.0	Maximum rms current in L1 and L2
{Np/Naux}(min)	(-)	15.3	Minimum Turn Ratio (Naux: turns number for auxiliary winding)
Np/Naux	(-)	10.0	Your selected turn ratio
P(bridge)	(W)	6.4	Diode bridge losses assuming a 1-V forward voltage per diode
Pon(L1), Pon(L2)	(W)	2.4	M1 or M2 conduction losses assuming that Rds(on) doubles at the highest junction temperature of your application
P(D1), P(D2)	(W)	0.4	losses in each of the D1 and D2 boost diodes (assuming a 1-V forward voltage)

(*) Do not forget to check that the ESR is low enough to avoid any over-heating of the bulk capacitor. You can use 1.21 A as a starting value for the bulk capacitor rms current (estimation based on AND8355 or AND8407 equation). Doublecheck on the bench that the bulk capacitor heating is not excessive

Brown-Out Circuitry			
VacBOH	(V)	81	
VacBOL	(V)	72	
Fbo / Fac	(%)	10	You can take 10% by default
Cbo_calc	(nF)	225	
Cbo	(nF)	220	Your Cbo choice (standard value close to "Cbo_calc")
Rbo1	(kΩ)	7413	
Rbo2	(kΩ)	120	
Kbo	(%)	1.59	BO scale down factor (for information)

Power Capability Setting			
Rt(min)	(kΩ)	14.0	
Rt	(kΩ)	16.2	Your Rt choice. Select a resistor at least 15% higher for margin
PinHL	(W)	425	Power capability of your PFC stage based on the selected "Rt"

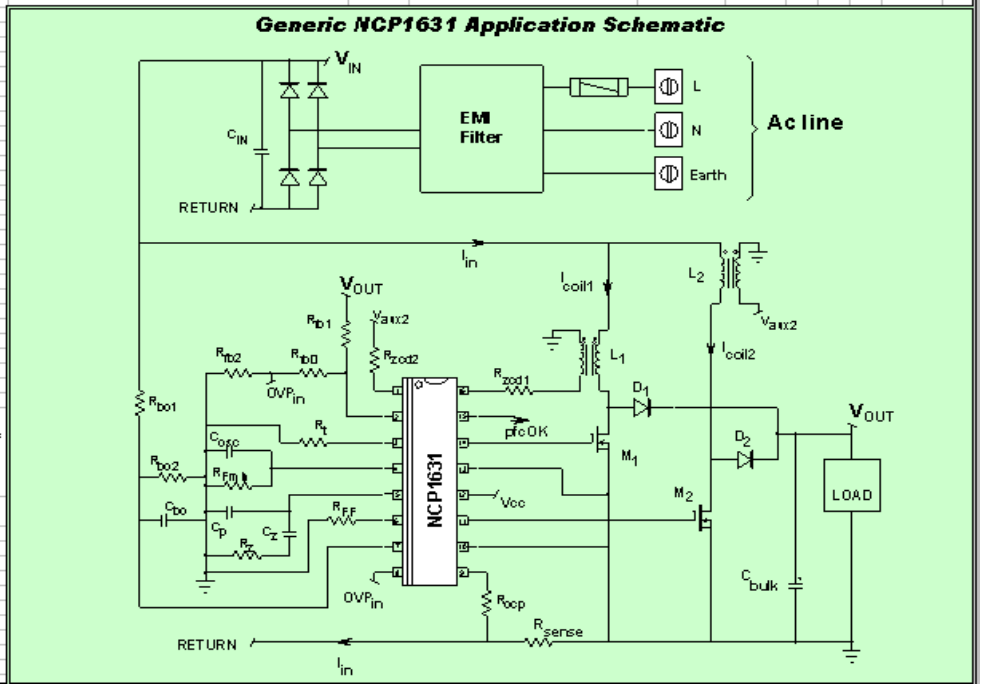
Frequency Control			
Cosc(th)	(pF)	217	
Cosc	(pF)	220	The oscillator capacitor you actually select
Fsw(max)	(kHz)	118	Clamp Frequency in each branch (no Frequency Foldback)
Rff	(kΩ)	7.9	Pin6 resistor
Rfmin	(kΩ)	220	Resistor placed across Cosc to set "Fsw(min)".
Fsw(min)	(kHz)	13.1	Minimum frequency per branch resulting from your "Rfmin" choice

Feed-back and OVP arrangements and Compensation			
Rfb2	(kΩ)	27	You can choose 27 k by default
Rfb0	(kΩ)	1.38	
Rfb1	(kΩ)	4400	
Cp_calc	(nF)	74	
Cp	(nF)	100	The computation of the compensation elements ("xx_calc") targets the specified crossover frequency and 60° as the phase margin **(assymptotic approximation)**
Cz_calc	(µF)	1.11	
Cz	(µF)	1.00	
Rz_calc	(kΩ)	31.8	
Rz	(kΩ)	33.0	
Fc	(Hz)	20.7	Crossover frequency and phase margin resulting from the selected compensation elements **(assymptotic approximation)**
Φm	(°)	53.7	

Current Sense Network			
Iin(max)	(A)	6.3	Maximum input current
Rsense_calc	(mΩ)	51	Value that makes the Rsense dissipation = (0.2% * Pout)
Rsense	(mΩ)	50	Your "Rsense" choice
pRsense	(mW)	560	Losses resulting from your Rsense choice (full load, low line)
Rocp	(kΩ)	1.5	Value resulting from your Rsense choice

ZCD resistors			
Rzcd1(min), Rzcd2(min)	(kΩ)	13	Minimum value of the Rzcd resistor

Generic NCP1631 Application Schematic



- A (simple but easy to use) Excel Spreadsheet (www.onsemi.com) computes the external components

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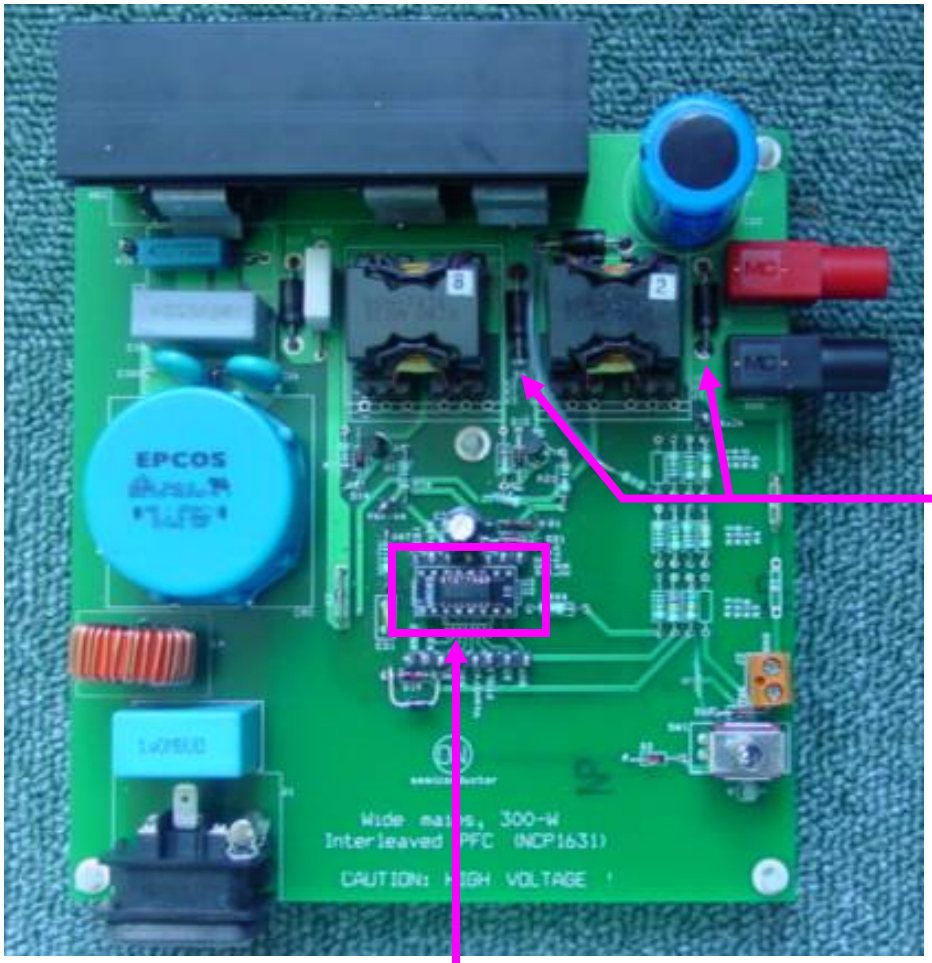
Agenda

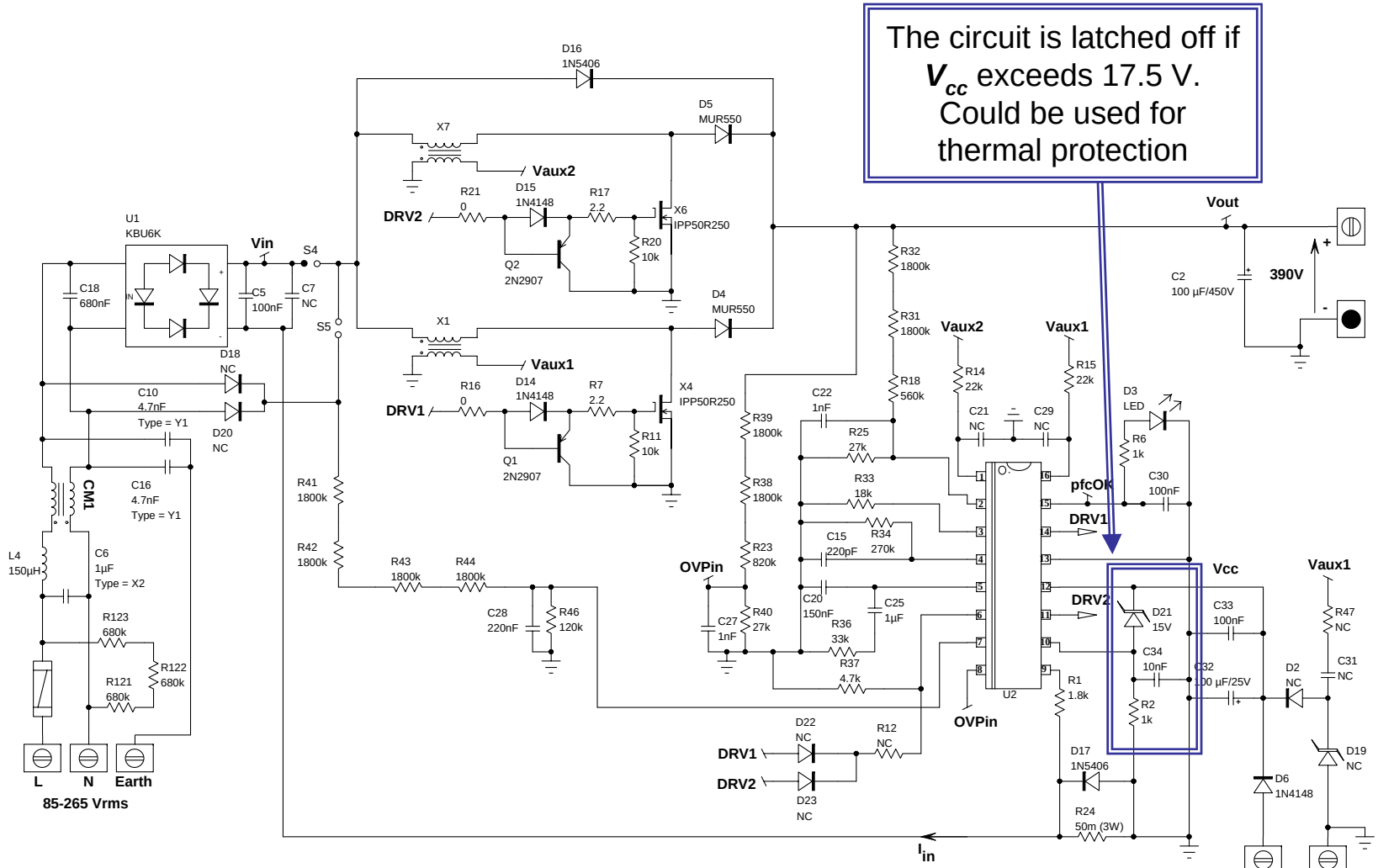
- Introduction:
  - Basics of interleaving
  - Main benefits
- NCP1631: a novel controller for interleaved PFC
  - Out-of-phase management
  - The NCP1631 allows the use of smaller inductors
  - Main functions
- Experimental results and performance
  - General waveforms
  - Efficiency
- Conclusion

NCP1631 Demoboard

Wide mains, 300 W, PFC pre-converter



NCP1631 Demoboard Schematic



300 W, wide mains PFC pre-converter

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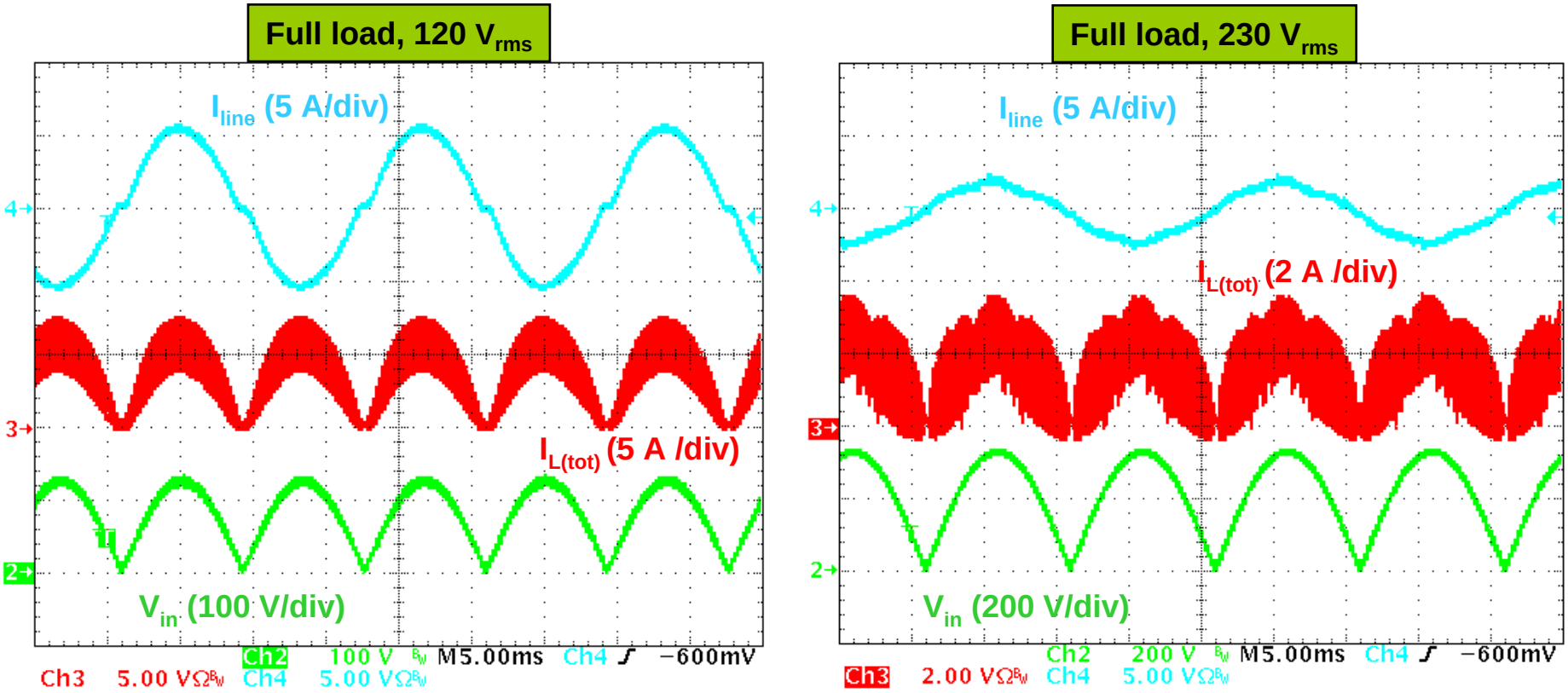
Input Voltage and Current



- ❑ As expected, the input current looks like a CCM one
- ❑ At high line, frequency foldback influences the ripple

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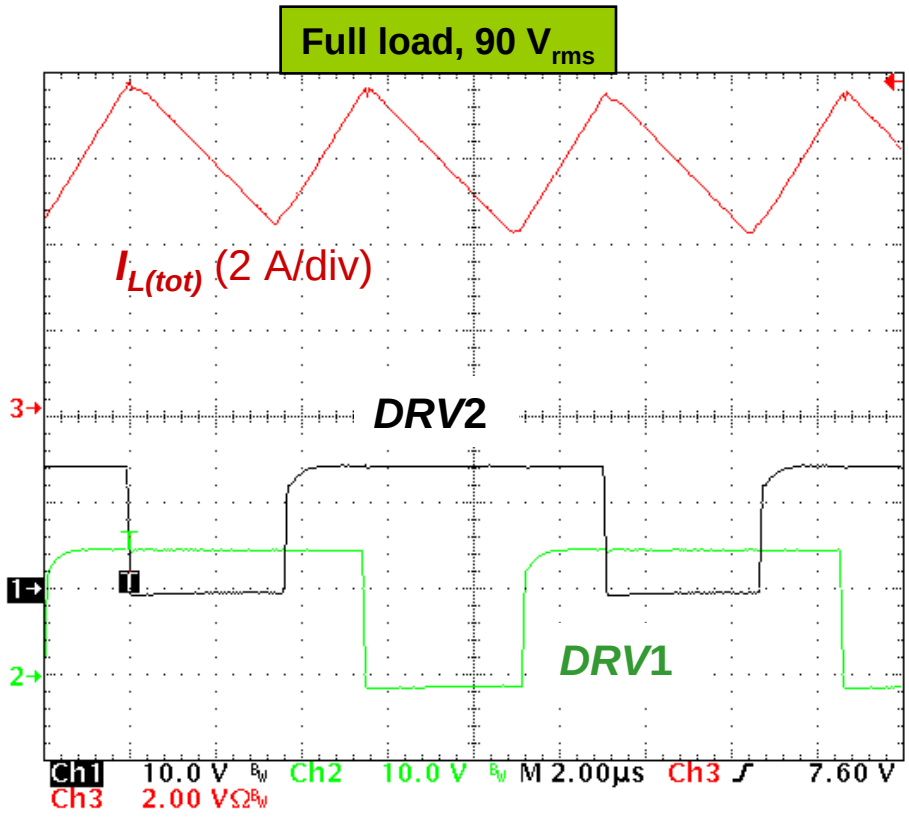
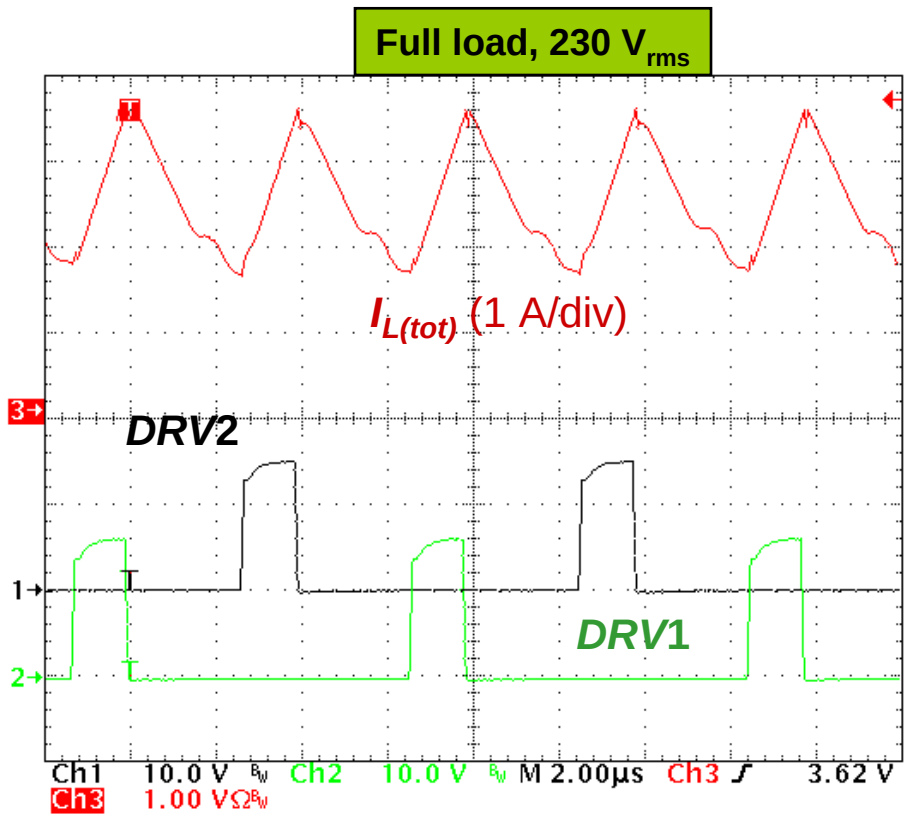
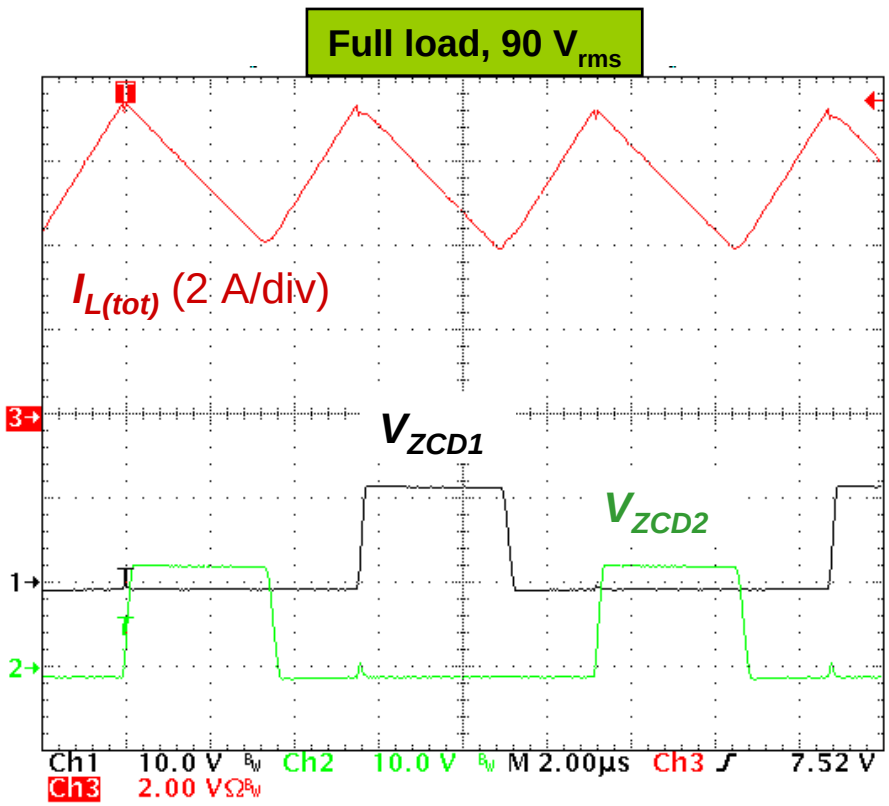
Zoom of the Precedent Plots

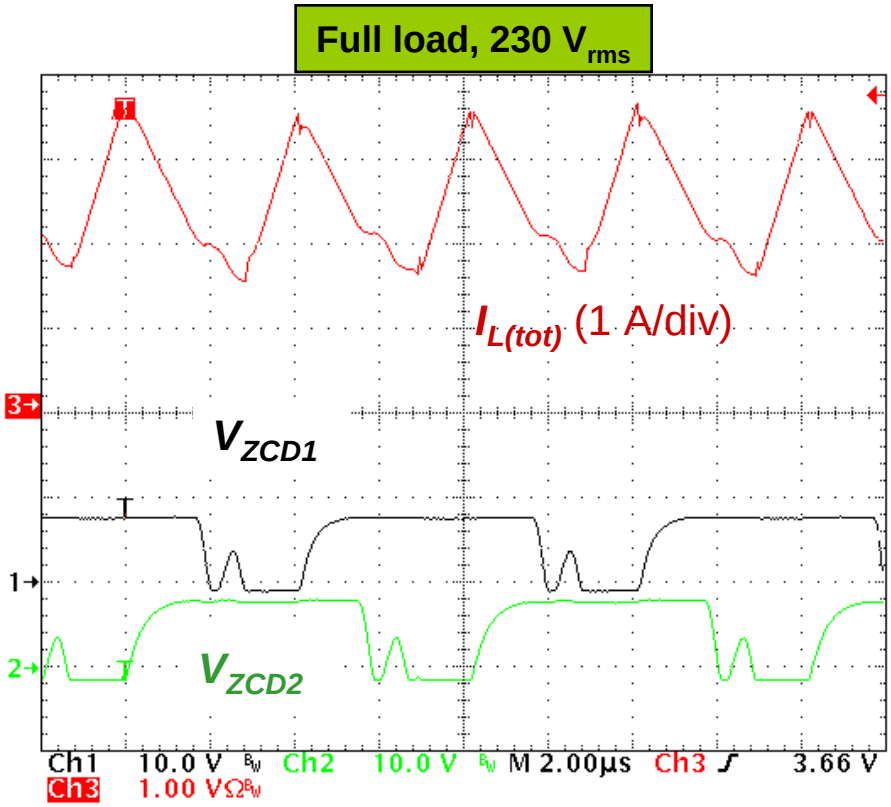




- These plots were obtained at the sinusoid top
- The current swings at twice the frequency of each phase
- At low and high line, the phase shift is substantially 180°

Refueling Sequences





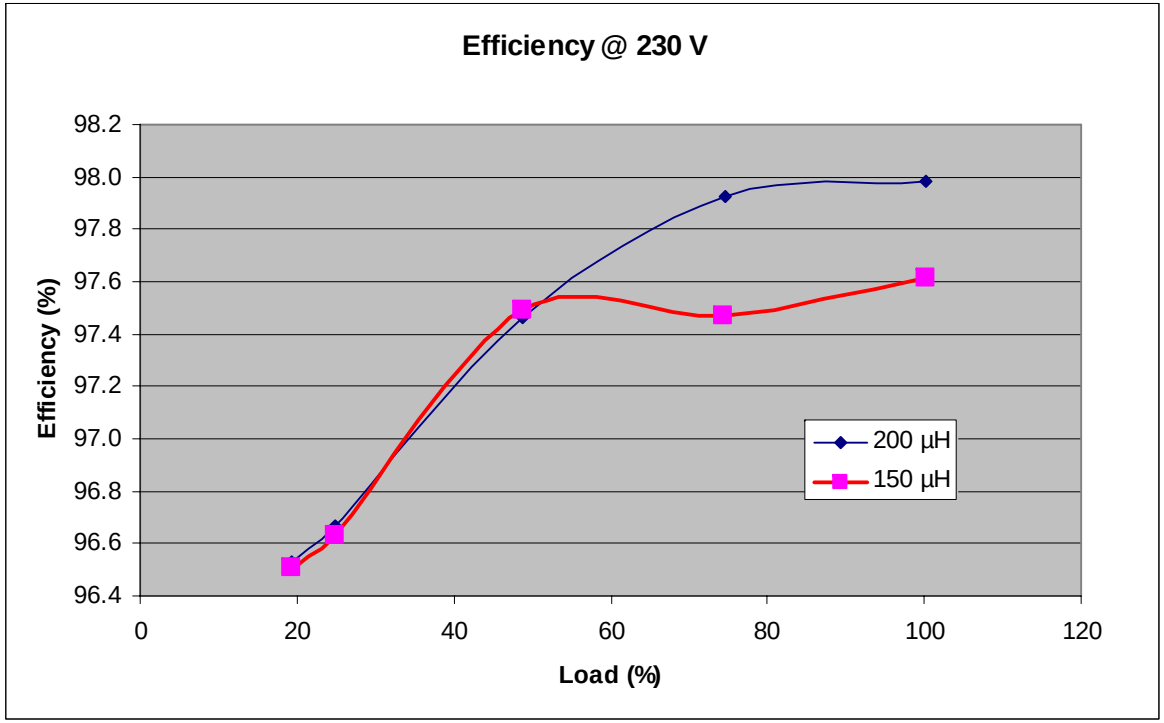
- CrM at low line with valley switching
- Fixed frequency operation at high line (frequency clamp)
- Out-of-phase operation in both cases

Efficiency Measurements

- The output voltage is generally 390 V
- For a 300 W application, the output current is:
  - 770 mA at full load
  - 154 mA at 20% of the load
- Both currents are generally measured with the same tool
- If @ 20% of the load, the input power is 63 W
- 1-mA error in I_{out} leads to
  - I_{out} = 153 mA ➔ Eff = 100 x 390 x 0.153 / 63 = 94.7 %
  - I_{out} = 155 mA ➔ Eff = 100 x 390 x 0.155 / 63 = 95.9 %
- A 1-mA error causes a 1.2% difference in the efficiency!
- Measurements @ 10% and 20% of the load need care!!!

Efficiency Measurements

- The efficiency does not only depend on the control mode
- The inductor, the MOSFETs, diodes, EMI filter… play a role
- For instance, if we compare the efficiency with a 200 µH PQ2625 inductor to that with a 150 µH PQ2620 one:



Frequency Foldback limits the difference at light load

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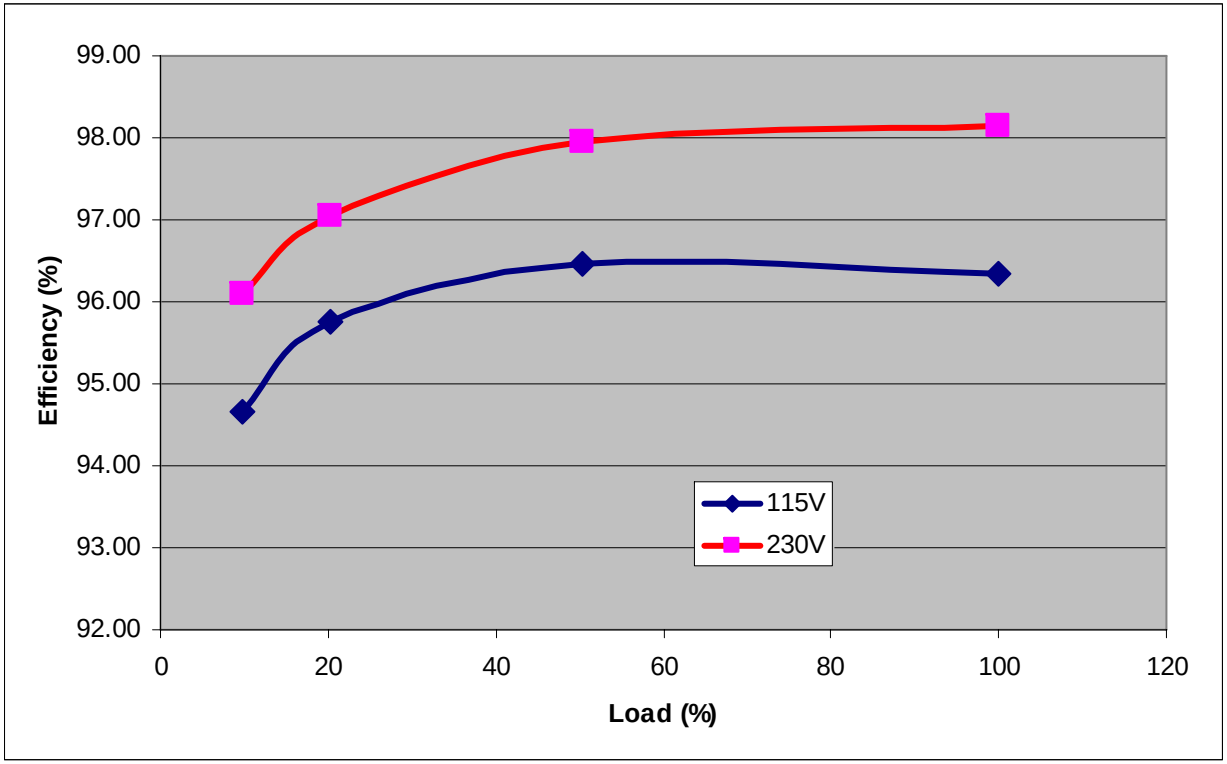
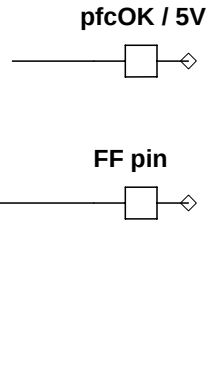
Demoboard Efficiency

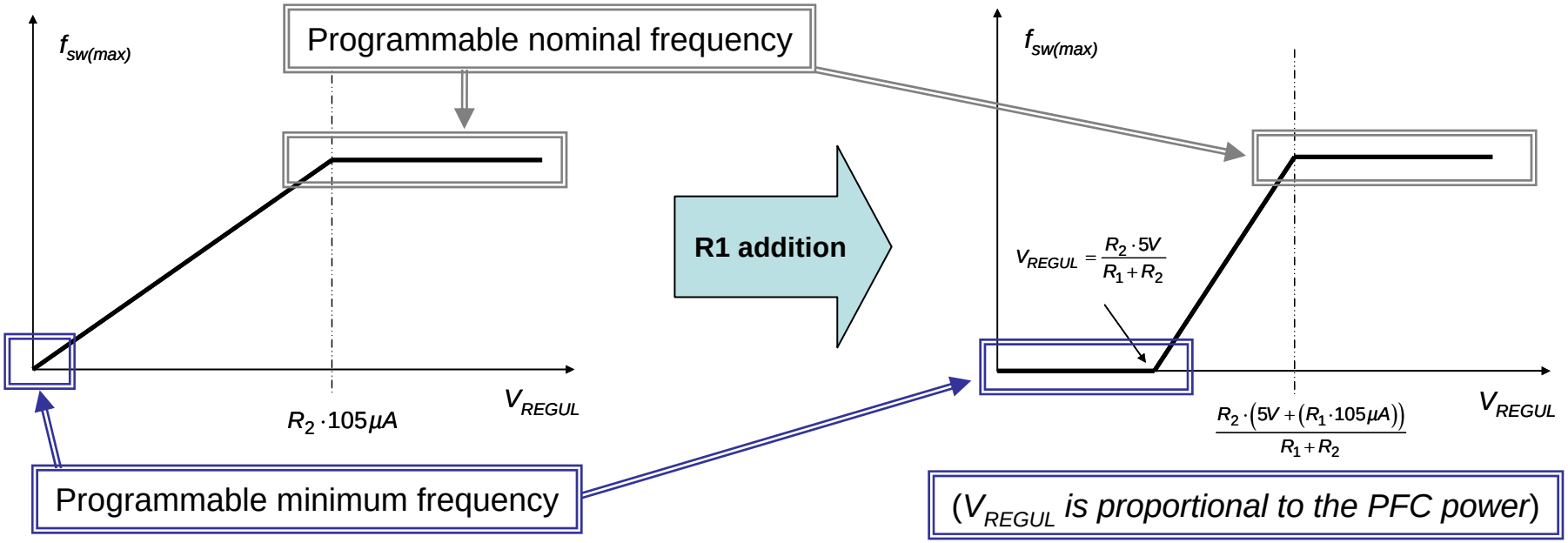


- In the 20% to 100% range, the efficiency remains:
  - > 95.8% at low line
  - > 97.0 % at high line
- Refer to NCP1631EVB/D at www.onsemi.com for details

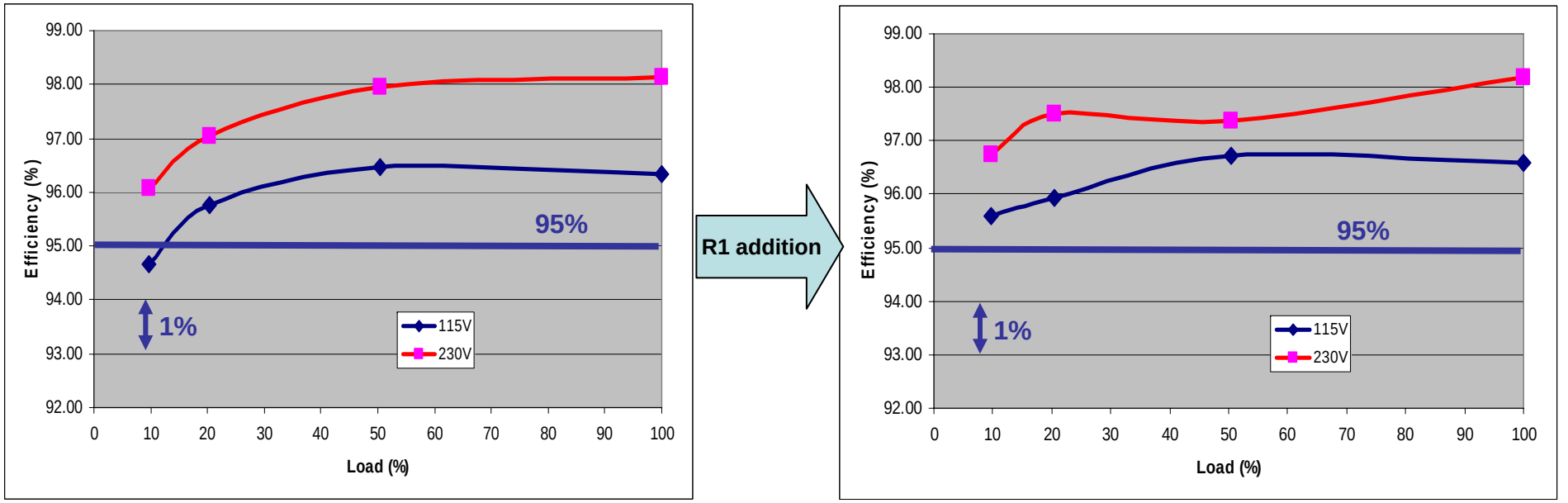
Tweaking Frequency Foldback …

- A resistor can be added between the pfcOK (5 V) and frequency foldback pins
- **Doing so, the frequency clamp decays more sharply:**





Efficiency Improvement



- A resistor on the oscillator pin sets the minimum frequency
- With R_1, the PFC stage operates at the minimum frequency (20 kHz) at 10% and 20% of the load
- The tweak further improves the light load efficiency

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Conclusion

- Interleaved PFC allows use of smaller components, improves thermal performance, increases the CrM power range and reduces current ripple.
- The NCP1631 provides a single IC solution which incorporates all the features necessary for building a robust and compact 2-phase interleaved PFC stage with minimal external components.
- Its FCCrM and frequency foldback allows an efficient operation over the load range with small inductors

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For More Information

- View the extensive portfolio of power management products from ON Semiconductor at www.onsemi.com
- View reference designs, design notes, and other material supporting the design of highly efficient power supplies at www.onsemi.com/powersupplies