

# Dual N- and P-Channel Enhancement Mode Field Effect Transistor

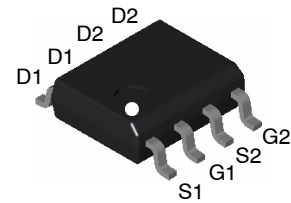
## SI4532DY

### General Description

These dual N- and P-Channel enhancement mode power field effect transistors are produced using onsemi's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

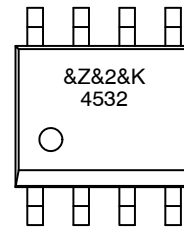
### Features

- N-Channel 3.9 A, 30 V
  - ◆  $R_{DS(ON)} = 0.065 \Omega @ V_{GS} = 10 V$
  - ◆  $R_{DS(ON)} = 0.095 \Omega @ V_{GS} = 4.5 V$
- P-Channel -3.5 A, -30 V
  - ◆  $R_{DS(ON)} = 0.085 \Omega @ V_{GS} = -10 V$
  - ◆  $R_{DS(ON)} = 0.190 \Omega @ V_{GS} = -4.5 V$
- High Density Cell Design for Extremely Low  $R_{DS(ON)}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- Dual (N & P-Channel) MOSFET in Surface Mount Package
- This Device is Pb-Free and Halide Free



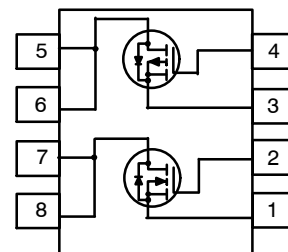
SOIC8  
CASE 751EB

### MARKING DIAGRAM



- &Z = Assembly Site
- &2 = 2-Digit Date Code
- &K = 2-Digits Lot Run Traceability Code
- 4532 = Specific Device Code

### PIN CONNECTION



### ORDERING INFORMATION

Device	Package	Shipping†
SI4532DY	SOIC8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

# SI4532DY

## ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Parameter	N-Channel	P-Channel	Unit
V <sub>DSS</sub>	Drain-Source Voltage	30	-30	V
V <sub>GSS</sub>	Gate-Source Voltage	20	-20	V
I <sub>D</sub>	Drain Current - Continuous (Note 1a)	3.9	-3.5	A
	Drain Current - Pulsed	20	-20	
P <sub>D</sub>	Power Dissipation for Dual Operation	2		W
	Power Dissipation for Single Operation (Note 1a)	1.6		
	(Note 1b)	1		
	(Note 1c)	0.9		
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	-55 to +150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS

Symbol	Characteristic	Value	Unit
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	°C/W
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case (Note 1)	40	°C/W

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Type	Min	Typ	Max	Unit
--------	-----------	----------------	------	-----	-----	-----	------

### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	N-Ch	30	-	-	V
		V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	P-Ch	-30	-	-	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V	N-Ch	-	-	1	μA
		V <sub>DS</sub> = -24 V, V <sub>GS</sub> = 0 V	P-Ch	-	-	-1	
I <sub>GSSF</sub>	Gate-Body Leakage, Forward	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V	All	-	-	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage, Reverse	V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0 V	All	-	-	-100	

### ON CHARACTERISTICS (Note 2)

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	N-Ch	1	-	3	V
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	P-Ch	-1	-	-3	
R <sub>DS(on)</sub>	Static Drain-Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.9 A	N-Ch	-	0.053	0.065	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 3.1 A		-	0.081	0.095	
		V <sub>GS</sub> = -10 V, I <sub>D</sub> = -2.5 A	P-Ch	-	0.06	0.085	
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -1.8 A		-	0.095	0.19	
I <sub>D(on)</sub>	On-State Drain Current	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 5 V	N-Ch	15	-	-	A
		V <sub>GS</sub> = -10 V, V <sub>DS</sub> = -5 V	P-Ch	-15	-	-	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 3.9 A	N-Ch	-	7	-	S
		V <sub>DS</sub> = -15 V, I <sub>D</sub> = -2.5 A	P-Ch	-	5	-	

# SI4532DY

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Type	Min	Typ	Max	Unit
<b>DYNAMIC CHARACTERISTICS</b>							
$C_{iss}$	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	N-Ch	-	235	-	pF
			P-Ch	-	420	-	
$C_{oss}$	Output Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	N-Ch	-	150	-	pF
			P-Ch	-	140	-	
$C_{rss}$	Reverse Transfer Capacitance		N-Ch	-	49	-	pF
			P-Ch	-	60	-	

## SWITCHING CHARACTERISTICS (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 10\text{ V}, I_D = 1\text{ A}, V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$	N-Ch	-	7	13	ns
			P-Ch	-	9	18	
$t_r$	Turn-On Rise Time		N-Ch	-	18	29	ns
			P-Ch	-	8	16	
$t_{d(off)}$	Turn-Off Delay Time	$V_{DD} = -10\text{ V}, I_D = -2.5\text{ A}, V_{GS} = -10\text{ V}, R_{GEN} = 6\ \Omega$	N-Ch	-	15	27	ns
			P-Ch	-	18	29	
$t_f$	Turn-Off Fall Time		N-Ch	-	0.8	8	ns
			P-Ch	-	6	12	
$t_{rr}$	Drain-Source Reverse Recovery Time	$I_F = 1.7\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$ $I_F = -1.7\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	N-Ch	-	-	80	ns
			P-Ch	-	-	80	
$Q_g$	Total Gate Charge	$V_{DS} = 10\text{ V}, I_D = 3.9\text{ A}, V_{GS} = 10\text{ V}$	N-Ch	-	3.7	15	nC
			P-Ch	-	5	15	
$Q_{gs}$	Gate-Source Charge	$V_{DS} = -10\text{ V}, I_D = -2.5\text{ A}, V_{GS} = -10\text{ V}$	N-Ch	-	0.9	-	nC
			P-Ch	-	1.7	-	
$Q_{gd}$	Gate-Drain Charge		N-Ch	-	1.9	-	nC
			P-Ch	-	1.8	-	

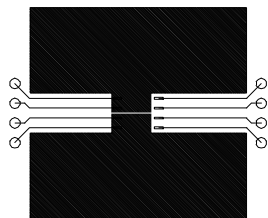
## DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

$I_S$	Maximum Continuous Drain-Source Diode Forward Current		N-Ch	-	-	1.7	A
			P-Ch	-	-	-1.7	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.7\text{ A}$ (Note 2)	N-Ch	-	0.75	1.2	V
			P-Ch	-	-0.75	-1.2	

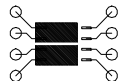
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

### NOTES:

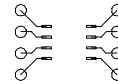
- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $78^\circ\text{C}/\text{W}$  when mounted on a  $0.05\text{ in}^2$  pad of 2 oz copper.



b)  $125^\circ\text{C}/\text{W}$  when mounted on a  $0.02\text{ in}^2$  pad of 2 oz copper.



c)  $135^\circ\text{C}/\text{W}$  when mounted on a minimum mounting pad.

- Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$

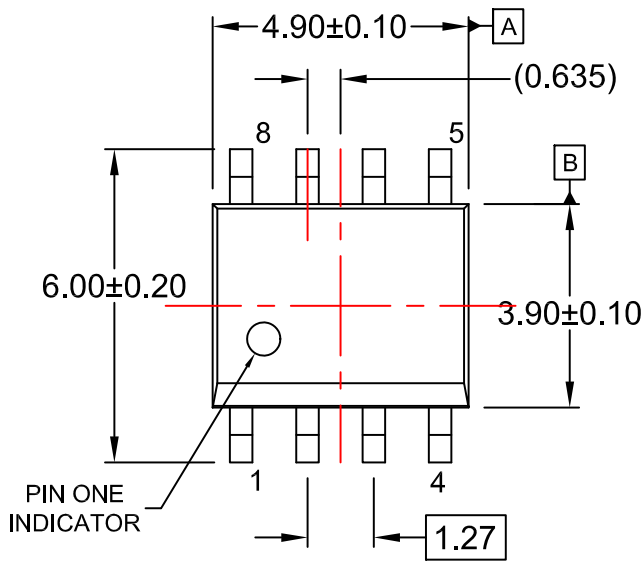
**MECHANICAL CASE OUTLINE**  
**PACKAGE DIMENSIONS**

ON Semiconductor®

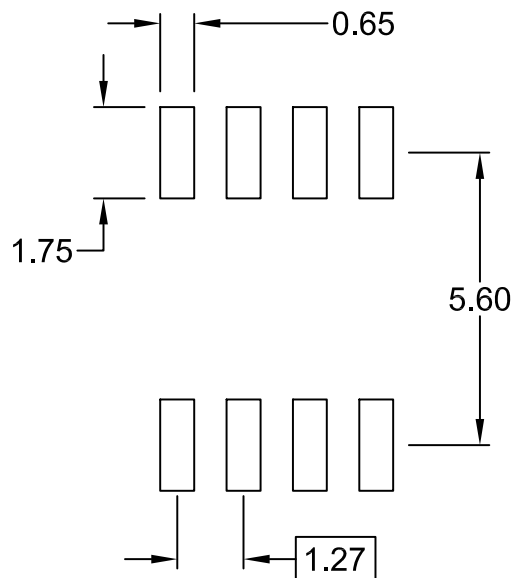


**SOIC8**  
**CASE 751EB**  
**ISSUE A**

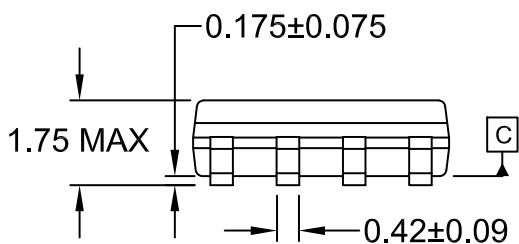
DATE 24 AUG 2017



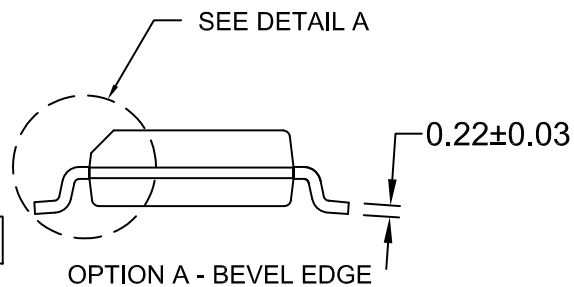
$\varnothing$  0.25 (M) C B A



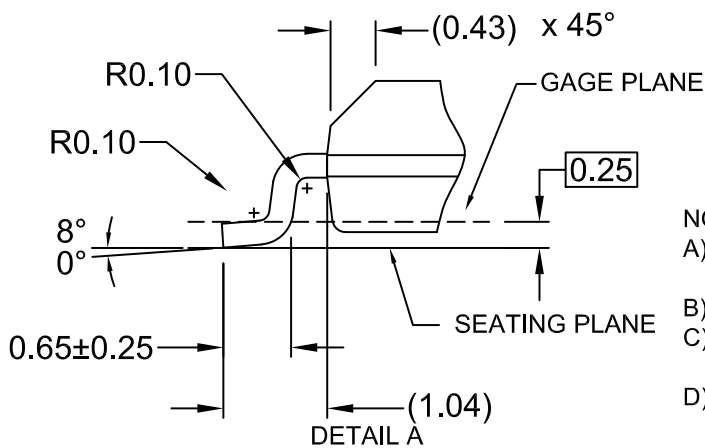
LAND PATTERN RECOMMENDATION



$\frac{1}{2}$  0.10



OPTION B - NO BEVEL EDGE



SCALE: 2:1

**NOTES:**

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M

<b>DOCUMENT NUMBER:</b>	<b>98AON13735G</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>SOIC8</b>	<b>PAGE 1 OF 1</b>

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

---

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)

