

# PACVGA200

## VGA Port Companion Circuit

### Product Description

The PACVGA200 incorporates seven channels of ESD protection for all signal lines commonly found in a VGA port. ESD protection is implemented with current steering diodes designed to safely handle the high surge currents encountered with IEC-61000-4-2 Level-4 ESD Protection ( $\pm 8$  kV contact discharge). When a channel is subjected to an electrostatic discharge, the ESD current pulse is diverted via the protection diodes into either the positive supply rail or ground where it may be safely dissipated. Separate positive supply rails are provided for the VIDEO, DDC and SYNC channels to facilitate interfacing with low voltage Video Controller ICs and provide design flexibility in multi-supply-voltage environments.

Two non-inverting drivers provide buffering for the HSYNC and VSYNC signals from the Video Controller IC (SYNC\_IN1, SYNC\_IN2). These buffers accept TTL input levels and convert them to CMOS output levels that swing between Ground and  $V_{CC4}$ .

These drivers have nominal  $60 \Omega$  output impedance ( $R_S$ ) to match the characteristic impedance of the HSYNC & VSYNC lines of the video cables typically used in PC applications. Two N-channel FETs provide the level shifting function required when the DDC controller is operated at a lower supply voltage than the monitor. Three  $75 \Omega$  termination resistors suitable for terminating the video signals from the video DAC are also provided. These resistors have separate input pins to allow insertion of additional EMI filtering, if required, between the termination point and the ESD protection diodes. These resistors are matched to better than 2% for excellent signal level matching for the R/G/B signals.

When the PWR\_UP input is driven LOW, the SYNC inputs can be floated without causing the SYNC buffers to draw any current from the  $V_{CC4}$  supply. When the PWR\_UP input is LOW, the SYNC outputs are driven LOW.

An internal diode (D1 in schematic on previous page) is also provided so that  $V_{CC3}$  can be derived from  $V_{CC4}$ , if desired, by connecting  $V_{CC3}$  to  $V_{BIAS}$ . In applications where  $V_{CC4}$  may be powered down, diode D1 blocks any DC current paths from the DDC\_OUT pins back to the powered down  $V_{CC4}$  rail via the top ESD protection diodes.

### Features

- Single Chip Solution for the VGA Port Interface
- Includes ESD Protection, Level Shifting, and RGB Termination
- Seven Channels of ESD Protection for All VGA Port Connector Pins Meeting IEC-61000-4-2 Level-4 ESD Requirements ( $\pm 8$  kV Contact Discharge)
- Very Low Loading Capacitance from ESD Protection Diodes on VIDEO Lines, 4 pF Typical

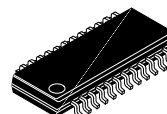
### Applications

- Notebook Computers with VGA Port



ON Semiconductor®

<http://onsemi.com>



QSOP24  
QR SUFFIX  
CASE 492B

### MARKING DIAGRAM



PACVGA200QR = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week

### ORDERING INFORMATION

| Device      | Package             | Shipping†        |
|-------------|---------------------|------------------|
| PACVGA200QR | QSOP24<br>(Pb-Free) | 2500/Tape & Reel |

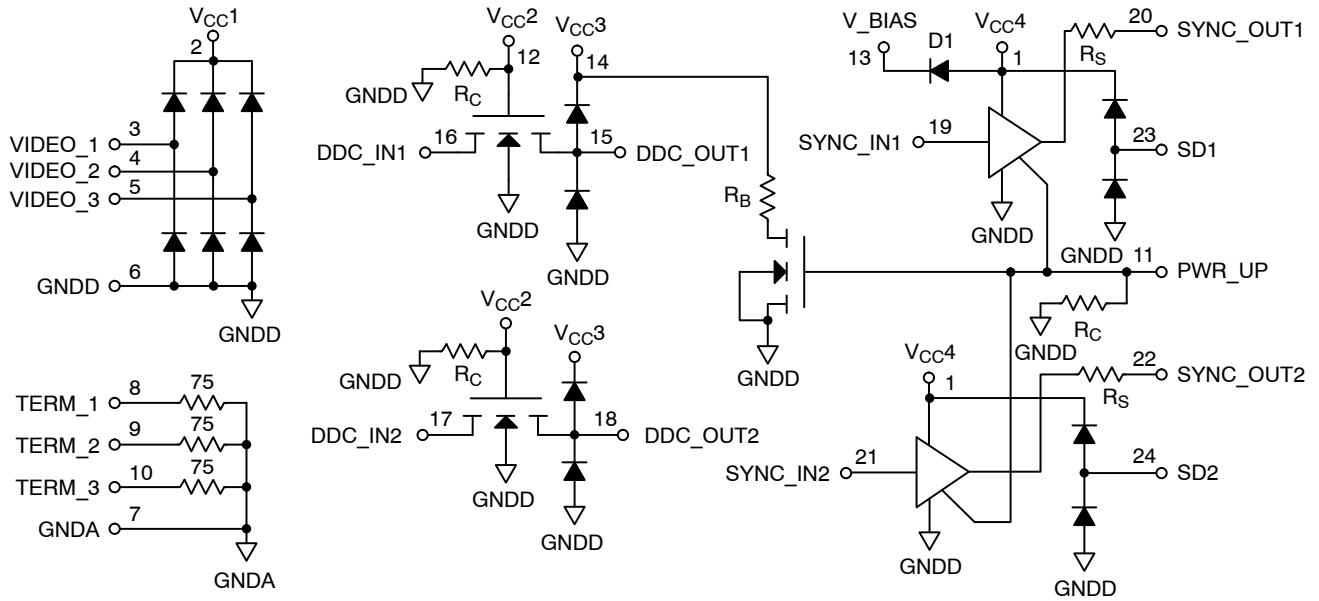
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

- $75 \Omega$  Termination Resistors for VIDEO Lines (Matched to 1% Typ.)
- TTL to CMOS Level-Translating Buffers with Power Down Mode for HSYNC and VSYNC Lines
- Bi-Directional Level Shifting N-Channel FETs Provided for DDC\_CLK & DDC\_DATA Channels
- Compact 24-Pin QSOP Package
- These Devices are Pb-Free and are RoHS Compliant

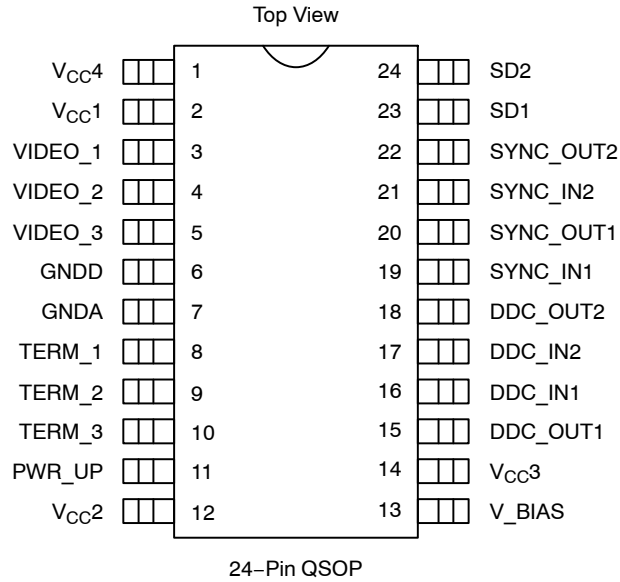
- Desktop PCs with VGA Port

# PACVGA200

## SIMPLIFIED ELECTRICAL SCHEMATIC



## PACKAGE / PINOUT DIAGRAMS



# PACVGA200

**Table 1. PIN DESCRIPTIONS**

| Lead(s) | Name                      | Description  |
|---------|---------------------------|--|
| 1       | V <sub>CC4</sub>          | Positive voltage supply pin. This is an isolated V <sub>CC</sub> pin for the SYNC_1, SYNC_2, SD1 and SD2 circuits.   |
| 2       | V <sub>CC1</sub>          | Positive voltage supply pin. This is an isolated V <sub>CC</sub> pin for the VIDEO_1, VIDEO_2 and VIDEO_3 ESD circuits.  |
| 3-5     | VIDEO_1, VIDEO_2, VIDEO_3 | RGB Video Protection Channels. These pins tie to the RGB video lines (for example, the Blue signal) between the VGA controller device and the video connector.         |
| 6       | GNDD                      | Digital Ground reference supply pin.   |
| 7       | GNDA                      | Ground reference supply pin for TERM_1, TERM_2 and TERM_3 pins.  |
| 8-10    | TERM_1, TERM_2, TERM_3    | RGB Video Termination Channels. These pins tie to the RGB video lines (for example, the Blue signal) providing a 75 Ω termination to GNDA for the given video channel. |
| 11      | PWR_UP                    | Sync Signal Output 1. Ties to the video connector side of one of the sync lines (for example the Horizontal Sync signal).  |
| 12      | V <sub>CC2</sub>          | Positive voltage supply pin. This is an isolated V <sub>CC</sub> pin for the DDC_IN1 and DDC_IN2 input circuits. Defines the logic one level for the DDC_OUTn outputs. |
| 13      | V_BIAS                    | Used to derive V <sub>CC3</sub> from V <sub>CC4</sub> input.   |
| 14      | V <sub>CC3</sub>          | Positive voltage supply pin. This is an isolated V <sub>CC</sub> pin for the DDC_OUT1 and DDC_OUT2 ESD protection circuits.  |
| 15      | DDC_OUT1                  | DDC Signal Output 1. Connects to the connector side of one of the DDC signals (for example, the bidirectional DDC_Data serial line).                                   |
| 16      | DDC_IN1                   | DDC Signal Input 1. Connects to the VGA Controller side of one of the DDC signals (for example, the bidirectional DDC_Data serial line).                               |
| 17      | DDC_IN2                   | DDC Signal Input 2. Connects to the VGA Controller side of one of the DDC signals (for example, the bidirectional DDC_Clk).  |
| 18      | DDC_OUT2                  | DDC Signal Output 2. Connects to the connector side of one of the DDC signals (for example, the bidirectional DDC_Clk).  |
| 19      | SYNC_IN1                  | Sync Signal Buffer Input 1. Connects to the VGA Controller side of one of the sync lines (for example, the Horizontal Sync signal).                                    |
| 20      | SYNC_OUT1                 | Sync Signal Buffer Output 1. Connects to the video connector side of one of the sync lines (for example the Horizontal Sync signal).                                   |
| 21      | SYNC_IN2                  | Sync Signal Buffer Input 2. Connects to the VGA Controller side of one of the sync lines (for example, the Vertical Sync signal).                                      |
| 22      | SYNC_OUT2                 | Sync Signal Buffer Output 2. Connects to the video connector side of one of the sync lines (for example the Vertical Sync signal).                                     |
| 23      | SD1                       | Sync Signal Filter 1. Connects to the video connector side of one of the sync lines (for example the Vertical Sync signal).  |
| 24      | SD2                       | Sync Signal Filter 2. Connects to the video connector side of one of the sync lines (for example the Horizontal Sync signal).  |

# PACVGA200

## SPECIFICATIONS

**Table 2. ABSOLUTE MAXIMUM RATINGS**

| Parameter   | Rating   | Units |
|---|--|-------|
| V <sub>CC1</sub> , V <sub>CC2</sub> , V <sub>CC3</sub> and V <sub>CC4</sub> Supply Voltage  | [GND – 0.5] to +6.0  | V     |
| Diode D1 Forward DC Current   | 100  | μA    |
| Storage Temperature Range   | –65 to +150  | °C    |
| DC Voltage at Inputs<br>VIDEO_1, VIDEO_2, VIDEO_3<br>TERM_1, TERM_2, TERM_3<br>DDC_IN1, DDC_IN2<br>DDC_OUT1, DDC_OUT2<br>SYNC_IN1, SYNC_IN2 | [GND – 0.5] to [V <sub>CC1</sub> + 0.5]<br>–6.0, +6.0<br>[GND – 0.5] to [V <sub>CC2</sub> + 0.5]<br>[GND – 0.5] to [V <sub>CC3</sub> + 0.5]<br>[GND – 0.5] to [V <sub>CC4</sub> + 0.5] | V     |
| Package Power Rating  | 1000   | mW    |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Table 3. STANDARD OPERATING CONDITIONS**

| Parameter                   | Rating   | Units |
|-----------------------------|----------|-------|
| Operating Temperature Range | 0 to +70 | °C    |

**Table 4. ELECTRICAL OPERATING CHARACTERISTICS** (Note 1)

| Symbol                                 | Parameter  | Conditions   | Min   | Typ                   | Max      | Units |
|--|--|--|-------|-----------------------|----------|-------|
| I <sub>CC1</sub>                       | V <sub>CC1</sub> Supply Current                      | V <sub>CC1</sub> = 5.0 V, VIDEO inputs at V <sub>CC1</sub> or GND level  |       |                       | 10       | μA    |
| I <sub>CC2</sub> ,<br>I <sub>CC3</sub> | V <sub>CC2</sub> & V <sub>CC3</sub> Supply Current   | V <sub>CC2</sub> = V <sub>CC3</sub> = 5.0 V  |       |                       | 10       | μA    |
| I <sub>CC4</sub>                       | V <sub>CC4</sub> Supply Current                      | V <sub>CC4</sub> = 5.0 V, SYNC Inputs at GND or V <sub>CC4</sub> Level, PWR-UP pin at V <sub>CC4</sub> , SYNC Outputs Unloaded             |       | 10                    |          | μA    |
|  |  | V <sub>CC4</sub> = 5.0 V, SYNC Inputs at 3.0 V, PWR-UP Pin at V <sub>CC4</sub> , SYNC Outputs Unloaded                                     |       | 200                   |          | μA    |
|  |  | V <sub>CC4</sub> = 5.0 V, PWR-UP Input at GND, SYNC Outputs Unloaded   |       |                       | 10       | μA    |
| V <sub>BIAS</sub>                      | V <sub>BIAS</sub> Open Circuit Voltage               | No External Current Drawn from V <sub>BIAS</sub> Pin   |       | V <sub>CC4</sub> –0.8 |          | V     |
| R <sub>T</sub>                         | Video Termination Resistance                         |  | 71.25 | 75                    | 78.75    | Ω     |
|  | R <sub>T</sub> Resistance Matching                   |  |       | 1                     | 2        | %     |
| V <sub>IH</sub>                        | Logic High Input Voltage                             | V <sub>CC4</sub> = 5.0 V (Note 2)  | 2.0   |                       |          | V     |
| V <sub>IL</sub>                        | Logic Low Input Voltage                              | V <sub>CC4</sub> = 5.0 V (Note 2)  |       |                       | 0.8      | V     |
| V <sub>OH</sub>                        | Logic High Output Voltage                            | I <sub>OH</sub> = –4 mA, V <sub>CC4</sub> = 5.0 V (Note 2)   | 4.5   |                       | 4.8      | V     |
| V <sub>OL</sub>                        | Logic Low Output Voltage                             | I <sub>OL</sub> = 4 mA, V <sub>CC4</sub> = 5.0 V (Note 2)  | 0.18  |                       | 0.32     | V     |
| R <sub>OH</sub>                        | Output Resistance                                    | (Note 2)   | 50    |                       | 125      | Ω     |
| R <sub>OL</sub>                        |  |  | 45    |                       | 80       | Ω     |
| R <sub>B</sub> , R <sub>P</sub>        | Resistor Value                                       | PWR_UP = V <sub>CC3</sub> = 5.0 V  | 0.5   | 1.0                   | 2.0      | MΩ    |
| R <sub>C</sub>                         | V <sub>CC2</sub> Pull-down Resistor Value            | V <sub>CC2</sub> = 3.0 V   | 0.5   | 1.5                   | 3.0      | MΩ    |
| I <sub>N</sub>                         | Input Current<br>VIDEO Inputs<br>HSYNC, VSYNC Inputs | V <sub>CC1</sub> = 5.0 V, V <sub>IN</sub> = V <sub>CC1</sub> or GND<br>V <sub>CC4</sub> = 5.0 V, V <sub>IN</sub> = V <sub>CC4</sub> or GND |       |                       | ±1<br>±1 | μA    |

# PACVGA200

**Table 4. ELECTRICAL OPERATING CHARACTERISTICS** (Note 1)

| Symbol     | Parameter   | Conditions  | Min        | Typ        | Max        | Units         |
|------------|---|---|------------|------------|------------|---------------|
| $I_{OFF}$  | Off-State Leakage Current,<br>Level-Shifting NFET         | $(V_{CC2} - V_{DDC\_IN}) \leq 0.4\text{ V}$ ,<br>$V_{DDC\_OUT} = V_{CC2}$<br>$(V_{CC2} - V_{DDC\_OUT}) \leq 0.4\text{ V}$ ,<br>$V_{DDC\_IN} = V_{CC2}$  |            |            | 10<br>10   | $\mu\text{A}$ |
| $V_{ON}$   | Voltage Drop Across Level<br>Shifting NFET when Turned ON | $V_{CC2} = 2.5\text{ V}$ , $V_S = \text{GND}$ , $I_{DS} = 3\text{ mA}$  |            |            | 0.15       | V             |
| $C_{IN}$   | Input Capacitance<br>VIDEO_1, VIDEO_2 & VIDEO_3<br>Inputs | $V_{CC1} = 5.0\text{ V}$ , $V_{IN} = 2.5\text{ V}$ ,<br>Measured at 1 MHz<br>$V_{CC1} = 2.5\text{ V}$ , $V_{IN} = 1.25\text{ V}$ ,<br>Measured at 1 MHz | 3.0<br>3.0 | 4.0<br>4.5 | 5.0<br>5.6 | pF            |
| $t_{PLH}$  | SYNC Drivers L $\geq$ H Propagation<br>Delay              | $C_L = 50\text{ pF}$ , $V_{CC} = 5.0\text{ V}$ ,<br>Input $t_R$ and $t_F \leq 5\text{ ns}$  |            | 8.0        | 12.0       | ns            |
| $t_{PHL}$  | SYNC Drivers H $\geq$ L Propagation<br>Delay              | $C_L = 50\text{ pF}$ , $V_{CC} = 5.0\text{ V}$ ,<br>Input $t_R$ and $t_F \leq 5\text{ ns}$  |            | 8.0        | 12.0       | ns            |
| $t_R, t_F$ | SYNC Drivers Output Rise & Fall<br>Times                  | $C_L = 50\text{ pF}$ , $V_{CC} = 5.0\text{ V}$ ,<br>Input $t_R$ and $t_F \leq 5\text{ ns}$<br>(Measured 10% - 90%)                                      | 5.0        | 7.0        | 10.0       | ns            |
| $V_{ESD}$  | ESD Withstand Voltage                                     | $V_{CC1} = V_{CC3} = V_{CC4} = 5\text{ V}$ (Note 3)   | $\pm 8$    |            |            | kV            |

1. All parameters specified over standard operating conditions unless otherwise noted.
2. This parameter applies only to the HSYNC and VSYNC channels. HSYNC and VSYNC have 8 mA drivers with  $R_S$  added in series to terminate transmission line.
3. Per the IEC-61000-4-2 International ESD Standard, Level 4 contact discharge method.  $V_{CC1}$ ,  $V_{CC3}$  and  $V_{CC4}$  must be bypassed to GND via a low impedance ground plane with a 0.2  $\mu\text{F}$ , low inductance, chip ceramic capacitor at each supply pin. ESD pulse is applied between the applicable pins and GND. ESD pulse can be positive or negative with respect to GND. Applicable pins are: VIDEO\_1, VIDEO\_2, VIDEO\_3, SYNC\_OUT1, SD1, SYNC\_OUT2, SD2, DDC\_OUT1 and DDC\_OUT2. All other pins are ESD protected to the industry standard 2 kV per the Human Body Model (MIL-STD-883, Method 3015).

# PACVGA200

## TEST CIRCUIT INFORMATION

### Average Current through $V_{CC4}$ ( $I_{CC4}$ )

The circuit in Figure 1 was used to characterize  $I_{CC4}$  current as SYNC\_IN signal frequency varies. A square wave signal was connected to the input of one of the SYNC buffers (i.e. pin 19 or pin 21). The frequency of this signal was varied between 0 and 100 kHz. The risetime and falltime was kept constant at 10 ns. Three different values of C1 were used: 0 pF, 50 pF and 100 pF. The results are plotted in Figure 2.

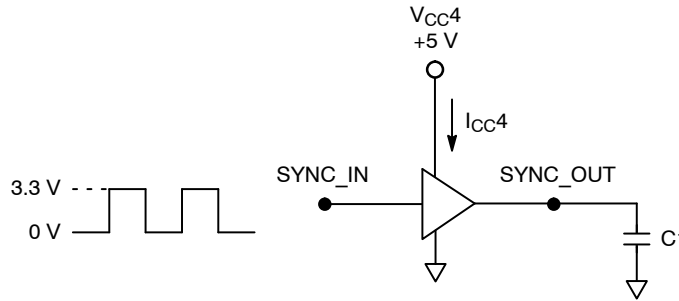


Figure 1. Sync Buffer  $I_{CC4}$  Test Circuit

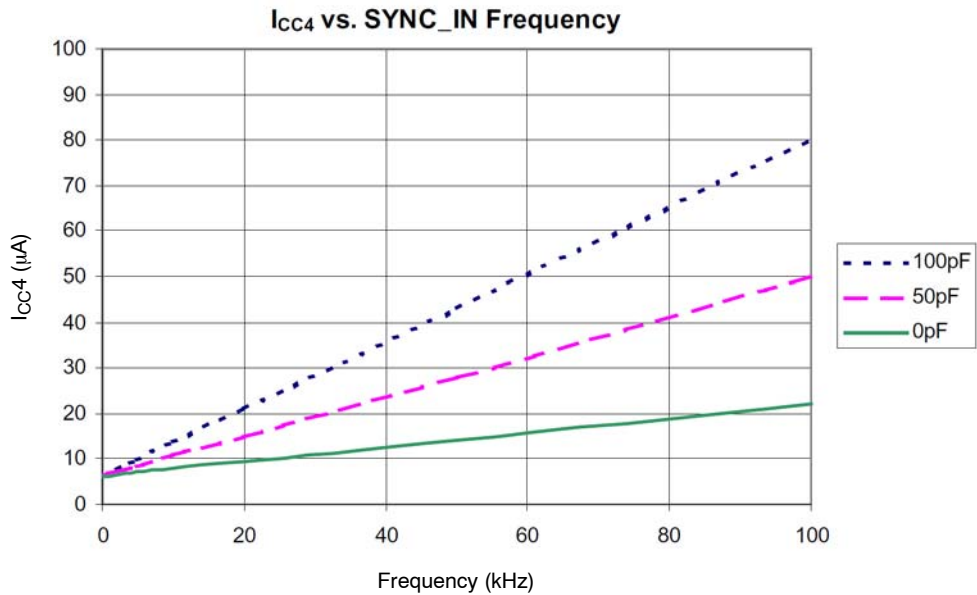
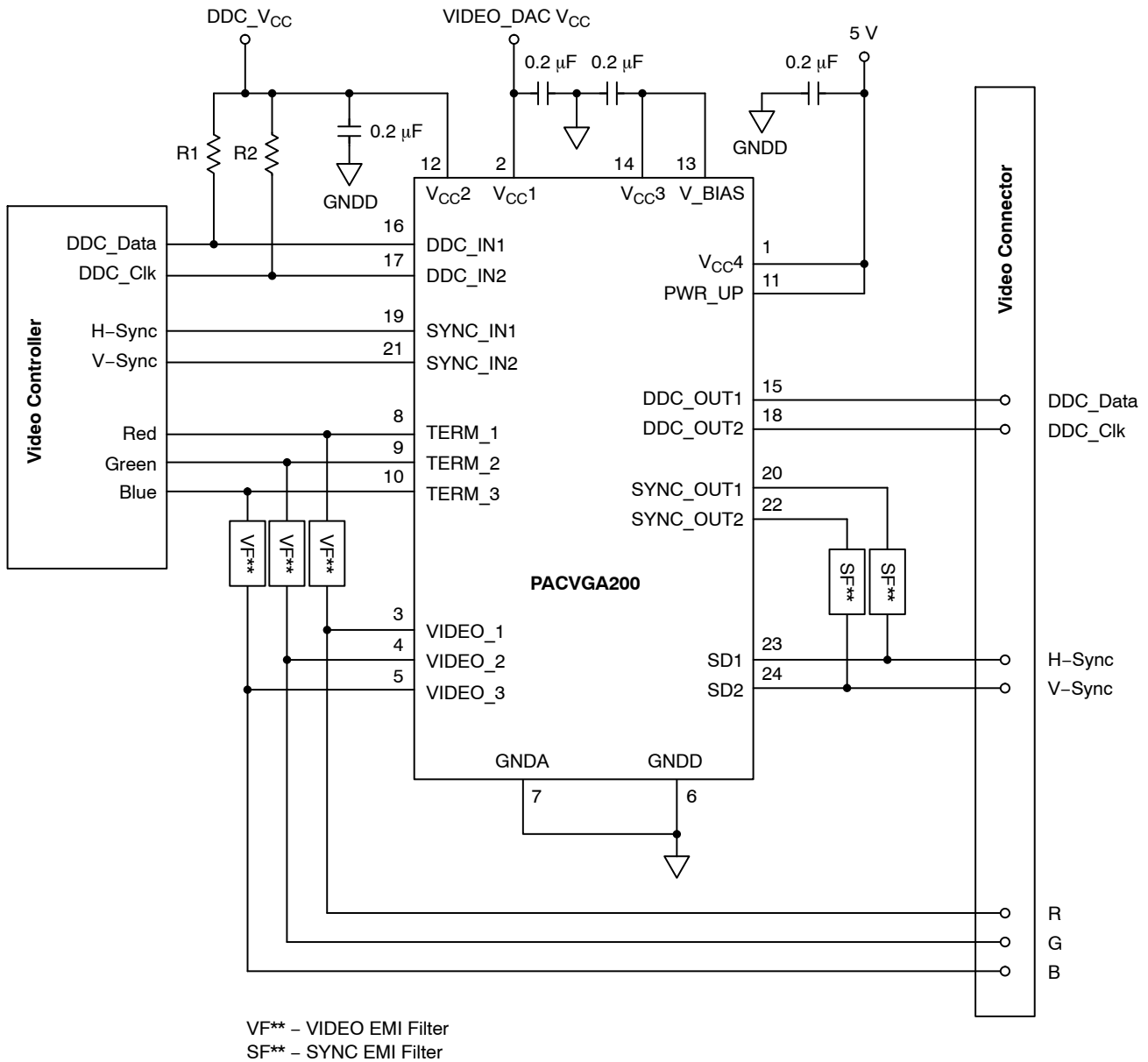


Figure 2.  $I_{CC4}$  vs. SYNC\_IN Frequency Performance Data

# PACVGA200

## APPLICATION INFORMATION



**Figure 3. Typical Connection Diagram**

A resistor may be necessary between the  $V_{CC3}$  pin and ground if protection against a stream of ESD pulses is required while the PACVGA200 is in the power-down state. The value of this resistor should be chosen such that the extra charge deposited into the  $V_{CC3}$  bypass capacitor by each ESD pulse will be discharged before the next ESD pulse occurs. The maximum ESD repetition rate specified by the IEC-61000-4-2 standard is one pulse per second. When the PACVGA200 is in the power-up state, an internal discharge resistor is connected to ground via an FET switch for this purpose.

For the same reason,  $V_{CC1}$  and  $V_{CC4}$  may also require bypass capacitor discharging resistors to ground if there are no other components in the system to provide a discharge path to ground.

GNDA, the reference voltage for the 75  $\Omega$  resistors is not connected internally to GNDD and should ideally be connected to the ground of the video DAC IC.

# MECHANICAL CASE OUTLINE

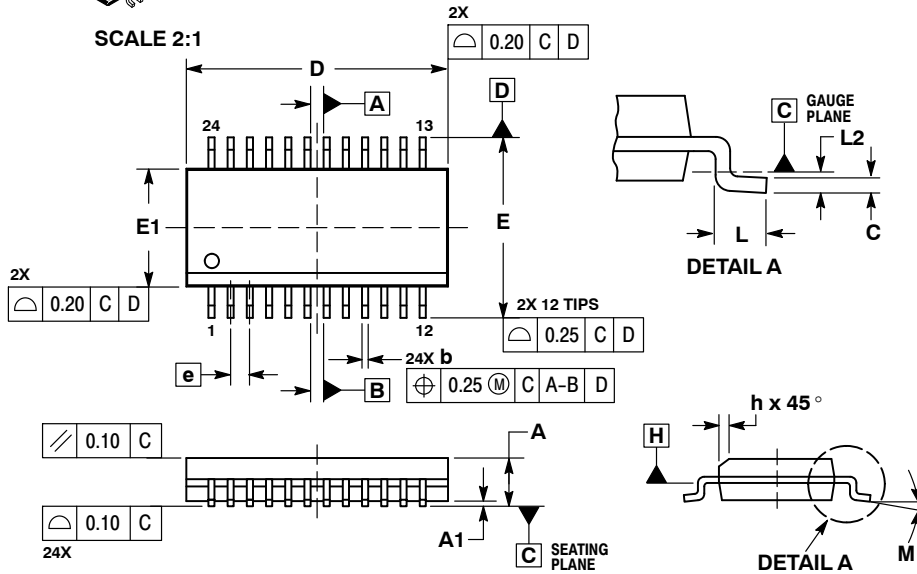
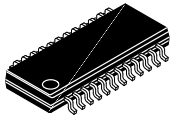
## PACKAGE DIMENSIONS

ON Semiconductor®



### QSOP24 NB CASE 492B-01 ISSUE A

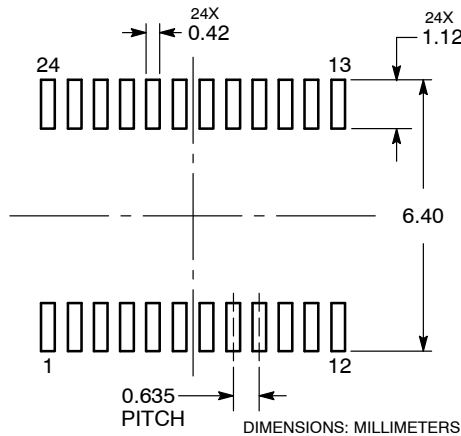
DATE 06 MAY 2008



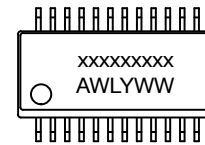
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
  4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 PER SIDE. D AND E1 ARE DETERMINED AT DATUM H.
  5. DATUMS A AND B ARE DETERMINED AT DATUM H.

| MILLIMETERS |           |      |
|-------------|-----------|------|
| DIM         | MIN       | MAX  |
| A           | 1.35      | 1.75 |
| A1          | 0.10      | 0.25 |
| b           | 0.20      | 0.30 |
| C           | 0.19      | 0.25 |
| D           | 8.65 BSC  |      |
| E           | 6.00 BSC  |      |
| E1          | 3.90 BSC  |      |
| e           | 0.635 BSC |      |
| h           | 0.22      | 0.50 |
| L           | 0.40      | 1.27 |
| L2          | 0.25 BSC  |      |
| M           | 0°        | 8°   |

### SOLDERING FOOTPRINT



### GENERIC MARKING DIAGRAM\*



- xxx = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.

|                         |                    |  |
|-------------------------|--------------------|--|
| <b>DOCUMENT NUMBER:</b> | <b>98AON04474D</b> | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| <b>DESCRIPTION:</b>     | <b>QSOP24 NB</b>   | <b>PAGE 1 OF 1</b>   |

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.



**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)