

NVMTS0D6N04CL

MOSFET – Power, Single N-Channel 40 V, 0.42 mΩ, 554.5 A

Features

- Small Footprint (8x8 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- Wettable Flank Plated for Enhanced Optical Inspection
- AEC-101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Parameter | | Symbol | Value | Unit | |
|--|---|---------------------------|-------------|------------------|---|
| Drain-to-Source Voltage | | V_{DS} | 40 | V | |
| Gate-to-Source Voltage | | V_{GS} | ± 20 | V | |
| Continuous Drain Current $R_{\theta JC}$ (Note 2) | Steady State | $T_C = 25^\circ\text{C}$ | I_D | 554.5 | A |
| | | $T_C = 100^\circ\text{C}$ | | 392.1 | |
| Power Dissipation $R_{\theta JC}$ (Note 2) | Steady State | $T_C = 25^\circ\text{C}$ | P_D | 245.4 | W |
| | | $T_C = 100^\circ\text{C}$ | | 122.7 | |
| Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2) | Steady State | $T_A = 25^\circ\text{C}$ | I_D | 78.9 | A |
| | | $T_A = 100^\circ\text{C}$ | | 55.8 | |
| Power Dissipation $R_{\theta JA}$ (Notes 1, 2) | Steady State | $T_A = 25^\circ\text{C}$ | P_D | 5.0 | W |
| | | $T_A = 100^\circ\text{C}$ | | 2.5 | |
| Pulsed Drain Current | $T_A = 25^\circ\text{C}$, $t_p = 10 \mu\text{s}$ | I_{DM} | 900 | A | |
| Operating Junction and Storage Temperature Range | | T_J, T_{stg} | -55 to +175 | $^\circ\text{C}$ | |
| Source Current (Body Diode) | | I_S | 204.5 | A | |
| Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 52.7 \text{ A}$) | | E_{AS} | 2058 | mJ | |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | | T_L | 260 | $^\circ\text{C}$ | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---|-----------------|-------|---------------------------|
| Junction-to-Case – Steady State (Note 2) | $R_{\theta JC}$ | 0.61 | $^\circ\text{C}/\text{W}$ |
| Junction-to-Ambient – Steady State (Note 2) | $R_{\theta JA}$ | 30.2 | |

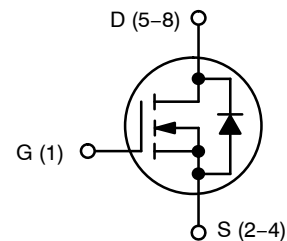
1. Surface-mounted on FR4 board using a 1 in² pad size, 1 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.



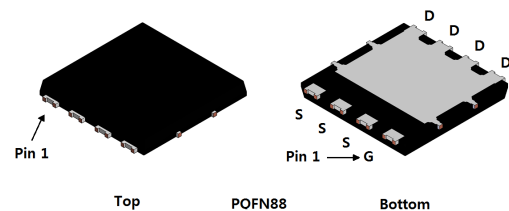
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| $V_{(BR)DSS}$ | $R_{DS(ON)} \text{ MAX}$ | $I_D \text{ MAX}$ |
|---------------|--------------------------|-------------------|
| 40 V | 0.42 mΩ @ 10 V | 554.5 A |
| | 0.66 mΩ @ 4.5 V | |

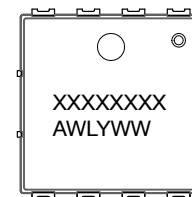


N-CHANNEL MOSFET



POWER 88
CASE 507AP

MARKING DIAGRAM



XXX = Device Code
(8 A–N characters max)
A = Assembly Location
WL = 2-digit Wafer Lot Code
Y = Year Code
WW = Work Week Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NVMTS0D6N04CL

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|-------------------|--|---------------------------|------|-----|----------------------|
| OFF CHARACTERISTICS | | | | | | |
| Drain-to-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$ | 40 | | | V |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | $I_D = 250\ \mu\text{A}$, ref to 25°C | | 12.6 | | mV/ $^\circ\text{C}$ |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}$ | $T_J = 25^\circ\text{C}$ | | 10 | μA |
| | | | $T_J = 125^\circ\text{C}$ | | 250 | |
| Gate-to-Source Leakage Current | I_{GSS} | $V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$ | | | 100 | nA |

ON CHARACTERISTICS (Note 3)

| | | | | | | |
|--|------------------|--|---------------------|------|------|----------------------|
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$ | 1.2 | | 2.0 | V |
| Negative Threshold Temperature Coefficient | $V_{GS(TH)}/T_J$ | $I_D = 250\ \mu\text{A}$, ref to 25°C | | -6.0 | | mV/ $^\circ\text{C}$ |
| Drain-to-Source On Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}$ | $I_D = 50\text{ A}$ | 0.35 | 0.42 | m Ω |
| | | $V_{GS} = 4.5\text{ V}$ | $I_D = 50\text{ A}$ | 0.52 | 0.66 | |
| Forward Transconductance | g_{FS} | $V_{DS} = 5\text{ V}, I_D = 50\text{ A}$ | | 323 | | S |
| Gate Resistance | R_G | $T_A = 25^\circ\text{C}$ | | 1.0 | | Ω |

CHARGES, CAPACITANCES & GATE RESISTANCE

| | | | | | | |
|------------------------------|--------------|--|--|-------|--|----|
| Input Capacitance | C_{ISS} | $V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 20\text{ V}$ | | 16013 | | pF |
| Output Capacitance | C_{OSS} | | | 6801 | | |
| Reverse Transfer Capacitance | C_{RSS} | | | 299 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS} = 4.5\text{ V}, V_{DS} = 20\text{ V}; I_D = 50\text{ A}$ | | 126 | | nC |
| Threshold Gate Charge | $Q_{G(TH)}$ | | | 22.5 | | |
| Gate-to-Source Charge | Q_{GS} | | | 39.9 | | |
| Gate-to-Drain Charge | Q_{GD} | | | 38.4 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS} = 10\text{ V}, V_{DS} = 20\text{ V}; I_D = 50\text{ A}$ | | 265 | | nC |

SWITCHING CHARACTERISTICS, $V_{GS} = 4.5\text{ V}$ (Note 4)

| | | | | | | |
|---------------------|--------------|---|--|------|--|----|
| Turn-On Delay Time | $t_{d(ON)}$ | $V_{GS} = 4.5\text{ V}, V_{DS} = 20\text{ V}, I_D = 50\text{ A}, R_G = 6\ \Omega$ | | 89.4 | | ns |
| Rise Time | t_r | | | 111 | | |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | | 180 | | |
| Fall Time | t_f | | | 84.7 | | |

DRAIN-SOURCE DIODE CHARACTERISTICS

| | | | | | | | |
|-------------------------|----------|--|---------------------------|------|------|-----|----|
| Forward Diode Voltage | V_{SD} | $V_{GS} = 0\text{ V}, I_S = 50\text{ A}$ | $T_J = 25^\circ\text{C}$ | | 0.75 | 1.2 | V |
| | | | $T_J = 125^\circ\text{C}$ | | 0.6 | | |
| Reverse Recovery Time | t_{RR} | $V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 50\text{ A}$ | | 99.3 | | ns | |
| Charge Time | t_a | | | 62.4 | | | |
| Discharge Time | t_b | | | 36.9 | | | |
| Reverse Recovery Charge | Q_{RR} | | | 228 | | | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

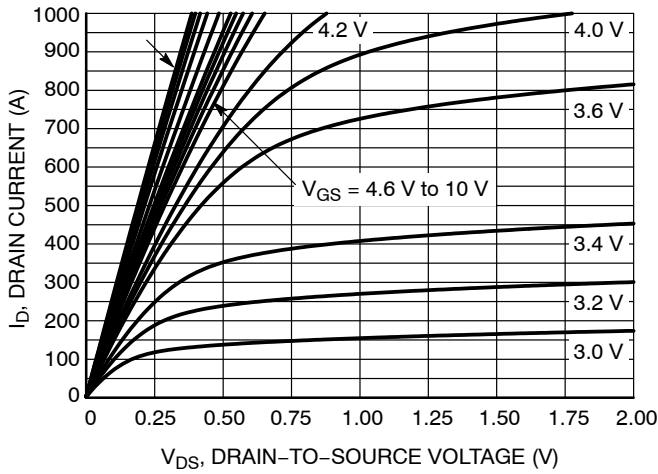


Figure 1. On-Region Characteristics

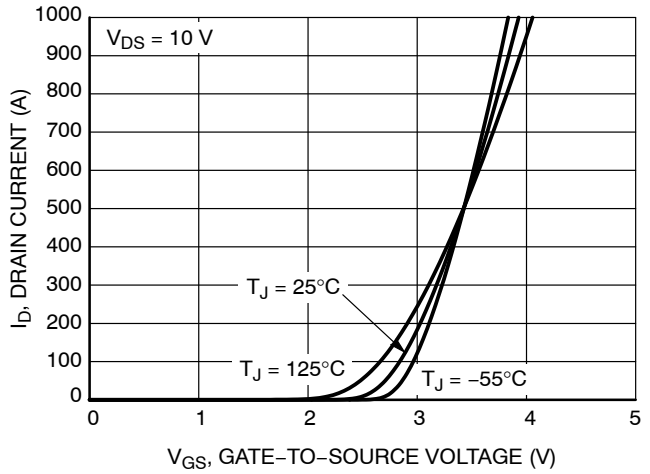


Figure 2. Transfer Characteristics

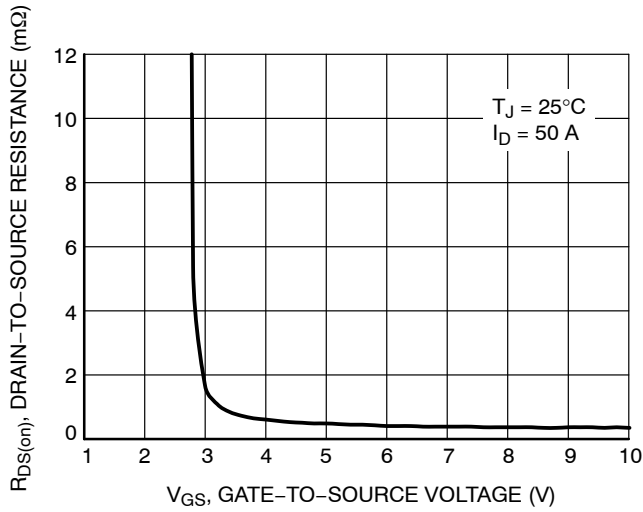


Figure 3. On-Resistance vs. Gate-to-Source Voltage

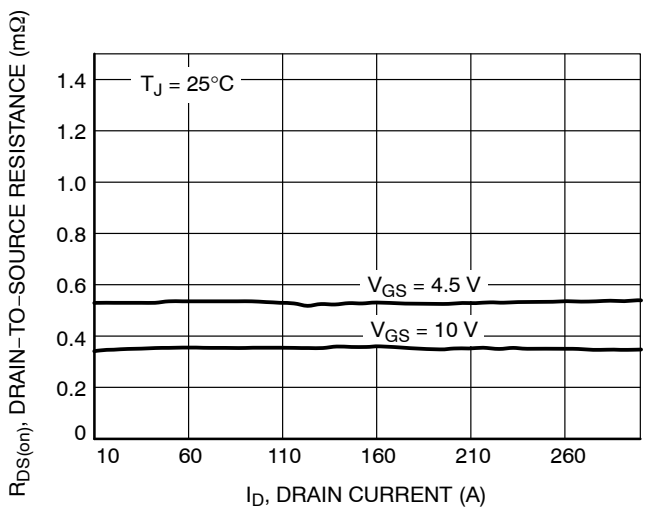


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

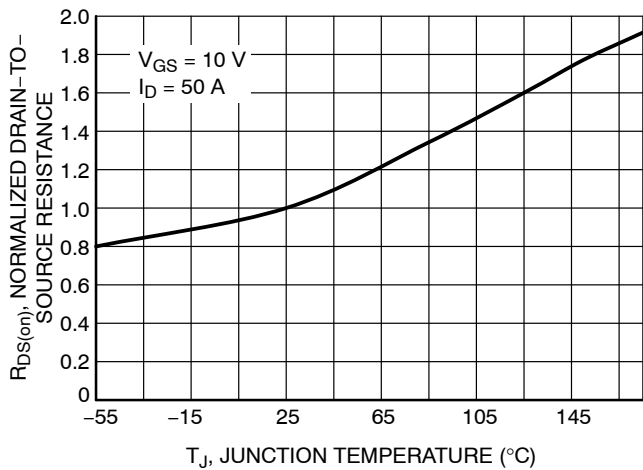


Figure 5. On-Resistance Variation with Temperature

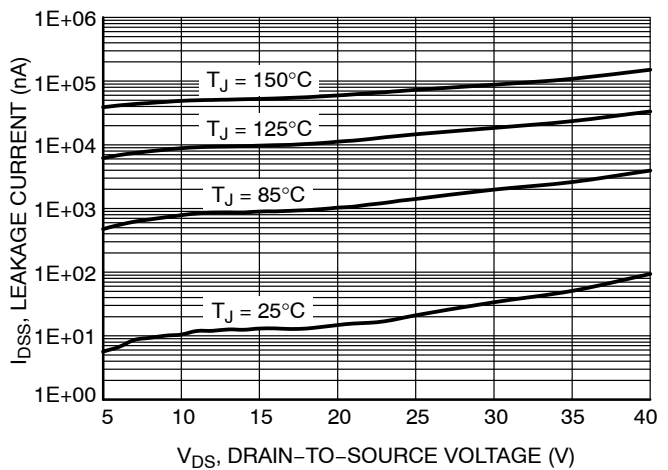


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

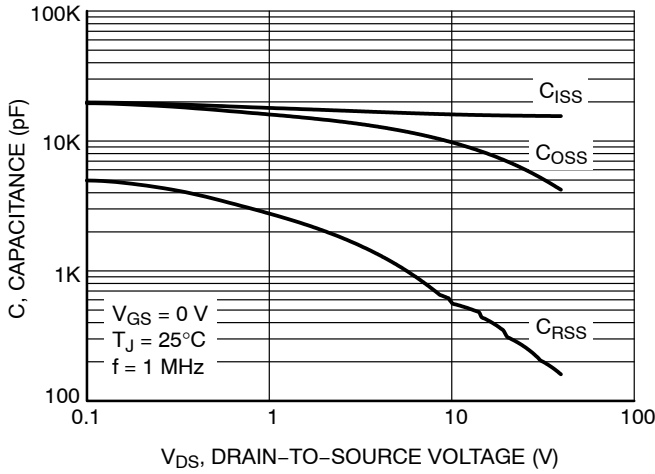


Figure 7. Capacitance Variation

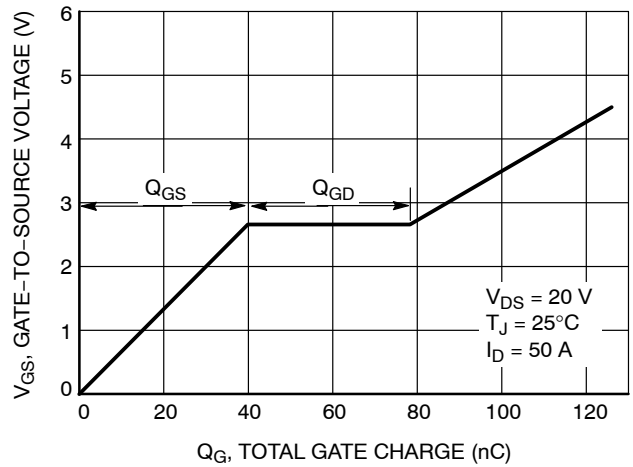


Figure 8. Gate-to-Source Voltage vs. Total Charge

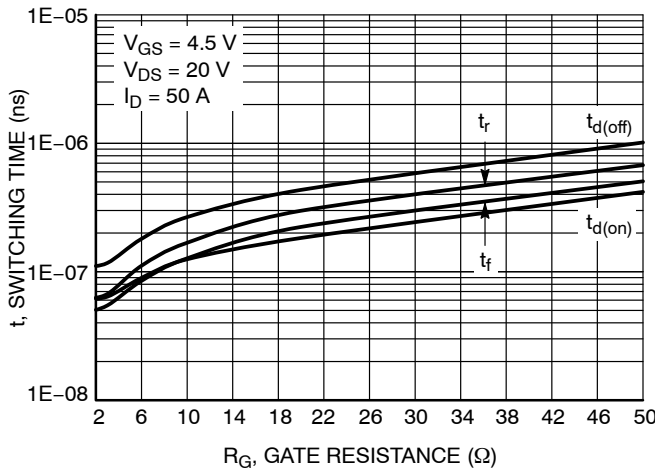


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

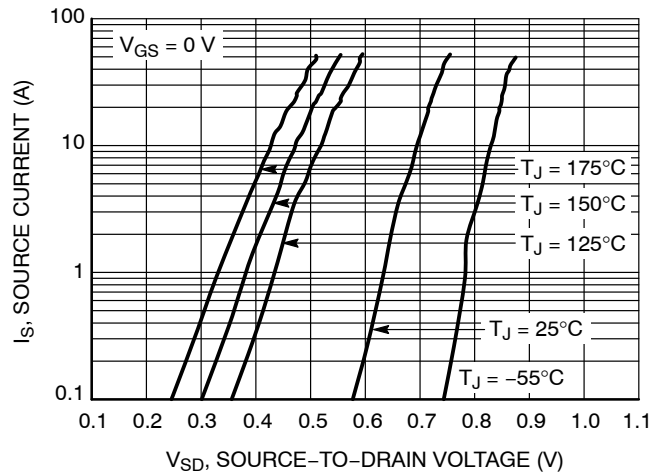


Figure 10. Diode Forward Voltage vs. Current

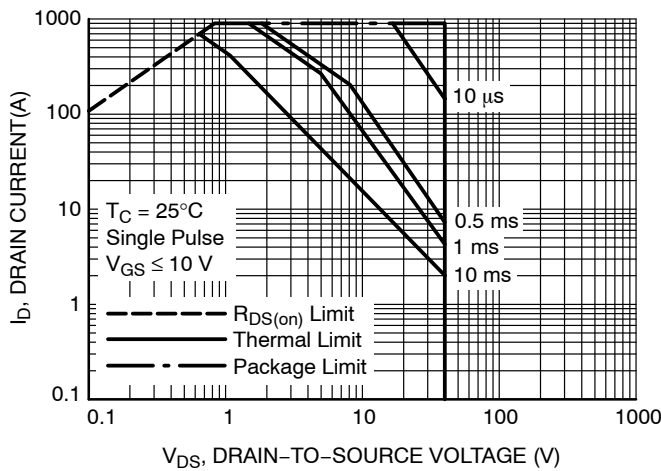


Figure 11. Maximum Rated Forward Biased Safe Operating Area

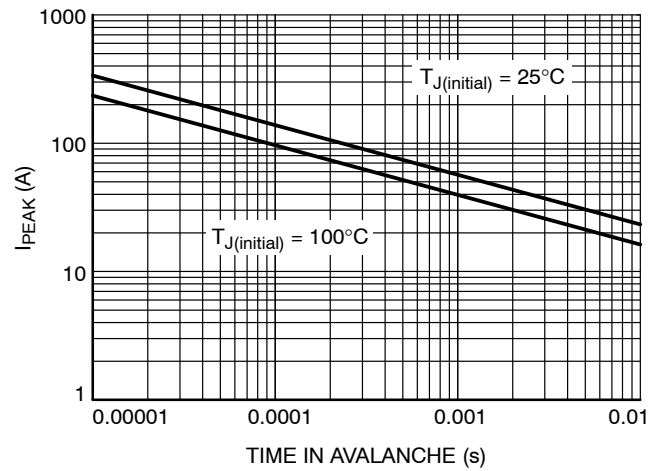


Figure 12. I_{PEAK} vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

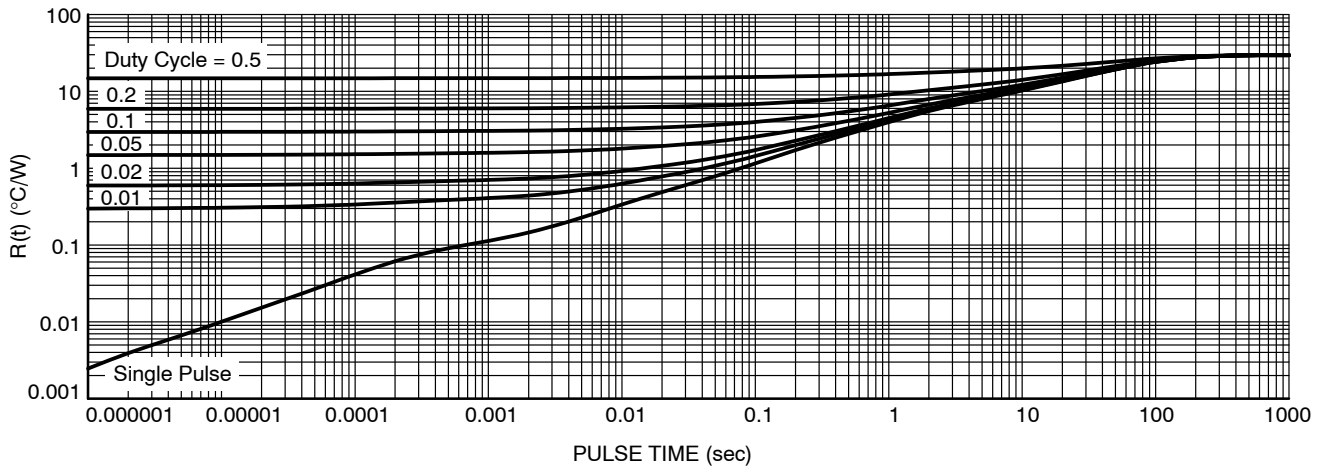


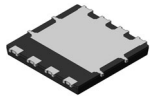
Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

| Device | Marking | Package | Shipping [†] |
|------------------|----------|-----------------------|-----------------------|
| NVMTS0D6N04CLTXG | 0D6N04CL | POWER 88 (Pb-Free) | 3000 / Tape & Reel |

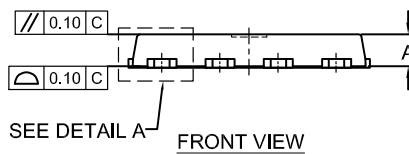
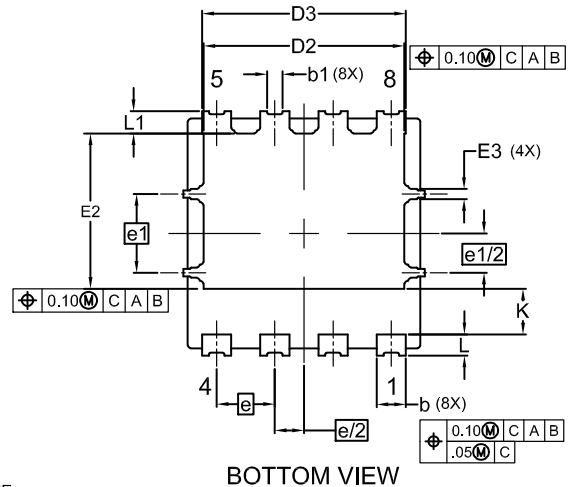
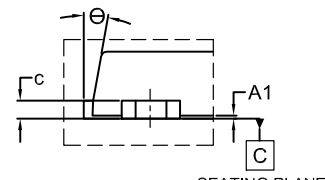
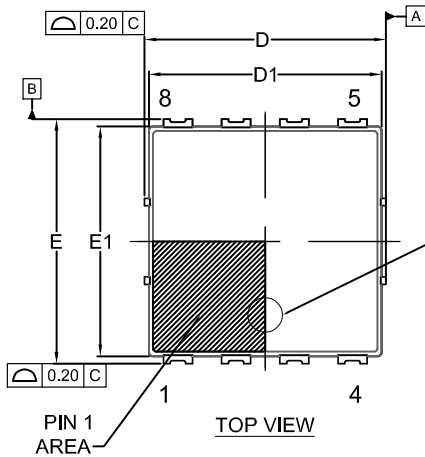
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

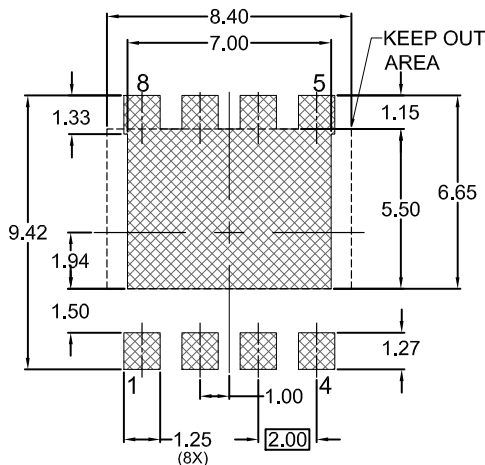


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CASE 507AP
ISSUE E

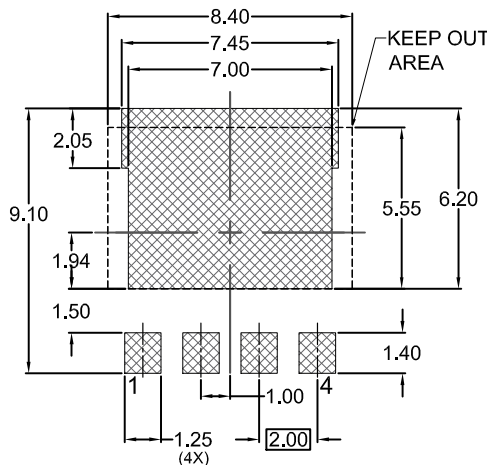
DATE 08 MAY 2024



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
 2. CONTROLLING DIMENSION: MILLIMETERS
 3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
 4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
 5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



RECOMMENDED LAND PATTERN*



UNIVERSAL LAND PATTERN*

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

| DIM | MILLIMETERS | | |
|------|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | 1.00 | 1.10 | 1.20 |
| A1 | 0.00 | — | 0.05 |
| b | 0.90 | 1.00 | 1.10 |
| b1 | 0.35 | 0.45 | 0.55 |
| c | 0.23 | 0.28 | 0.33 |
| D | 8.20 | 8.30 | 8.40 |
| D1 | 7.90 | 8.00 | 8.10 |
| D2 | 6.80 | 6.90 | 7.00 |
| D3 | 6.90 | 7.00 | 7.10 |
| E | 8.30 | 8.40 | 8.50 |
| E1 | 7.80 | 7.90 | 8.00 |
| E2 | 5.24 | 5.34 | 5.44 |
| E3 | 0.25 | 0.35 | 0.45 |
| e | 2.00 BSC | | |
| e/2 | 1.00 BSC | | |
| e1 | 2.70 BSC | | |
| e1/2 | 1.35 BSC | | |
| K | 1.50 | 1.57 | 1.70 |
| L | 0.64 | 0.74 | 0.84 |
| L1 | 0.67 | 0.77 | 0.87 |
| θ | 0° | — | 12° |

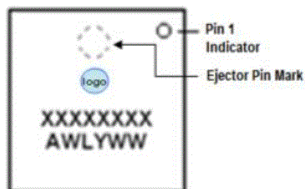
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CASE 507AP
ISSUE E

DATE 08 MAY 2024

GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot Code
- Y = Year Code
- WW = Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| | | |
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