

MOSFET – Power, Single N-Channel

60 V, 48 A, 10 mΩ

NVMFS5H610NL

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFS5H610NLWF – Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit	
V_{DSS}	Drain-to-Source Voltage	60	V	
V_{GS}	Gate-to-Source Voltage	± 20	V	
I_D	Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	$T_C = 25^\circ\text{C}$	48	A
		$T_C = 100^\circ\text{C}$	34	
P_D	Power Dissipation $R_{\theta JC}$ (Note 1)	$T_C = 25^\circ\text{C}$	52	W
		$T_C = 100^\circ\text{C}$	26	
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	$T_A = 25^\circ\text{C}$	13	A
		$T_A = 100^\circ\text{C}$	9	
P_D	Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	$T_A = 25^\circ\text{C}$	3.6	W
		$T_A = 100^\circ\text{C}$	1.8	
I_{DM}	Pulsed Drain Current $T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	243	A	
T_J, T_{stg}	Operating Junction and Storage Temperature Range	-55 to +175	$^\circ\text{C}$	
I_S	Source Current (Body Diode)	43	A	
E_{AS}	Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 2.8 \text{ A}$)	175	mJ	
T_L	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	260	$^\circ\text{C}$	

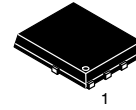
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

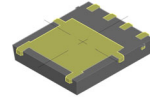
Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State	2.9	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Note 2)	42	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(ON) MAX}$	$I_D MAX$
60 V	10 mΩ @ 10 V	48 A
	13 mΩ @ 4.5 V	

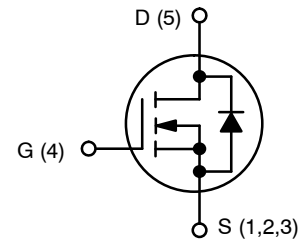


DFN5
(SO-8FL)
CASE 488AA
STYLE 1

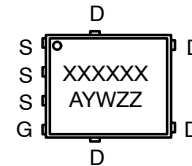


DFN5
(FULL-CUT SO8FL WF)
CASE 507BA

N-CHANNEL MOSFET



MARKING DIAGRAM



XXXXXX = 5H610L (NVMFS5H610NL) or 610LWF (NVMFS5H610NLWF)
 A = Assembly Location
 Y = Year
 W = Work Week
 ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5.

NVMFS5H610NL

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	60			V
$V_{(BR)DSS}/T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient			39.2		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{GS} = 0\text{ V}, V_{DS} = 60\text{ V}$	$T_J = 25\ ^\circ\text{C}$		10	μA
			$T_J = 125^\circ\text{C}$		250	
I_{GSS}	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS (Note 4)

$V_{GS(TH)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 40\ \mu\text{A}$	1.2		2.0	V
$V_{GS(TH)}/T_J$	Threshold Temperature Coefficient			-5.0		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 10\text{ V}$	$I_D = 8\text{ A}$	8.0	10	m Ω
		$V_{GS} = 4.5\text{ V}$	$I_D = 7\text{ A}$	10.5	13	

CHARGES, CAPACITANCES & GATE RESISTANCE

C_{ISS}	Input Capacitance	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 30\text{ V}$		880		pF
C_{OSS}	Output Capacitance			150		
C_{RSS}	Reverse Transfer Capacitance			6.0		
Q_{OSS}	Output Charge	$V_{GS} = 0\text{ V}, V_{DD} = 30\text{ V}$		12		nC
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 30\text{ V}; I_D = 8\text{ A}$		13.7		
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = 4.5\text{ V}, V_{DS} = 30\text{ V}; I_D = 8\text{ A}$		6.4		
$Q_{G(TH)}$	Threshold Gate Charge			1.6		
Q_{GS}	Gate-to-Source Charge			2.6		
Q_{GD}	Gate-to-Drain Charge			1.3		
V_{GP}	Plateau Voltage			2.6		

SWITCHING CHARACTERISTICS (Note 5)

$t_{d(ON)}$	Turn-On Delay Time	$V_{GS} = 4.5\text{ V}, V_{DS} = 48\text{ V}, I_D = 8\text{ A}, R_G = 2.5\ \Omega$		9.5		ns
t_r	Rise Time			23		
$t_{d(OFF)}$	Turn-Off Delay Time			22		
t_f	Fall Time			6		

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Forward Diode Voltage	$V_{GS} = 0\text{ V}, I_S = 8\text{ A}$	$T_J = 25^\circ\text{C}$		0.8	1.2	V
			$T_J = 125^\circ\text{C}$		0.65		
t_{RR}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, di_S/dt = 100\text{ A}/\mu\text{s}, I_S = 4\text{ A}$		24		ns	
t_a	Charge Time			15			
t_b	Discharge Time			9			
Q_{RR}	Reverse Recovery Charge			17			nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

5. Switching characteristics are independent of operating junction temperatures.

NVMFS5H610NL

TYPICAL CHARACTERISTICS

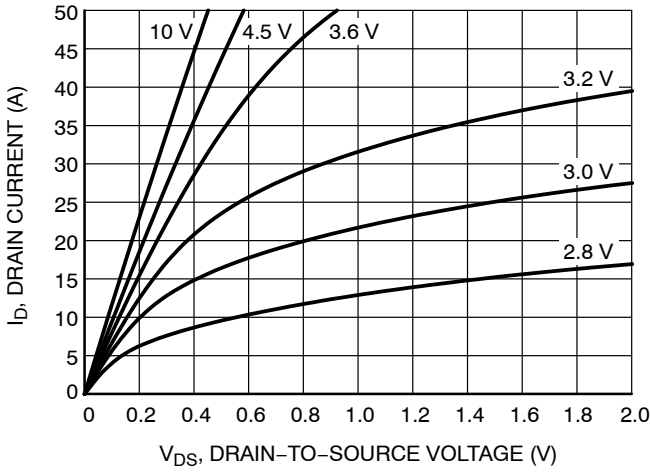


Figure 1. On-Region Characteristics

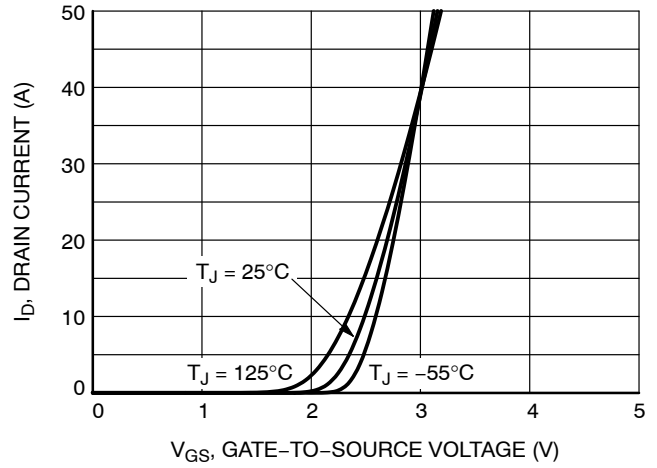


Figure 2. Transfer Characteristics

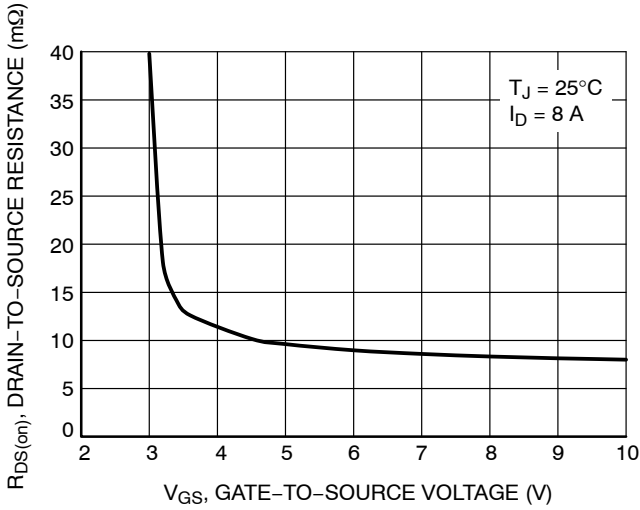


Figure 3. On-Resistance vs. Gate-to-Source Voltage

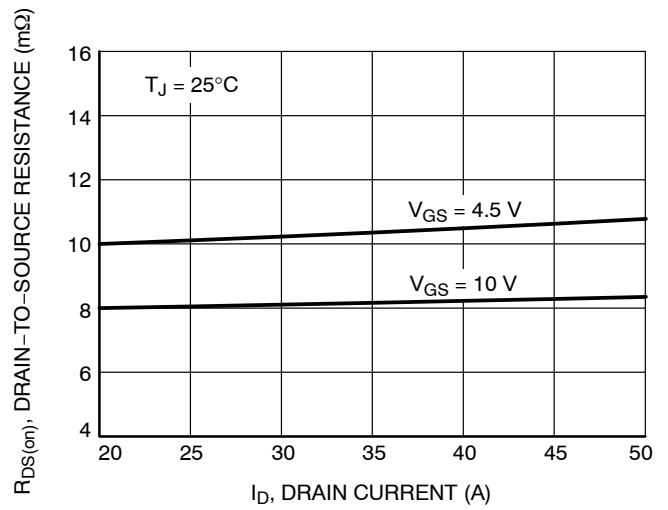


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

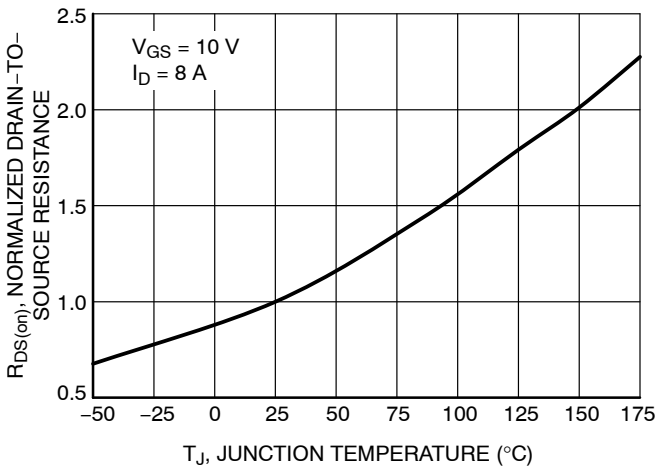


Figure 5. On-Resistance Variation with Temperature

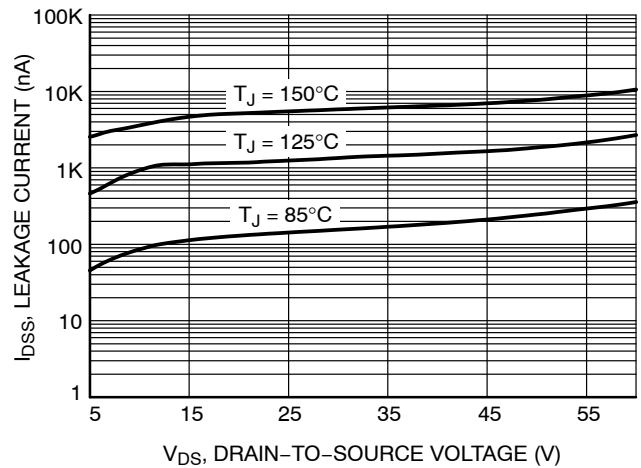


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NVMFS5H610NL

TYPICAL CHARACTERISTICS (continued)

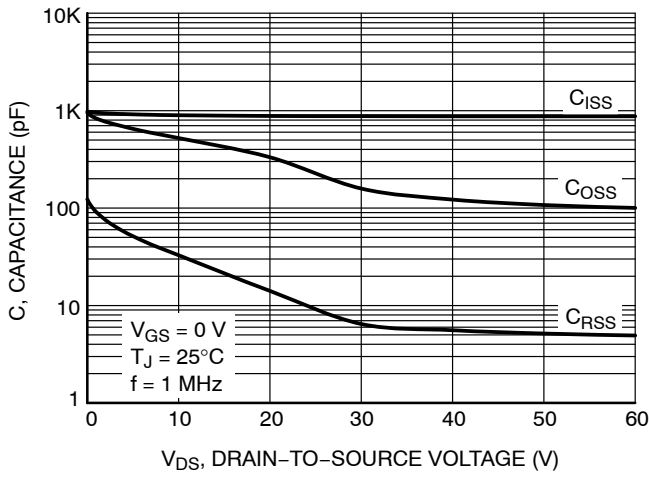


Figure 7. Capacitance Variation

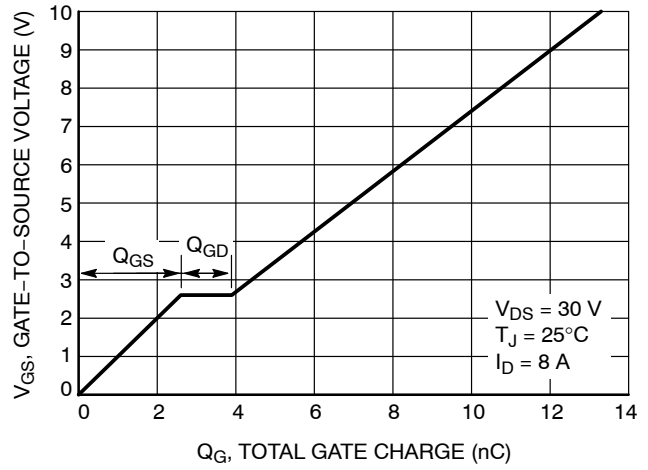


Figure 8. Gate-to-Source Voltage vs. Total Charge

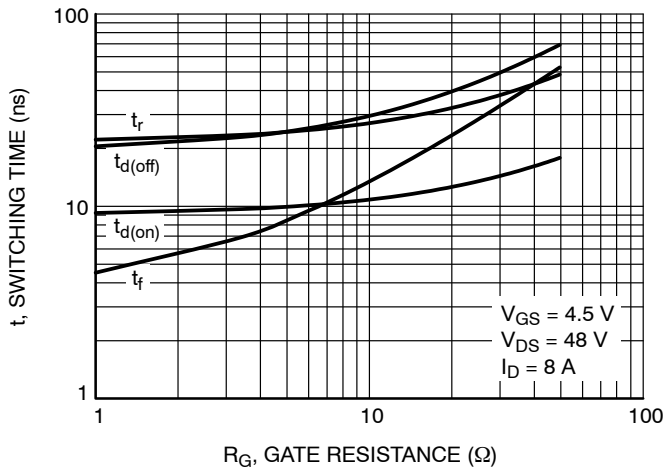


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

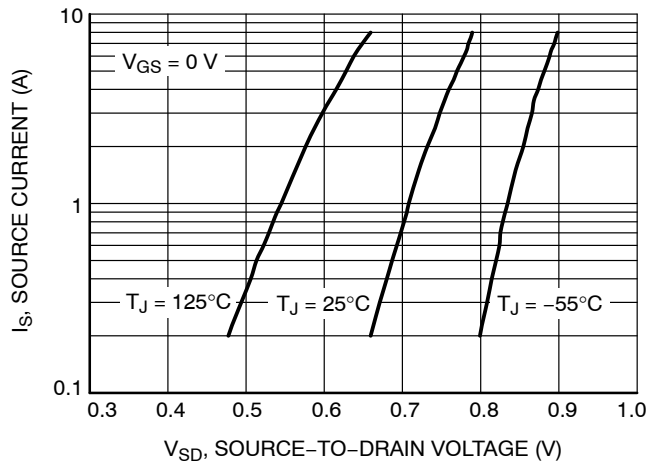


Figure 10. Diode Forward Voltage vs. Current

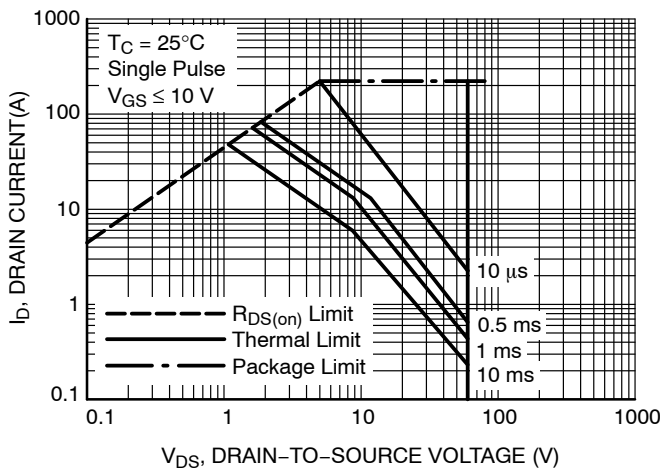


Figure 11. Maximum Rated Forward Biased Safe Operating Area

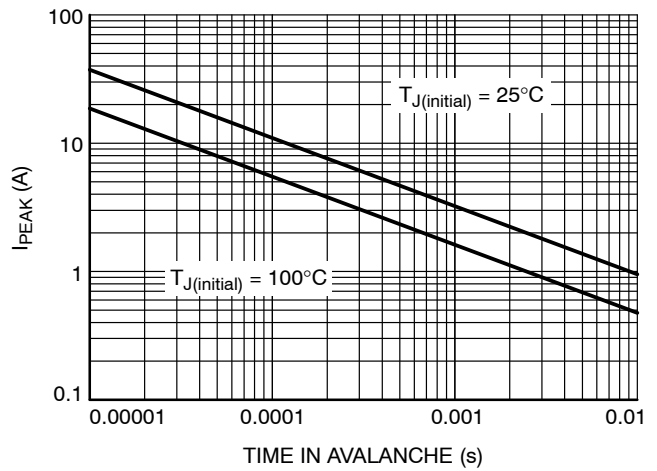


Figure 12. IPEAK vs. Time in Avalanche

NVMFS5H610NL

TYPICAL CHARACTERISTICS (continued)

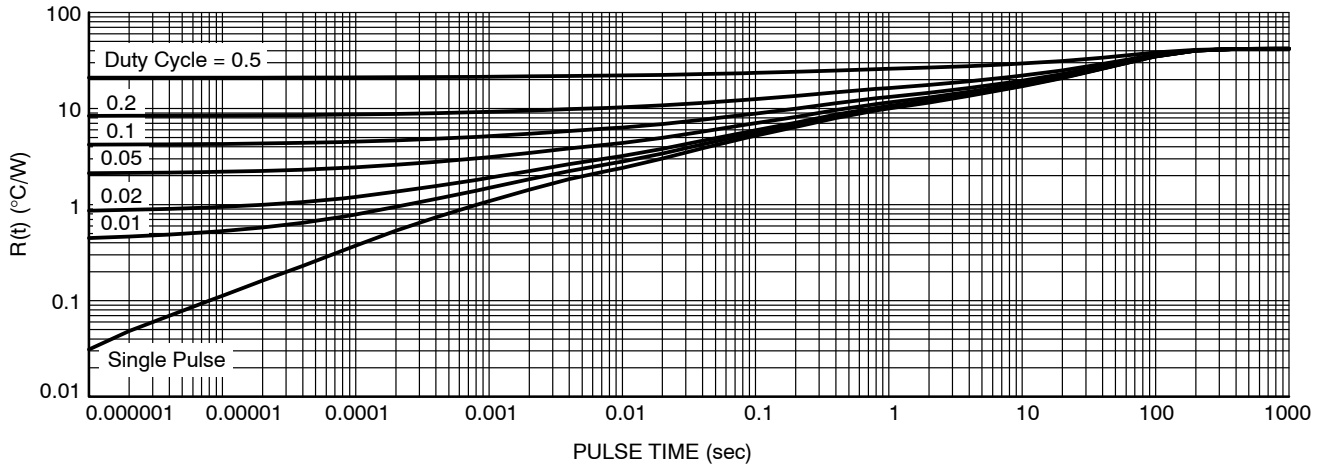


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVMFS5H610NLWFT1G	610LWF	DFNW5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

DISCONTINUED (Note 6)

NVMFS5H610NLT1G	5H610L	DFN5 (Pb-Free)	1500 / Tape & Reel
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[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

6. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



1
SCALE 2:1

DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE N

DATE 25 JUN 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



- STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
- STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



DFNW5 5x6 (FULL-CUT SO8FL WF) CASE 507BA ISSUE A

DATE 03 FEB 2021



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.150 REF		
M	3.00	3.40	3.80
θ	0°	---	12°



GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 W = Work Week
 ZZ = Lot Traceability
- *This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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