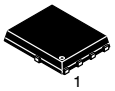
MOSFET – Power, Single N-Channel, DFN5/DFNW5

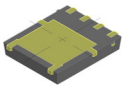
60 V, 250 A, 1.3 mΩ

NVMFS5H600NL

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
60 V	1.3 mΩ @ 10 V	250 A
	1.7 mΩ @ 4.5 V	



DFN5
CASE 506EZ

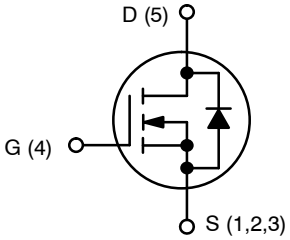


DFNW5
CASE 507BA

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

N−CHANNEL MOSFET



MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Symbol	Parameter			Value	Unit
V_{DSS}	Drain−to−Source Voltage			60	V
V_{GS}	Gate−to−Source Voltage			±20	V
I_D	Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	T_C = 25°C	250	A
			T_C = 100°C	160	
P_D	Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	160	W
			T_C = 100°C	63	
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T_A = 25°C	35	A
			T_A = 100°C	22	
P_D	Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		T_A = 25°C	3.3	W
			T_A = 100°C	1.3	
I_{DM}	Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		900	A
T_J, T_{stg}	Operating Junction and Storage Temperature			−55 to + 175	°C
I_S	Source Current (Body Diode)			170	A
E_{AS}	Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 26 A)			338	mJ
T_L	Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			260	°C

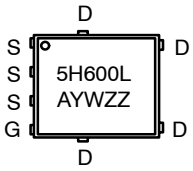
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction−to−Case − Steady State	0.80	°C/W
$R_{\theta JA}$	Junction−to−Ambient − Steady State (Note 2)	38	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

MARKING DIAGRAM



5H600L = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
$V_{(BR)DSS}$	Drain−to−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA		60			V
$V_{(BR)DSS}/T_J$	Drain−to−Source Breakdown Voltage Temperature Coefficient				34.3		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25 °C			10	μA
			T_J = 125°C			250	
I_{GSS}	Gate−to−Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
$V_{GS(TH)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA		1.2		2.0	V
$V_{GS(TH)}/T_J$	Threshold Temperature Coefficient				−5.0		mV/°C
$R_{DS(on)}$	Drain−to−Source On Resistance	V_{GS} = 10 V	I_D = 50 A		1.1	1.3	mΩ
		V_{GS} = 4.5 V	I_D = 50 A		1.4	1.7	
g_{FS}	Forward Transconductance	V_{DS} =15 V, I_D = 50 A			280		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
C_{ISS}	Input Capacitance	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 30 V			6680		pF
C_{OSS}	Output Capacitance				1230		
C_{RSS}	Reverse Transfer Capacitance				30		
Q_{OSS}	Output Charge	V_{GS} = 0 V, V_{DD} = 30 V			100		nC
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = 4.5 V, V_{DS} = 30 V; I_D = 50 A			40		
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = 10 V, V_{DS} = 30 V; I_D = 50 A			89		
$Q_{G(TH)}$	Threshold Gate Charge	V_{GS} = 4.5 V, V_{DS} = 30 V; I_D = 50 A			11		
Q_{GS}	Gate−to−Source Charge				20		
Q_{GD}	Gate−to−Drain Charge				6.5		
V_{GP}	Plateau Voltage				3.0		V
SWITCHING CHARACTERISTICS (Note 5)							
$t_{d(ON)}$	Turn−On Delay Time	V_{GS} = 4.5 V, V_{DS} = 30 V, I_D = 50 A, R_G = 2.5 Ω			28		ns
t_r	Rise Time				130		
$t_{d(OFF)}$	Turn−Off Delay Time				88		
t_f	Fall Time				160		
DRAIN−SOURCE DIODE CHARACTERISTICS							
V_{SD}	Forward Diode Voltage	V_{GS} = 0 V, I_S = 50 A	T_J = 25°C		0.77	1.2	V
			T_J = 125°C		0.63		
t_{RR}	Reverse Recovery Time	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 50 A			72		ns
t_a	Charge Time				36		
t_b	Discharge Time				36		
Q_{RR}	Reverse Recovery Charge				60		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

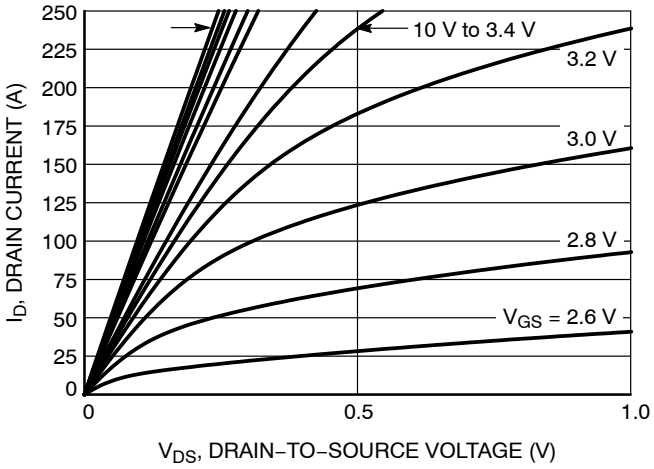


Figure 1. On−Region Characteristics

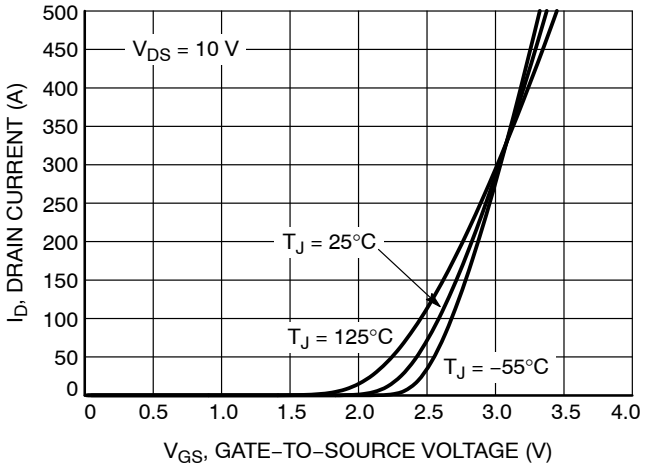


Figure 2. Transfer Characteristics

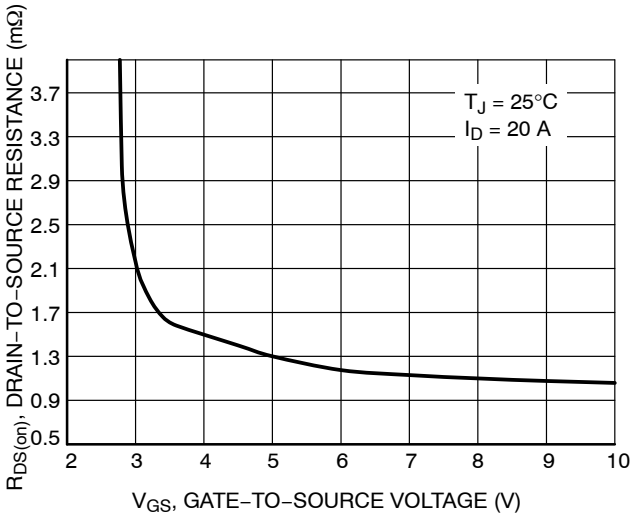


Figure 3. On−Resistance vs. Gate−to−Source Voltage

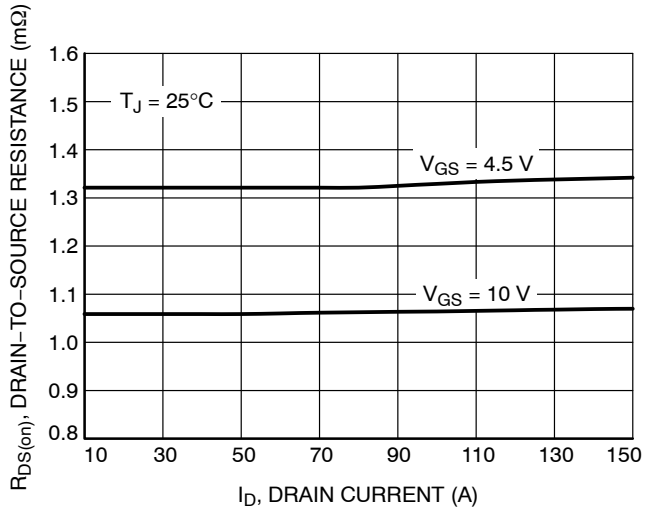


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

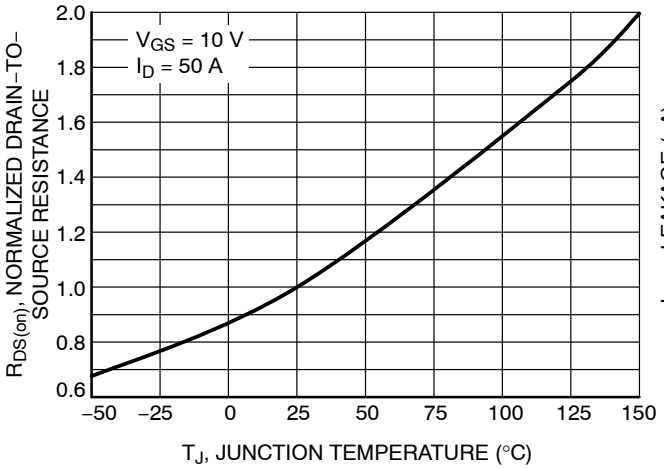


Figure 5. On−Resistance Variation with Temperature

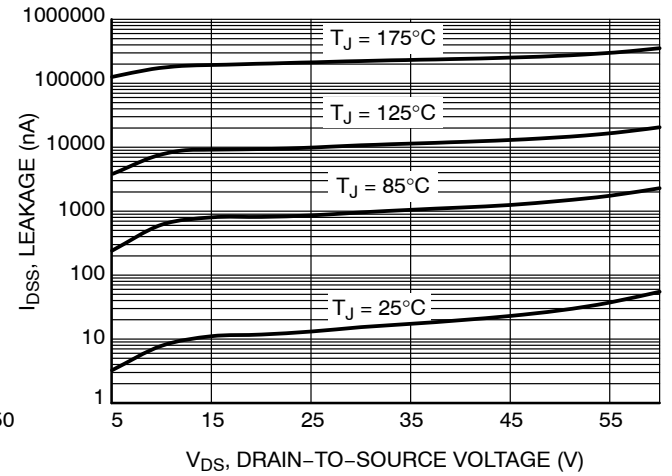


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS (continued)

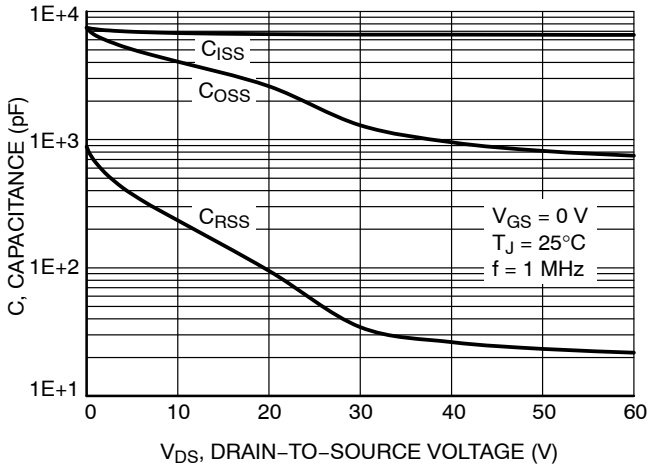


Figure 7. Capacitance Variation

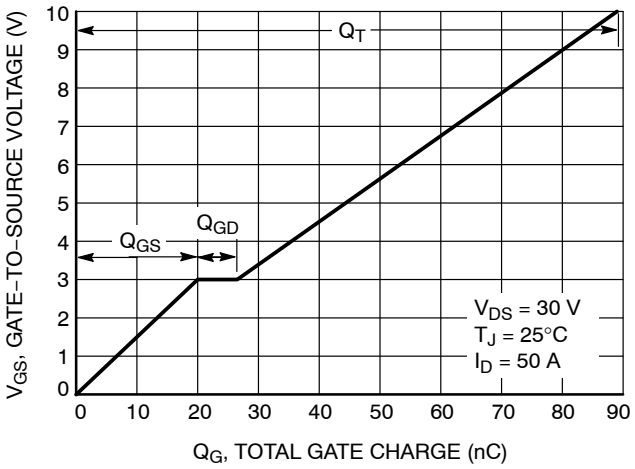


Figure 8. Gate−to−Source Voltage vs. Total Charge

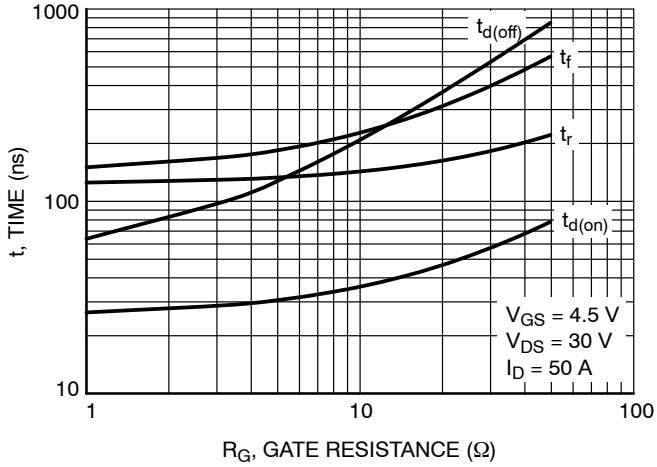


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

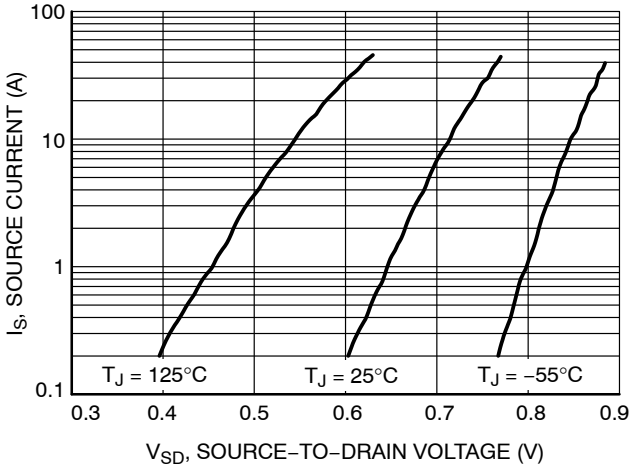


Figure 10. Diode Forward Voltage vs. Current

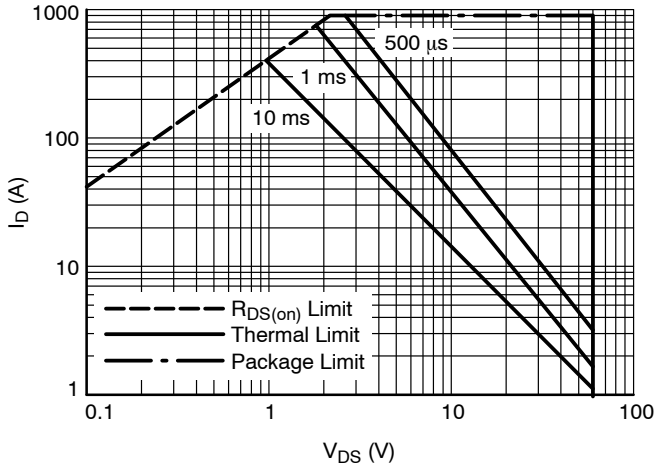


Figure 11. Safe Operating Area

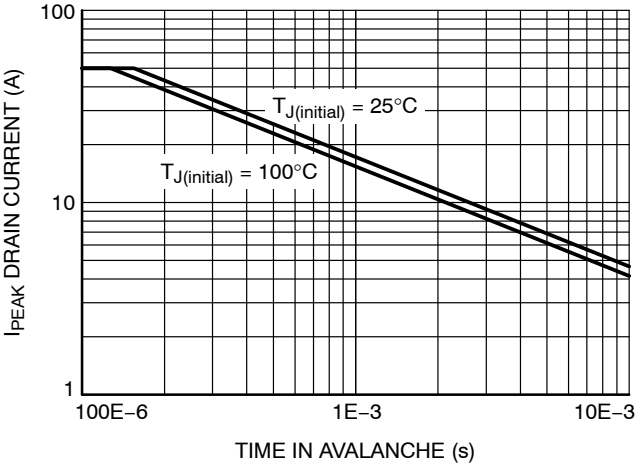


Figure 12. I_{PEAK} vs. Time in Avalanche

TYPICAL CHARACTERISTICS (continued)

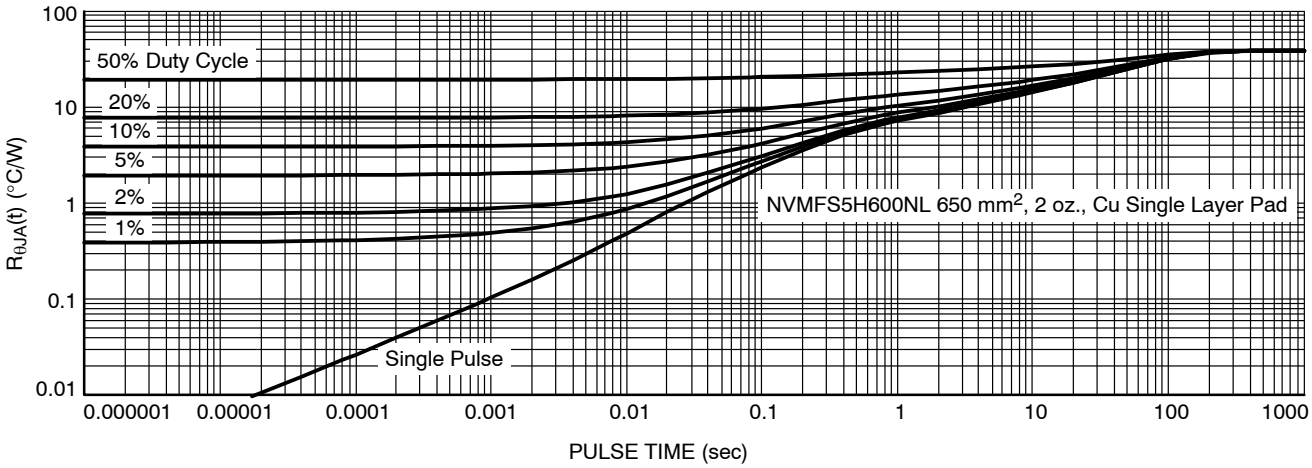


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Case	Marking	Package	Shipping†
NVMFS5H600NLT1G	506EZ	5H600L	DFN5 (Pb−Free)	1500 / Tape & Reel

DISCONTINUED (Note 6)

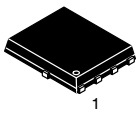
NVMFS5H600NLT3G	506EZ	5H600L	DFN5 (Pb−Free)	5000 / Tape & Reel
NVMFS5H600NLWFT1G	507BA	600LWF	DFNW5 (Pb−Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

6. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®



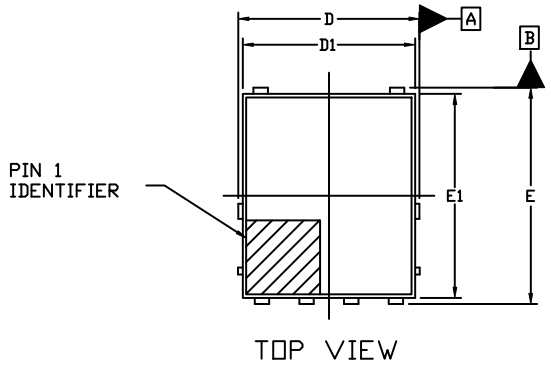
SCALE 2:1

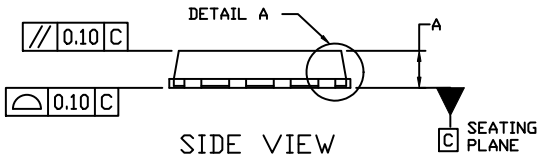
DFN5 5x6, 1.27P (SO−8FL)
CASE 506EZ
ISSUE A

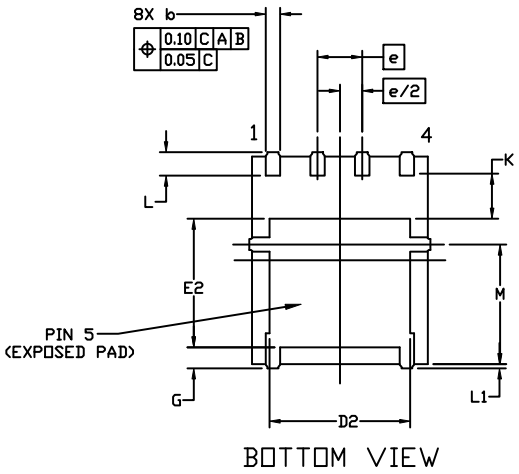
DATE 25 AUG 2021

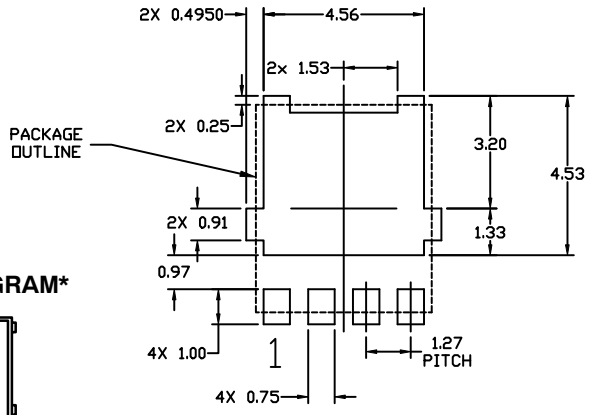
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.80	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
k	1.10	1.20	1.40
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°



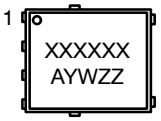






* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

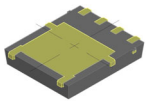
GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

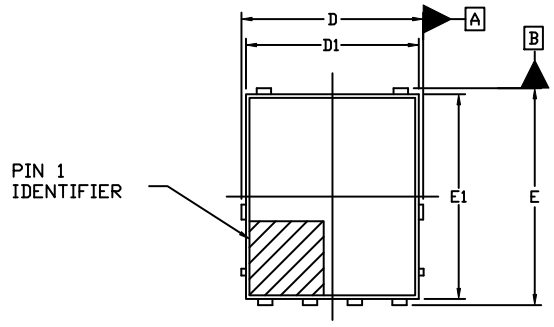
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

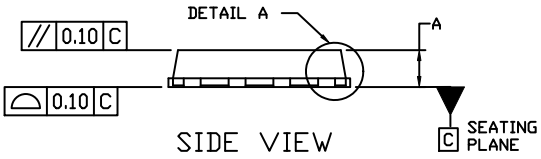
DOCUMENT NUMBER:	**98AON24855H**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**DFN5 5x6, 1.27P (SO−8FL)**	**PAGE 1 OF 1**

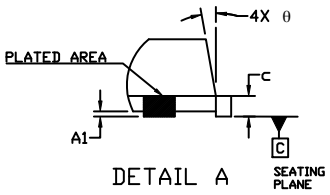


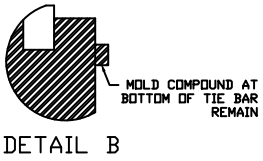
DFNW5 5x6 (FULL−CUT SO8FL WF)
CASE 507BA
ISSUE A

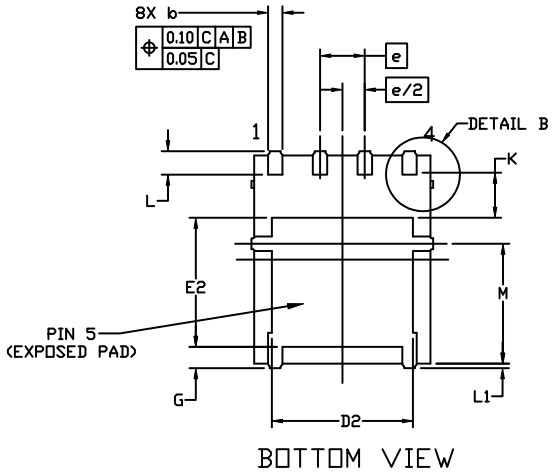
DATE 03 FEB 2021





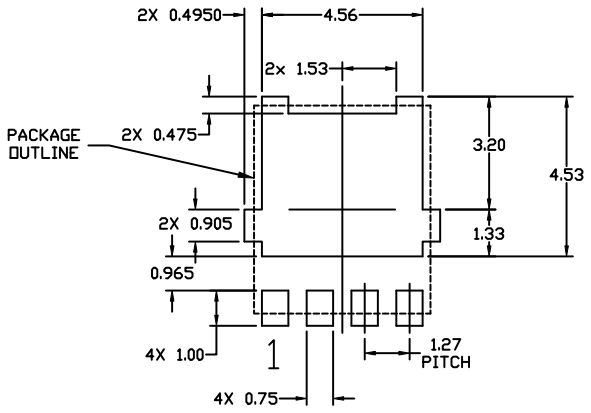






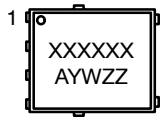
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.150 REF		
M	3.00	3.40	3.80
θ	0°	---	12°



* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



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*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON26450H**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**DFNW5 5x6 (FULL−CUT SO8FL WF)**	**PAGE 1 OF 1**

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