

NVMFS5A160PLZ

MOSFET – Power, Single P-Channel

-60 V, -100 A, 7.7 mΩ



ON Semiconductor®

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Features

- Small Footprint (5 x 6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- NVMFS5A160PLZWF: Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

| V_{DSS} | $R_{DS(on)}$ MAX | I_D MAX |
|-----------|------------------|-----------|
| -60 V | 7.7 mΩ @ -10 V | -100 A |
| | 10.5 mΩ @ -4.5 V | |

SPECIFICATION MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (Notes 1, 2, 3)

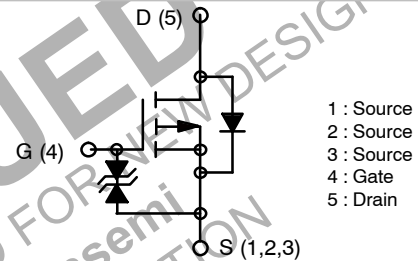
| Symbol | Parameter | Value | Unit | |
|----------------|--|---|------|---------------------------------|
| V_{DSS} | Drain to Source Voltage | -60 | V | |
| V_{GS} | Gate to Source Voltage | ±20 | V | |
| I_D | Continuous Drain, Current $R_{\theta JC}$, (Notes 1, 3) | $T_C = 25^\circ\text{C}$ -100 | A | |
| P_D | Power Dissipation $R_{\theta JC}$ (Note 1) | | | $T_C = 25^\circ\text{C}$ 200 |
| I_D | Continuous Drain: Current $R_{\theta JA}$ (Notes 1, 2, 3) | $T_A = 25^\circ\text{C}$ -15 | A | |
| P_D | Power Dissipation $R_{\theta JA}$ (Note 1, 2) | | | $T_A = 25^\circ\text{C}$ 3.8 |
| I_{DP} | Pulsed Drain Current | $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$ | -400 | A |
| T_J, T_{STG} | Operating Junction and Storage Temperature | -55 to +175 | | $^\circ\text{C}$ |
| I_S | Source Current (Body Diode) | -100 | | A |
| E_{AS} | Single Pulse Drain to Source Avalanche Energy ($L = 1.0 \text{ mH}$, $I_{L(pk)} = -26 \text{ A}$) | 335 | | mJ |
| T_L | Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | 260 | | $^\circ\text{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

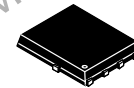
THERMAL CHARACTERISTICS

| Symbol | Parameter | Value | Unit |
|-----------------|---|-------|--------------------|
| $R_{\theta JC}$ | Junction to Case Steady State | 0.75 | $^\circ\text{C/W}$ |
| $R_{\theta JA}$ | Junction to Ambient Steady State (Note 3) | 39 | |

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

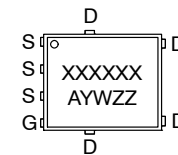


P-CHANNEL MOSFET



DFN5 (SO-8FL)

MARKING DIAGRAM



- XXXXXX = Specific Device Code
5A160L(NVMFS5A160PLZ)
160LWF(NVMFS5A160PLZWF)
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

NVMFS5A160PLZ

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---------------|-----------------------------------|---|---------------------------------------|-----|----------|---------------|
| $V_{(BR)DSS}$ | Drain to Source Breakdown Voltage | $I_D = -1\text{ mA}, V_{GS} = 0\text{ V}$ | -60 | | | V |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = -60\text{ V}, V_{GS} = 0\text{ V}$ | $T_J = 25^\circ\text{C}$ | | -1.0 | μA |
| | | | $T_J = 100^\circ\text{C}$ (Note 4) | | -100 | μA |
| I_{GSS} | Gate to Source Leakage Current | $V_{GS} = \pm 16\text{ V}, V_{DS} = 0\text{ V}$ | | | ± 10 | μA |

ON CHARACTERISTICS (Note 5)

| | | | | | | |
|--------------|-------------------------------|---|----------------------|-----|------|-----------|
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS} = -10\text{ V}, I_D = -1\text{ mA}$ | -1.2 | | -2.6 | V |
| $R_{DS(on)}$ | Drain to Source On Resistance | $V_{GS} = -10\text{ V}$ | $I_D = -50\text{ A}$ | 5.8 | 7.7 | $m\Omega$ |
| | | $V_{GS} = -4.5\text{ V}$ | $I_D = -50\text{ A}$ | 7.3 | 10.5 | |
| g_{FS} | Forward Transconductance | $V_{DS} = -10\text{ V}, I_D = -50\text{ A}$ | | 119 | | S |

CHARGES, CAPACITANCES & GATE RESISTANCE

| | | | | | | |
|--------------|------------------------------|---|--|------|--|-------------|
| C_{iss} | Input Capacitance | $V_{GS} = 0\text{ V}, f = 1\text{ MHz}$ $V_{DS} = -20\text{ V},$ | | 7700 | | pF |
| C_{oss} | Output Capacitance | | | 720 | | |
| C_{rss} | Reverse Transfer Capacitance | | | 540 | | |
| $Q_{g(tot)}$ | Total Gate Charge | $V_{GS} = -10\text{ V}, I_D = -50\text{ A}$ $V_{DS} = -36\text{ V},$ | | 160 | | nC |
| Q_{gs} | Gate to Source Charge | | | 24 | | |
| Q_{gd} | Gate to Drain Charge | | | 45 | | |

SWITCHING CHARACTERISTICS (Note 6)

| | | | | | | |
|--------------|---------------------|--|--|-----|--|-------------|
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DS} = -36\text{ V}, I_D = -50\text{ A},$ $V_{GS} = -10\text{ V},$ $R_G = 50\ \Omega$ | | 50 | | ns |
| t_r | Rise Time | | | 690 | | |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 645 | | |
| t_f | Fall Time | | | 643 | | |

DRAIN-SOURCE DIODE CHARACTERISTICS

| | | | | | | |
|----------|-------------------------|---|--|-------|------|----|
| V_{SD} | Forward Diode Voltage | $V_{GS} = 0\text{ V}, I_S = -50\text{ A}$ | | -0.83 | -1.5 | V |
| t_{rr} | Reverse Recovery Time | $V_{GS} = 0\text{ V}, I_S = -50\text{ A}$ | | 93 | | ns |
| Q_{rr} | Reverse Recovery Charge | $di/dt = 100\text{ A}/\mu\text{s}$ | | 218 | | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at $T_J = 100^\circ\text{C}$. Product is not tested to this condition in production.

5. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

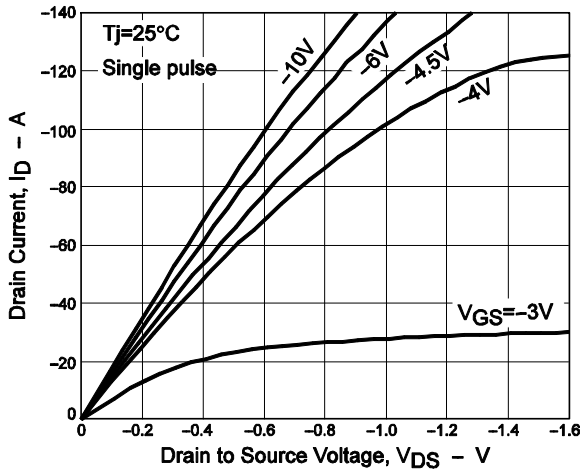


Figure 1. $I_D - V_{DS}$

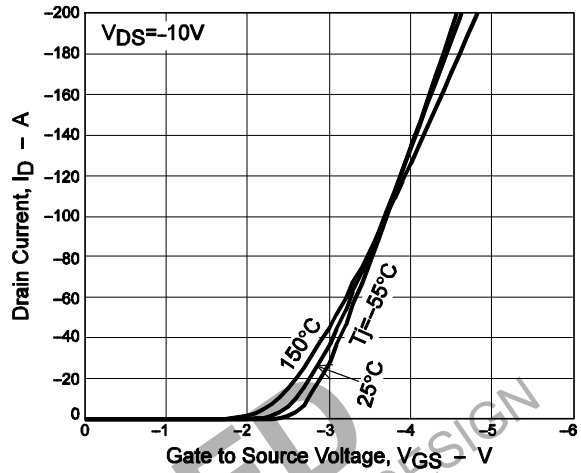


Figure 2. $I_D - V_{GS}$

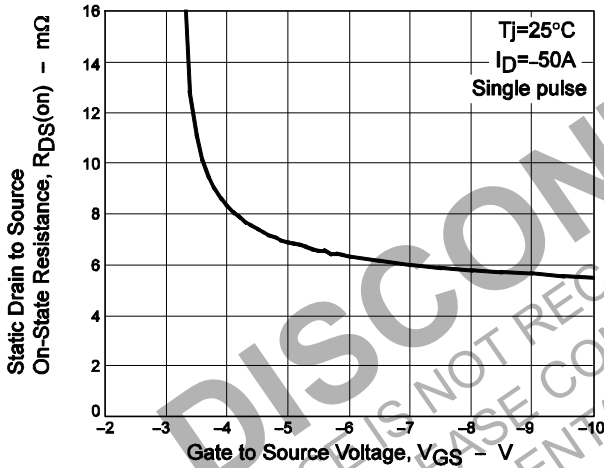


Figure 3. $R_{DS(on)} - V_{GS}$

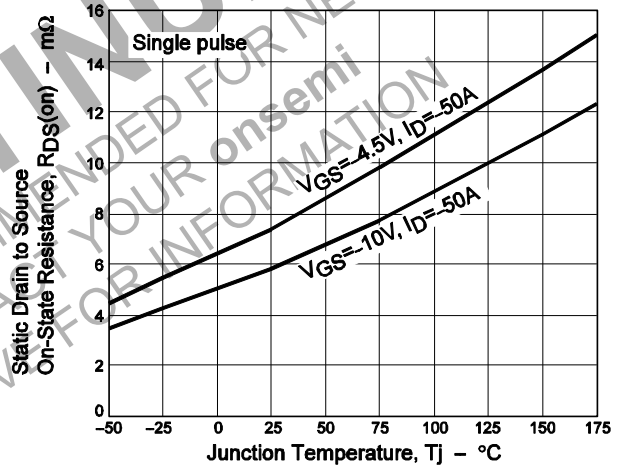


Figure 4. $R_{DS(on)} - T_J$

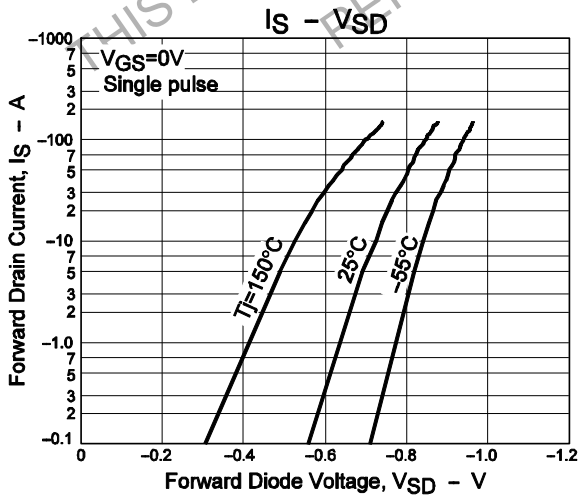


Figure 5. $I_S - V_{SD}$

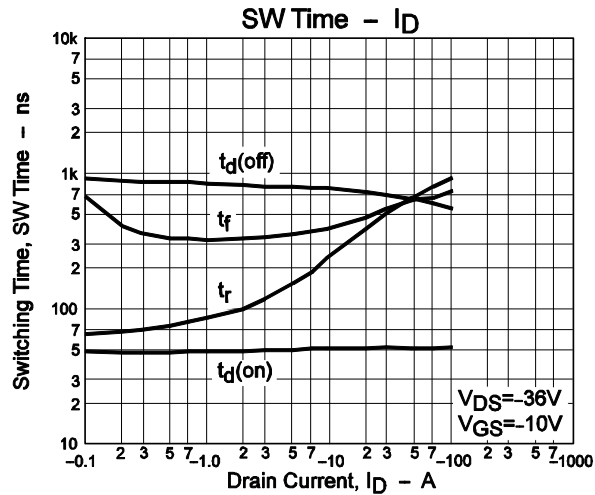


Figure 6. SW Time - I_D

NVMFS5A160PLZ

TYPICAL CHARACTERISTICS

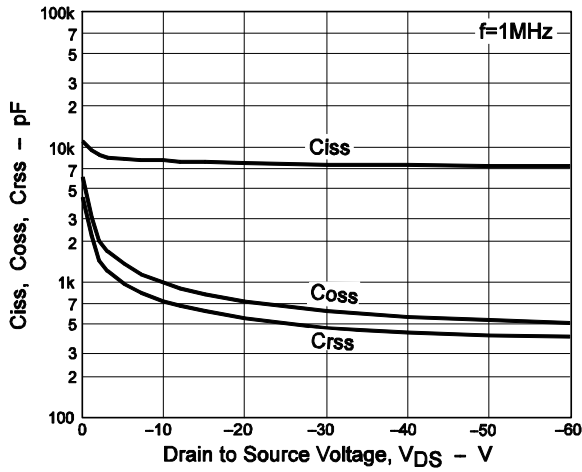


Figure 7. C_{iss} , C_{oss} , C_{rss} - V_{DS}

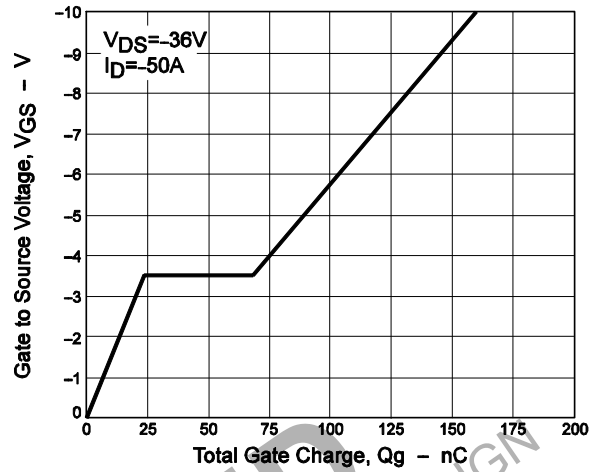


Figure 8. V_{GS} - Q_g

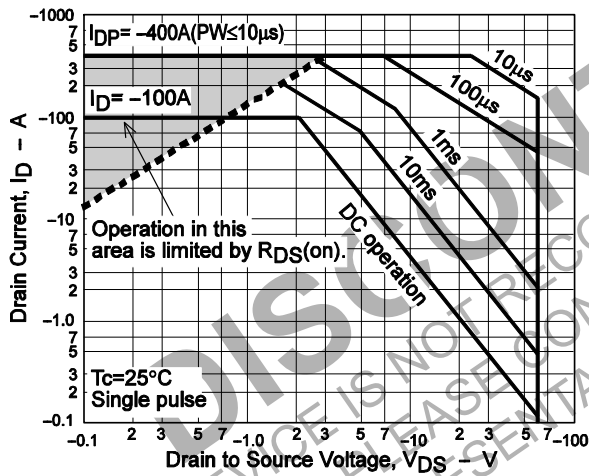


Figure 9. SOA

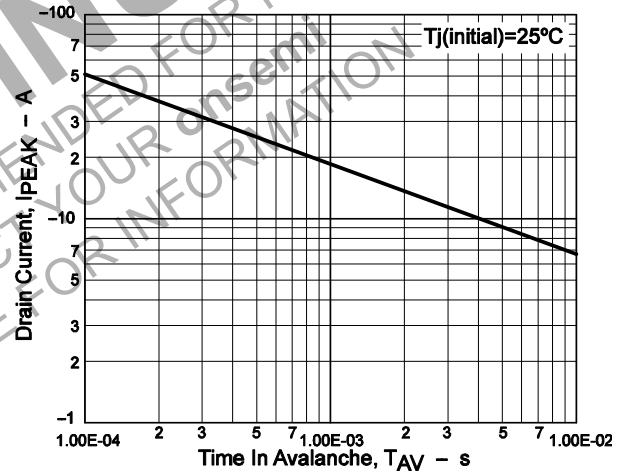


Figure 10. I_{PEAK} - T_{AV}

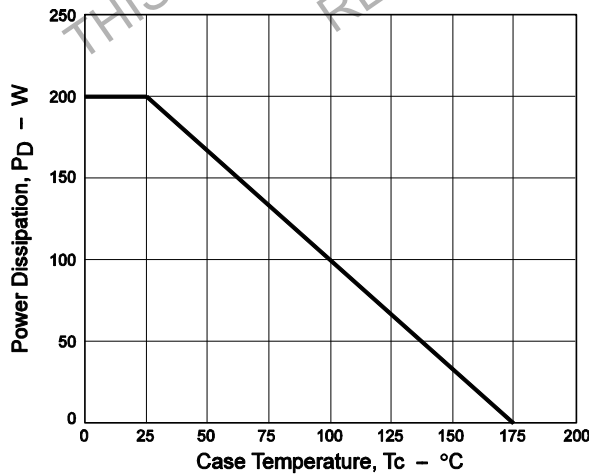


Figure 11. P_D - T_C

NVMFS5A160PLZ

TYPICAL CHARACTERISTICS

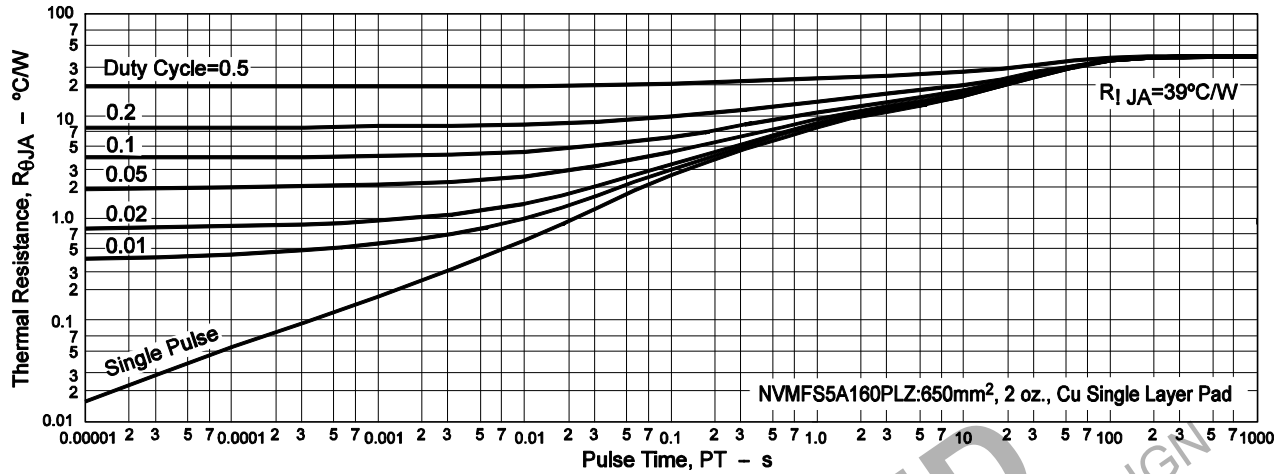
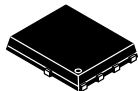


Figure 12. $R_{\theta JA}$ - Pulse Time

ORDERING INFORMATION

| Device | Marking | Package | Shipping (Qty / Packing) [†] |
|--------------------|---------|--|---------------------------------------|
| NVMFS5A160PLZT1G | 5A160L | DFN5 5x6, 1.27P (SO-8FL) (Pb-Free) | 1.500 / Tape & Reel |
| NVMFS5A160PLZWFT1G | 160LWF | DFN5 5x6, 1.27P (SO-8FL) (Pb-Free, Wettable Flanks) | 1.500 / Tape & Reel |
| NVMFS5A160PLZT3G | 5A160L | DFN5 5x6, 1.27P (SO-8FL) (Pb-Free) | 5.000 / Tape & Reel |
| NVMFS5A160PLZWFT3G | 160LWF | DFN5 5x6, 1.27P (SO-8FL) (Pb-Free, Wettable Flanks) | 5.000 / Tape & Reel |

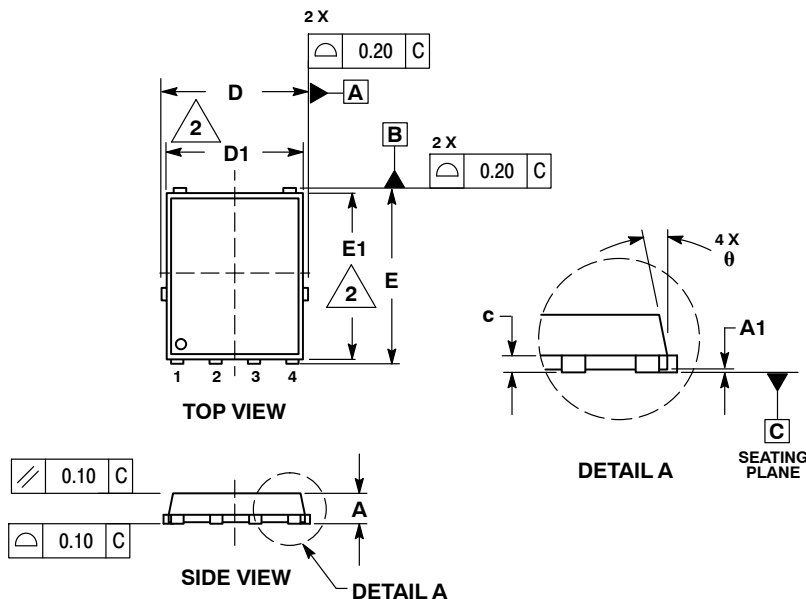
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



1
SCALE 2:1

DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE N

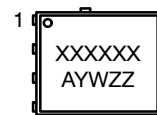
DATE 25 JUN 2018



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

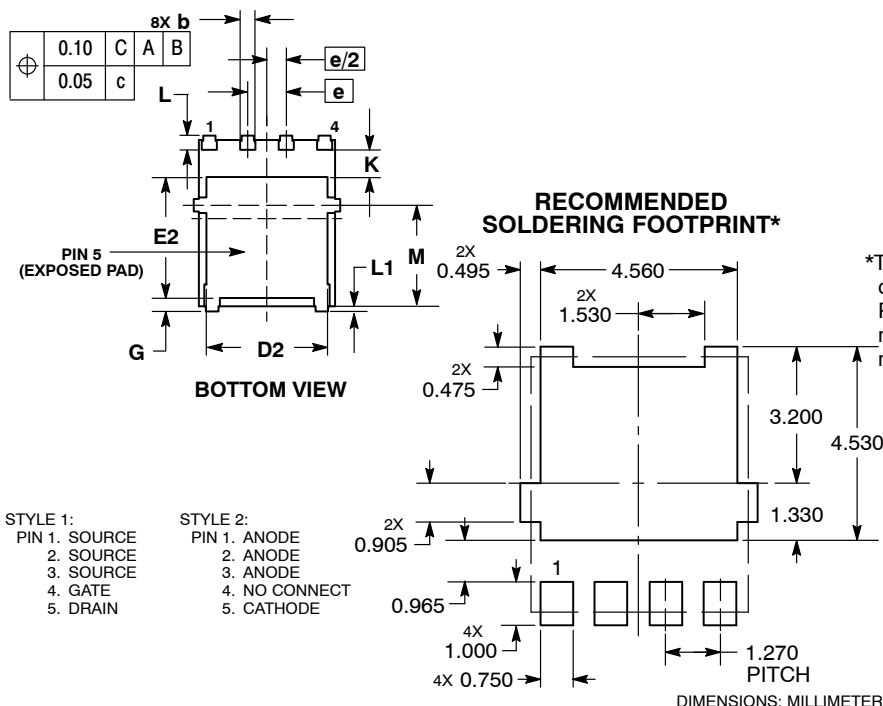
| DIM | MILLIMETERS | | |
|-----|-------------|-------|------|
| | MIN | NOM | MAX |
| A | 0.90 | 1.00 | 1.10 |
| A1 | 0.00 | --- | 0.05 |
| b | 0.33 | 0.41 | 0.51 |
| c | 0.23 | 0.28 | 0.33 |
| D | 5.00 | 5.15 | 5.30 |
| D1 | 4.70 | 4.90 | 5.10 |
| D2 | 3.80 | 4.00 | 4.20 |
| E | 6.00 | 6.15 | 6.30 |
| E1 | 5.70 | 5.90 | 6.10 |
| E2 | 3.45 | 3.65 | 3.85 |
| e | 1.27 BSC | | |
| G | 0.51 | 0.575 | 0.71 |
| K | 1.20 | 1.35 | 1.50 |
| L | 0.51 | 0.575 | 0.71 |
| L1 | 0.125 REF | | |
| M | 3.00 | 3.40 | 3.80 |
| θ | 0° | --- | 12° |

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



- STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
- STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|------------------|--------------------------|--|
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| DESCRIPTION: | DFN5 5x6, 1.27P (SO-8FL) | PAGE 1 OF 1 |

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