

MOSFET - Power, Dual N-Channel, DUAL SO8FL

60 V, 20.3 mΩ, 27 A



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NVMFD020N06C

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFWD020N06C – Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

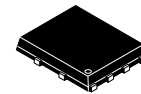
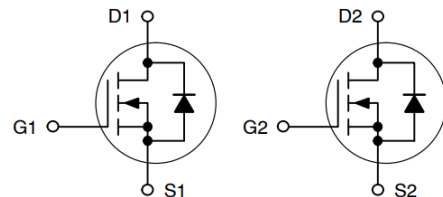
Parameter		Symbol	Value	Units	
Drain-to-Source Voltage		V_{DSS}	60	V	
Gate-to-Source Voltage		V_{GS}	± 20	V	
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	I_D	$T_C = 25^\circ\text{C}$	27	A
			$T_C = 100^\circ\text{C}$	19	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	P_D	$T_C = 25^\circ\text{C}$	31	W
			$T_C = 100^\circ\text{C}$	15	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	I_D	$T_A = 25^\circ\text{C}$	8	A
			$T_A = 100^\circ\text{C}$	6	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	P_D	$T_A = 25^\circ\text{C}$	3.1	W
			$T_A = 100^\circ\text{C}$	1.5	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM}	98	A	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +175	$^\circ\text{C}$	
Source Current (Body Diode)		I_S	25	A	
Single Pulse Drain-to-Source Avalanche Energy ($I_L = 5.7 \text{ A}_{pk}$)		E_{AS}	16	mJ	
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

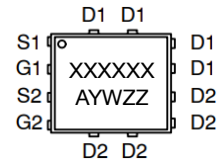
$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
60 V	20.3 mΩ @ 10 V	27 A

Dual N-Channel



DFN8 5x6
(SO8FL)
CASE 506BT

MARKING DIAGRAM



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

NVMFD020N06C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case – Steady State (Note 2)	$R_{\theta JC}$	4.8	°C/W
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	47	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS} / T_J$	$I_D = 250\ \mu\text{A}$, ref to 25°C		29		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 60\text{ V}$	$T_J = 25^\circ\text{C}$		10	μA
			$T_J = 125^\circ\text{C}$		250	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 20\ \mu\text{A}$	2.0		4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)} / T_J$	$I_D = 20\ \mu\text{A}$, ref to 25°C		-7.8		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 4\text{ A}$		16.9	20.3	m Ω
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 4\text{ A}$		12		S
Gate Resistance	R_G	$T_A = 25^\circ\text{C}$		1.0		Ω

CHARGES & CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 30\text{ V}$		355		pF
Output Capacitance	C_{OSS}			260		
Reverse Capacitance	C_{RSS}			4.9		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 48\text{ V}, I_D = 4\text{ A}$		5.8		nC
Threshold Gate Charge	$Q_{G(TH)}$			1.4		
Gate-to-Source Charge	Q_{GS}			2.3		
Gate-to-Drain Charge	Q_{GD}			0.53		

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 48\text{ V}, I_D = 4\text{ A}, R_G = 6\ \Omega$		6.5		ns
Rise Time	t_r			1.4		
Turn-Off Delay Time	$t_{d(OFF)}$			9.7		
Fall Time	t_f			4.0		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 4\text{ A}$	$T_J = 25^\circ\text{C}$	0.81	1.2	V
			$T_J = 125^\circ\text{C}$	0.67		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, d_i/d_t = 100\text{ A}/\mu\text{s}, V_{DS} = 30\text{ V}, I_S = 4\text{ A}$		24		ns
Charge Time	t_a			12		
Discharge Time	t_b			12		
Reverse Recovery Charge	Q_{RR}			12		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

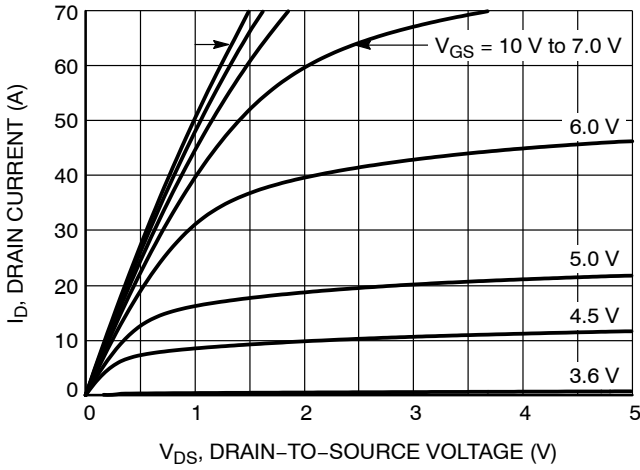


Figure 1. On-Region Characteristics

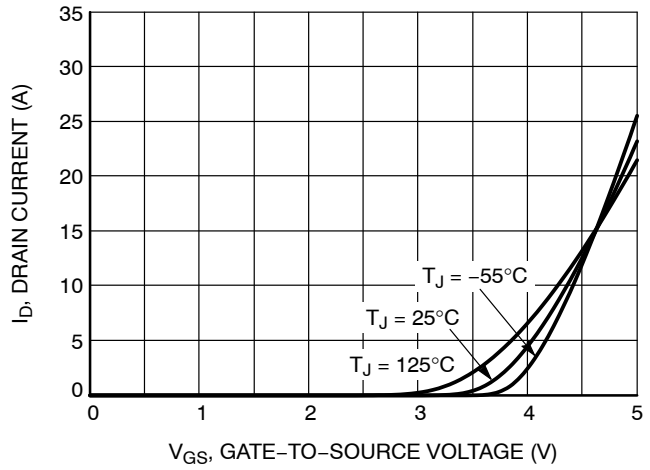


Figure 2. Transfer Characteristics

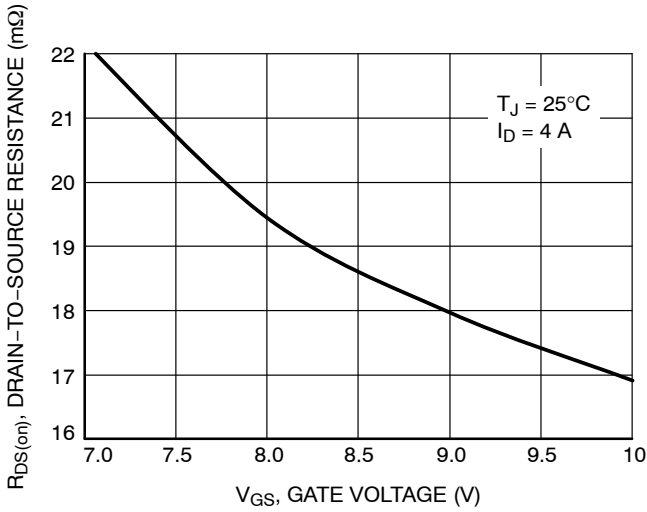


Figure 3. On-Resistance vs. Gate-to-Source Voltage

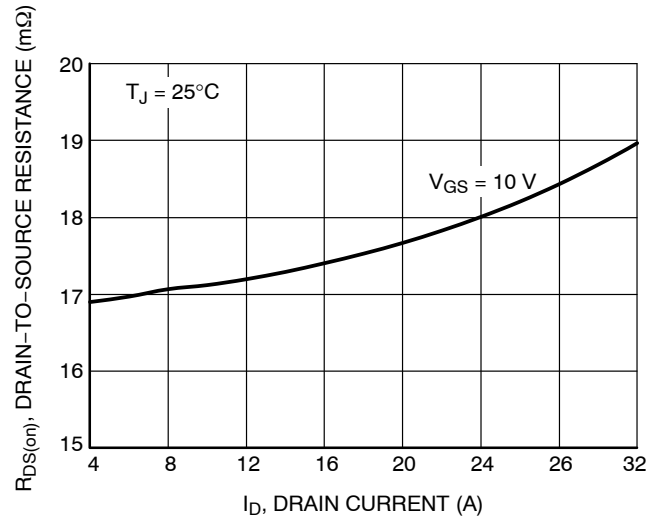


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

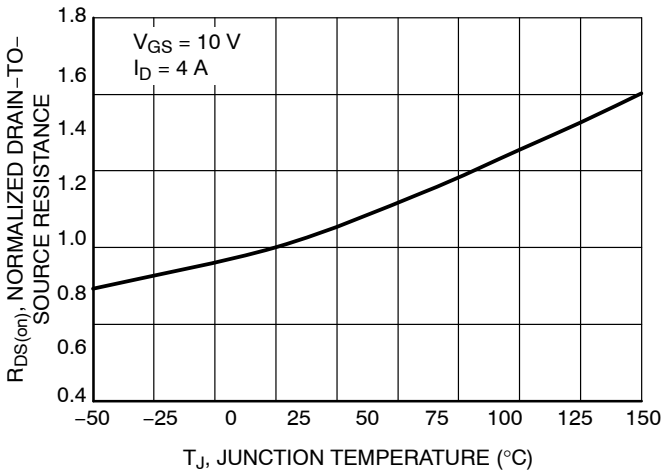


Figure 5. On-Resistance Variation with Temperature

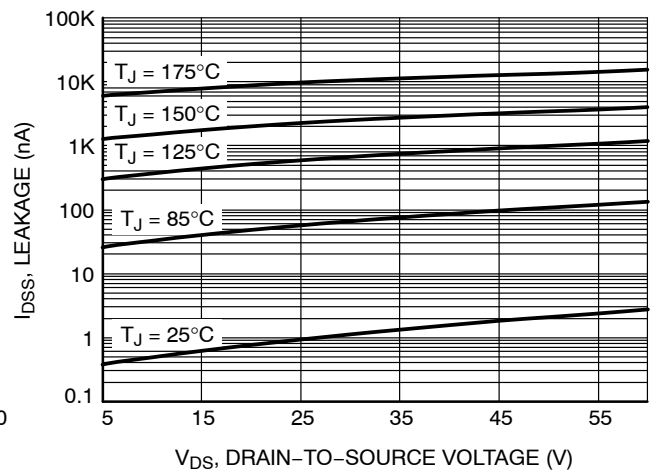


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NVMFD020N06C

TYPICAL CHARACTERISTICS

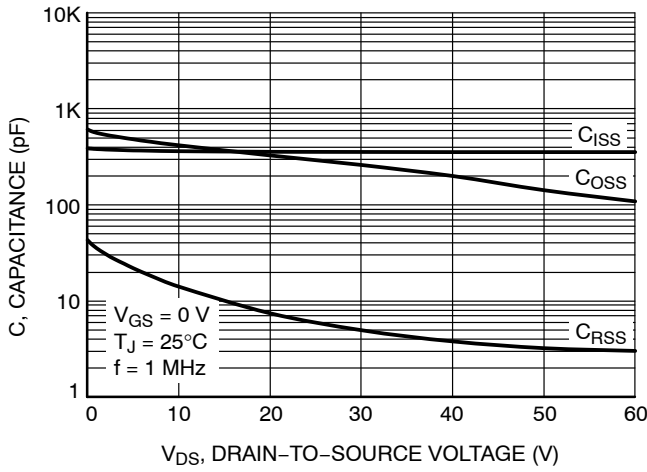


Figure 7. Capacitance Variation

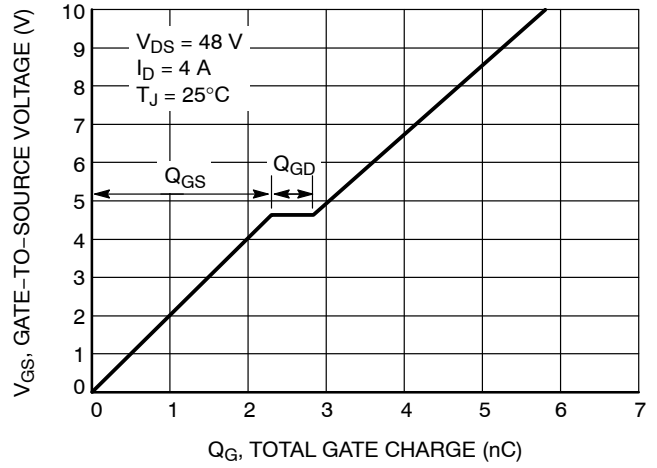


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

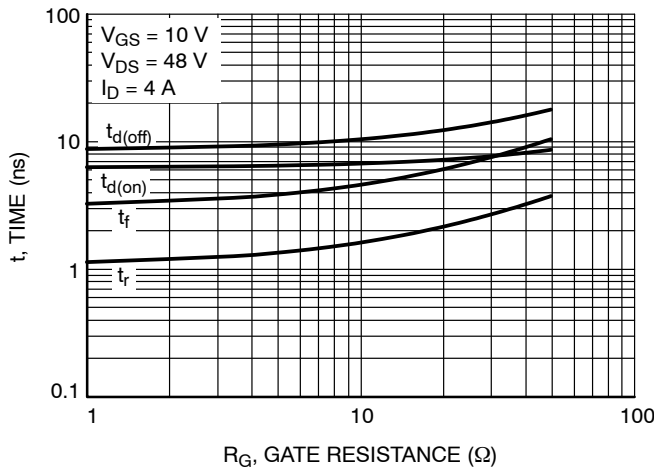


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

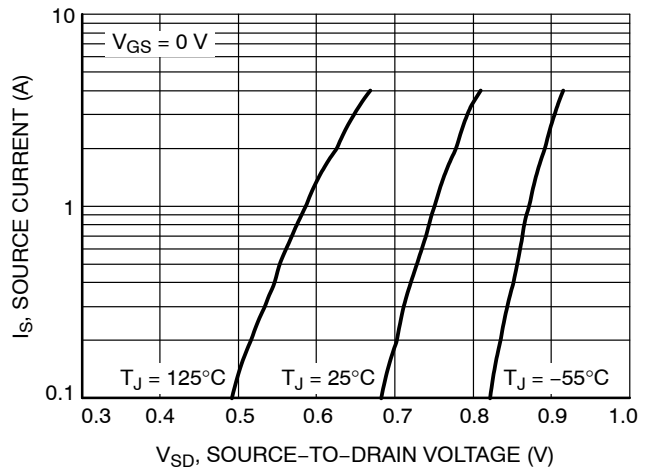


Figure 10. Diode Forward Voltage vs. Current

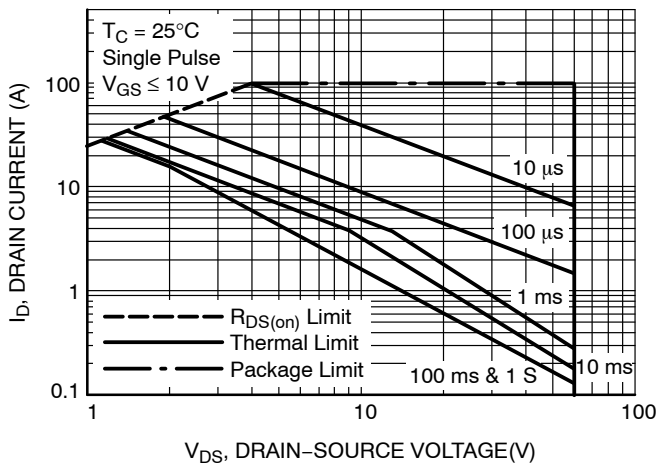


Figure 11. Safe Operating Area

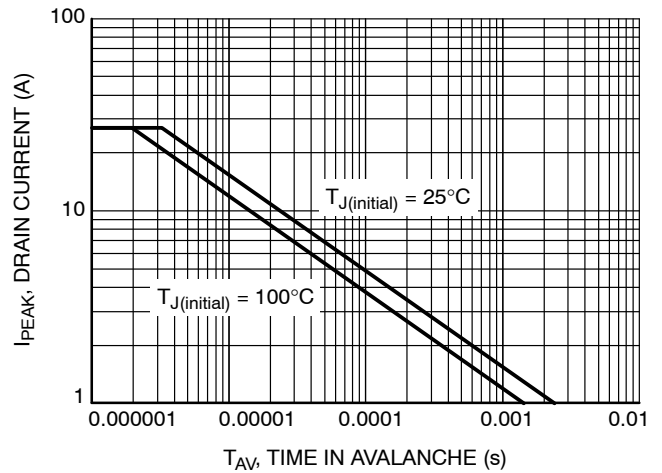


Figure 12. I_{PEAK} vs. Time in Avalanche

NVMFD020N06C

TYPICAL CHARACTERISTICS

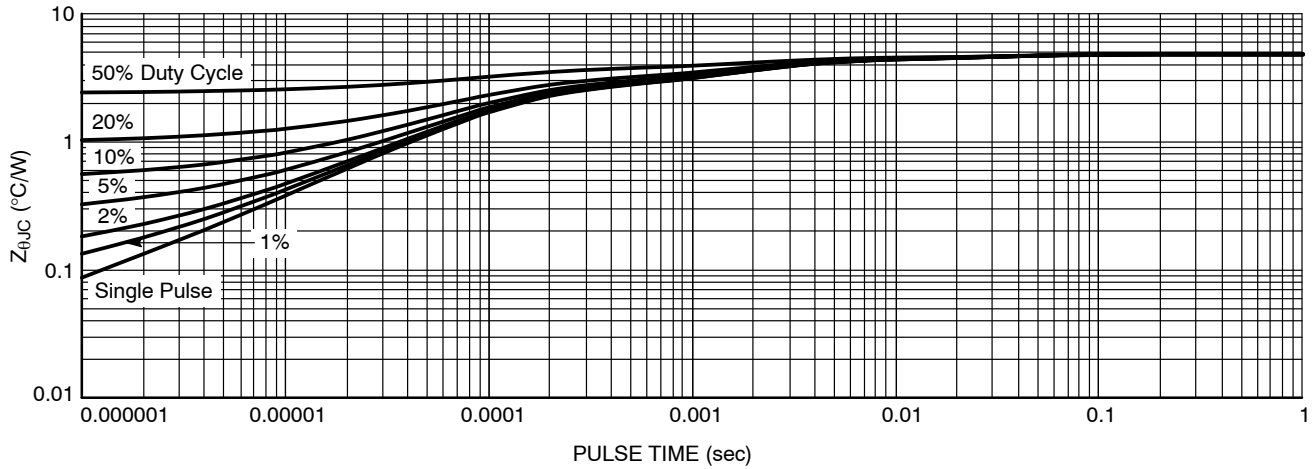


Figure 13. Thermal Response

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVMFD020N06CT1G	20DN6C	SO8FL Dual (Pb-Free)	1500 / Tape & Reel
NVMFWD020N06CT1G	20DN6W	SO8FL Dual (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

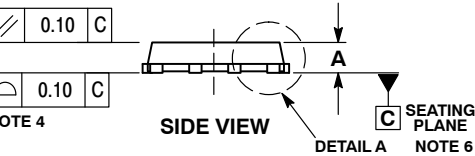
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

DFN8 5x6, 1.27P Dual Flag (SO8FL-Dual) CASE 506BT ISSUE F

DATE 23 NOV 2021



GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

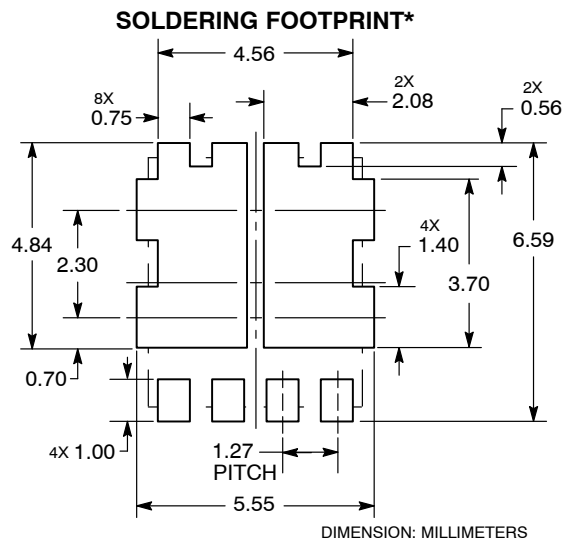
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. PROFILE TOLERANCE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. A VISUAL INDICATOR FOR PIN 1 MUST BE LOCATED IN THIS AREA.



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	---	1.10
A1	---	---	0.05
b	0.33	0.42	0.51
b1	0.33	0.42	0.51
c	0.20	---	0.33
D	5.15 BSC		
D1	4.70	4.90	5.10
D2	3.90	4.10	4.30
D3	1.50	1.70	1.90
E	6.15 BSC		
E1	5.70	5.90	6.10
E2	3.90	4.15	4.40
e	1.27 BSC		
G	0.45	0.55	0.65
h	---	---	12 °
K	0.51	---	---
K1	0.56	---	---
L	0.48	0.61	0.71
M	3.25	3.50	3.75
N	1.80	2.00	2.20



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DFN8 5X6, 1.27P DUAL FLAG (SO8FL-DUAL)	PAGE 1 OF 1

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