

NVBLS0D5N04M8

MOSFET – Power, Single, N-Channel

40 V, 300 A, 0.57 mΩ

Features

- Typical $R_{DS(on)}$ = 0.46 mΩ at $V_{GS} = 10$ V, $I_D = 80$ A
- Typical $Q_{g(tot)}$ = 220 nC at $V_{GS} = 10$ V, $I_D = 80$ A
- UIS Capability
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS $T_J = 25^\circ\text{C}$ unless otherwise noted

| Parameter | Symbol | Ratings | Units |
|---|-----------------|--------------|---------------------|
| Drain-to-Source Voltage | V_{DSS} | 40 | V |
| Gate-to-Source Voltage | V_{GS} | ± 20 | V |
| Drain Current – Continuous ($V_{GS} = 10$) (Note 1) | I_D | 300 | A |
| Pulsed Drain Current $T_C = 25^\circ\text{C}$ | | See Figure 4 | |
| Single Pulse Avalanche Energy (Note 2) | E_{AS} | 1064 | mJ |
| Power Dissipation | P_D | 429 | W |
| Derate Above 25°C | | 2.86 | W/ $^\circ\text{C}$ |
| Operating and Storage Temperature | T_J, T_{STG} | -55 to +175 | $^\circ\text{C}$ |
| Thermal Resistance, Junction-to-Case | $R_{\theta JC}$ | 0.35 | $^\circ\text{C/W}$ |
| Maximum Thermal Resistance, Junction-to-Ambient (Note 3) | $R_{\theta JA}$ | 43 | $^\circ\text{C/W}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by bondwire configuration.
2. Starting $T_J = 25^\circ\text{C}$, $L = 0.3$ mH, $I_{AS} = 84$ A, $V_{DD} = 40$ V during inductor charging and $V_{DD} = 0$ V during time in avalanche.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2 oz copper.

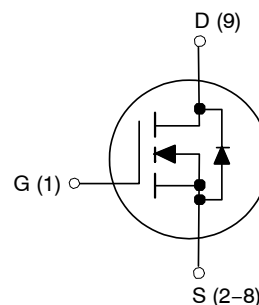


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**MO-299A
CASE 100CU**



ORDERING INFORMATION

| Device | Package | Marking |
|------------------|----------------------|----------|
| NVBLS0D5N04M8TXG | MO-299A (Pb-Free) | 0D5N04M8 |

NVBLS0D5N04M8

Table 1. ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units | |
|---|-----------------------------------|---|------------------------------------|-------|-----------|------------------|---------------|
| OFF CHARACTERISTICS | | | | | | | |
| B_{VDSS} | Drain-to-Source Breakdown Voltage | $I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$ | 40 | - | - | V | |
| I_{DSS} | Drain-to-Source Leakage Current | $V_{DS} = 40\ \text{V}$, $V_{GS} = 0\ \text{V}$ | $T_J = 25^\circ\text{C}$ | - | - | 1 | μA |
| | | | $T_J = 175^\circ\text{C}$ (Note 4) | - | - | 1 | mA |
| I_{GSS} | Gate-to-Source Leakage Current | $V_{GS} = \pm 20\ \text{V}$ | - | - | ± 100 | nA | |
| ON CHARACTERISTICS | | | | | | | |
| $V_{GS(th)}$ | Gate-to-Source Threshold Voltage | $V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$ | 2.0 | 3.0 | 4.0 | V | |
| $R_{DS(on)}$ | Drain-to-Source On Resistance | $I_D = 80\ \text{A}$, $V_{GS} = 10\ \text{V}$ | - | 0.46 | 0.57 | $\text{m}\Omega$ | |
| DYNAMIC CHARACTERISTICS | | | | | | | |
| C_{iss} | Input Capacitance | $V_{DS} = 25\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$ | - | 15900 | - | pF | |
| C_{oss} | Output Capacitance | | - | 4000 | - | pF | |
| C_{rss} | Reverse Transfer Capacitance | | - | 600 | - | pF | |
| R_g | Gate Resistance | $f = 1\ \text{MHz}$ | - | 2.6 | - | Ω | |
| $Q_{g(ToT)}$ | Total Gate Charge at 10 V | $V_{GS} = 0\ \text{to}\ 10\ \text{V}$ | - | 220 | 296 | nC | |
| $Q_{g(th)}$ | Threshold Gate Charge | $V_{GS} = 0\ \text{to}\ 2\ \text{V}$ | | | | | |
| Q_{gs} | Gate-to-Source Gate Charge | | - | 73 | - | nC | |
| Q_{gd} | Gate-to-Drain "Miller" Charge | | - | 41 | - | nC | |
| SWITCHING CHARACTERISTICS | | | | | | | |
| t_{on} | Turn-On Time | $V_{DD} = 20\ \text{V}$, $I_D = 80\ \text{A}$, $V_{GS} = 10\ \text{V}$, $R_{GEN} = 6\ \Omega$ | - | - | 221 | ns | |
| $t_{d(on)}$ | Turn-On Delay | | - | 54 | - | ns | |
| t_r | Rise Time | | - | 82 | - | ns | |
| $t_{d(off)}$ | Turn-Off Delay | | - | 106 | - | ns | |
| t_f | Fall Time | | - | 52 | - | ns | |
| t_{off} | Turn-Off Time | | - | - | 215 | ns | |
| DRAIN-SOURCE DIODE CHARACTERISTICS | | | | | | | |
| V_{SD} | Source-to-Drain Diode Voltage | $I_{SD} = 80\ \text{A}$, $V_{GS} = 0\ \text{V}$ | - | - | 1.25 | V | |
| | | $I_{SD} = 40\ \text{A}$, $V_{GS} = 0\ \text{V}$ | - | - | 1.2 | V | |
| t_{rr} | Reverse-Recovery Time | $I_F = 80\ \text{A}$, $dI_{SD}/dt = 100\ \text{A}/\mu\text{s}$, $V_{DD} = 32\ \text{V}$ | - | 119 | 133 | ns | |
| Q_{rr} | Reverse-Recovery Charge | | - | 228 | 274 | nC | |

4. The maximum value is specified by design at $T_J = 175^\circ\text{C}$. Product is not tested to this condition in production. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Typical Characteristics

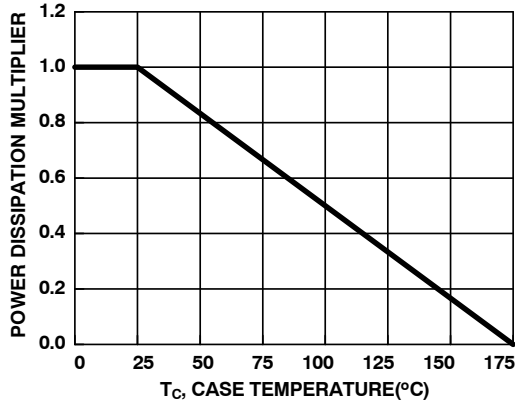


Figure 1. Normalized Power Dissipation vs. Case Temperature

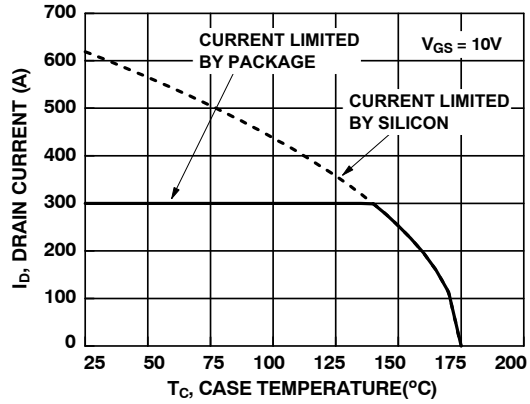


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

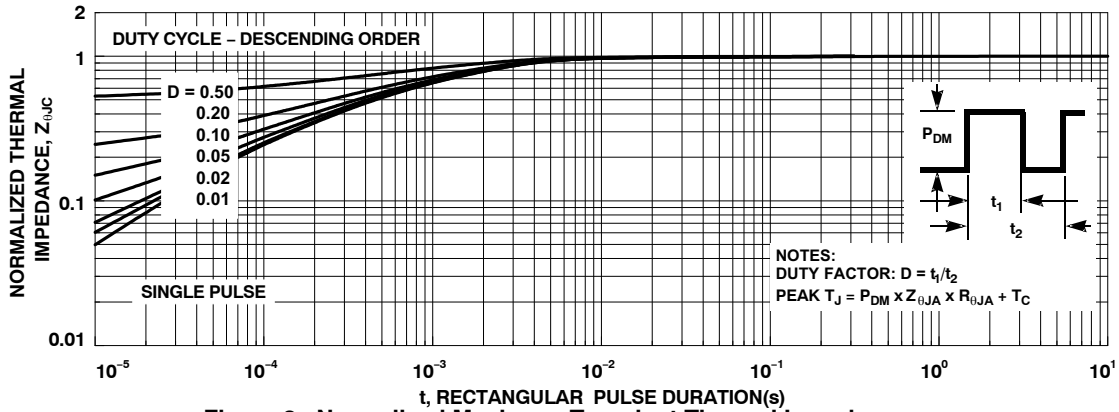


Figure 3. Normalized Maximum Transient Thermal Impedance

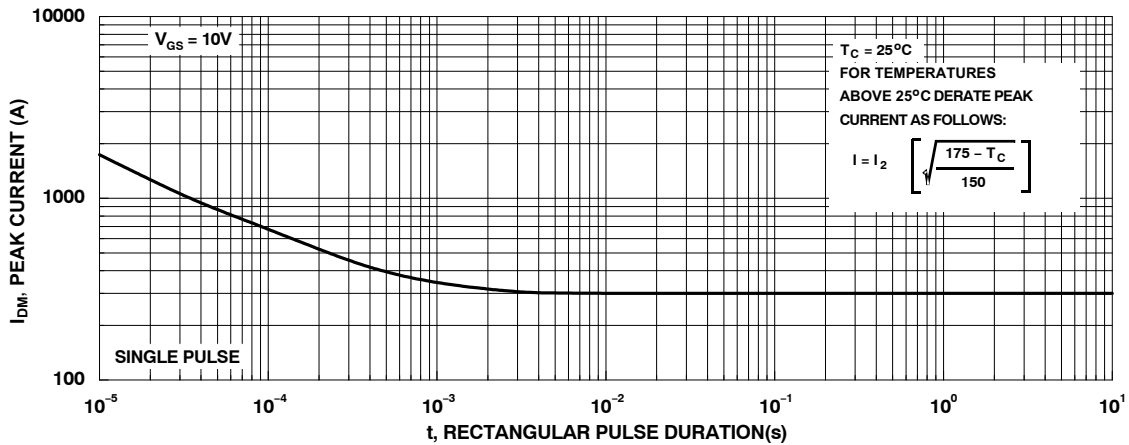


Figure 4. Peak Current Capability

Typical Characteristics

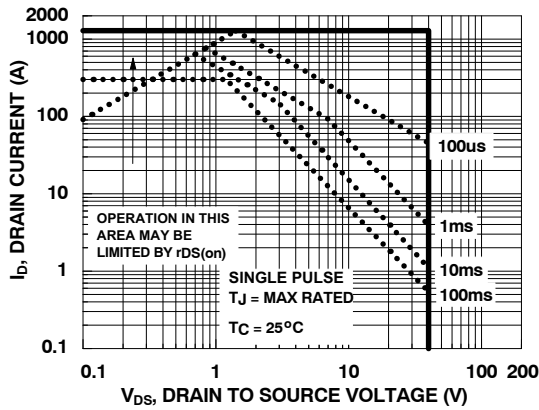
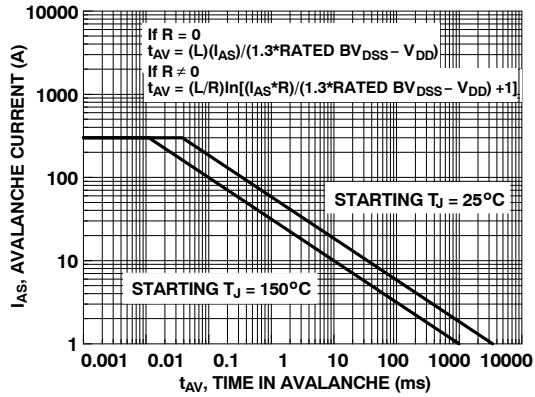


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

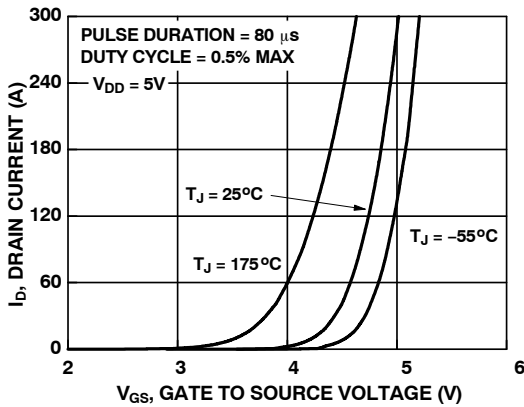


Figure 7. Transfer Characteristics

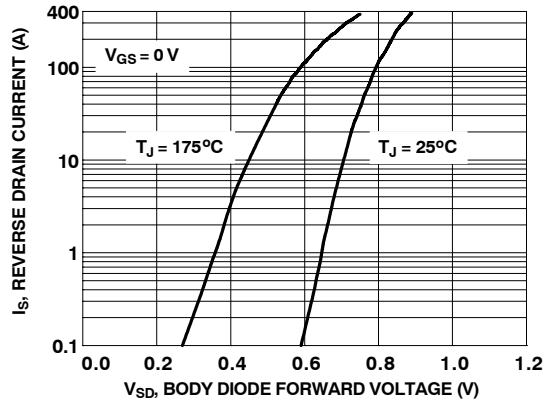


Figure 8. Forward Diode Characteristics

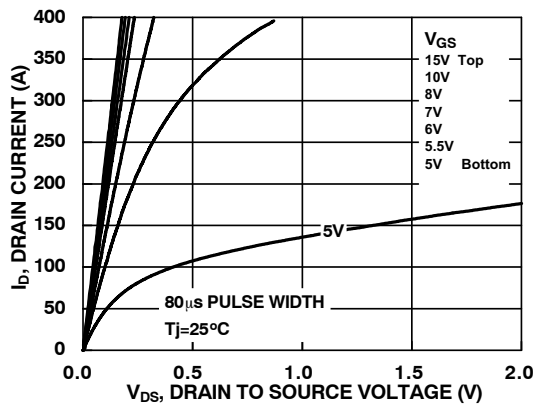


Figure 9. Saturation Characteristics

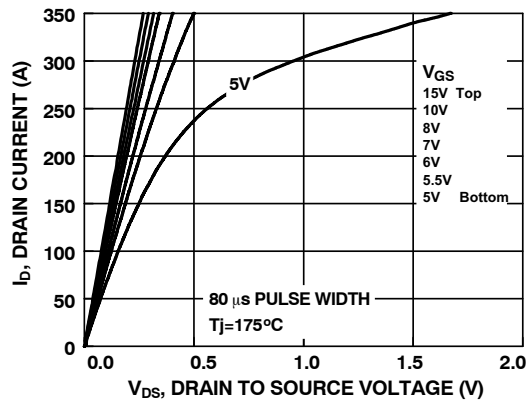


Figure 10. Saturation Characteristics

Typical Characteristics

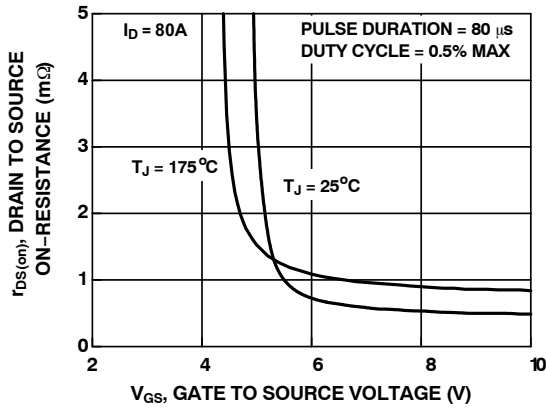


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

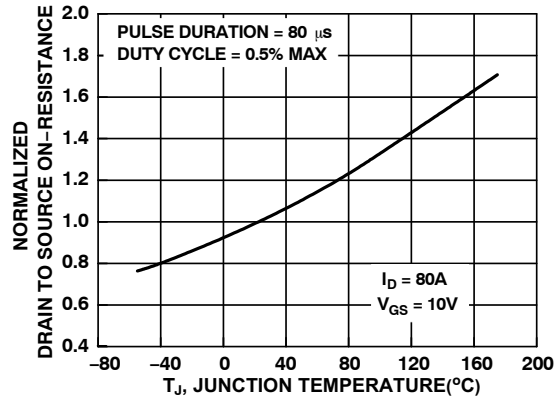


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

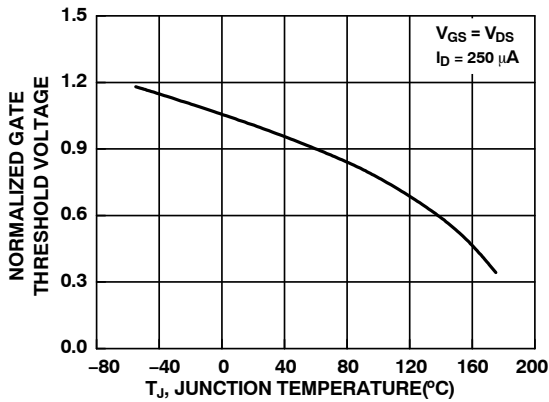


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

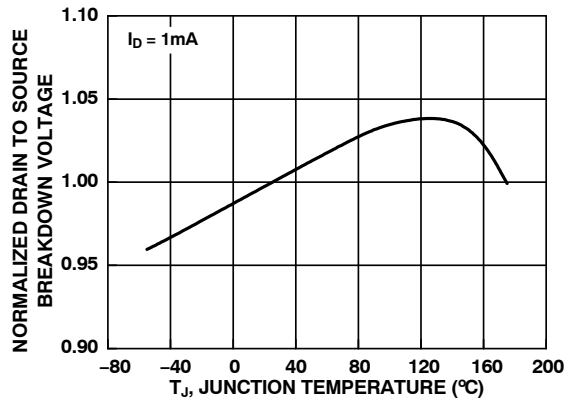


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

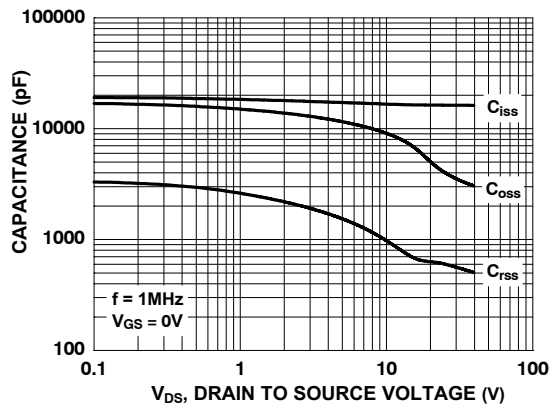


Figure 15. Capacitance vs. Drain to Source Voltage

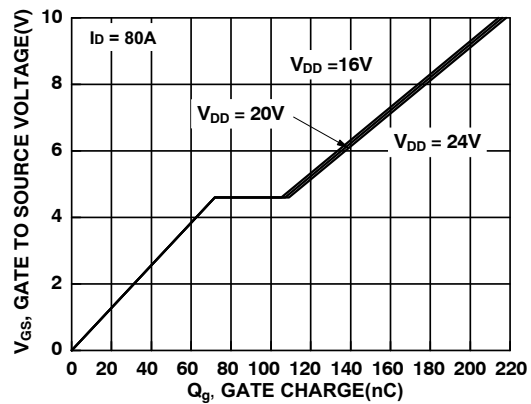


Figure 16. Gate Charge vs. Gate to Source Voltage

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