

MOSFET – Power, N-Channel, SUPERFET[®] III, Automotive, Easy-drive

650 V, 24 A, 125 mΩ



ON Semiconductor[®]

www.onsemi.com

NVB125N65S3

Description

SUPERFET III MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provides superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET Easy drive series helps manage EMI issues and allows for easier design implementation.

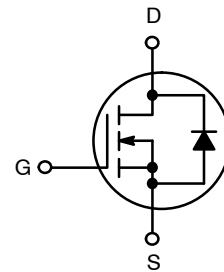
Features

- AEC-Q101 Qualified
- 700 V @ T_J = 150°C
- Typ. R_{DS(on)} = 105 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 46 nC)
- Low Effective Output Capacitance (Typ. C_{oss(eff.)} = 439 pF)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

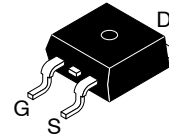
Applications

- Automotive On Board Charger
- Automotive DC/DC Converter for HEV

V _{DSS}	R _{DS(on)} MAX	I _D MAX
650 V	125 mΩ @ 10 V	24 A

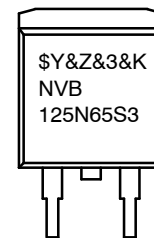


POWER MOSFET



D²PAK
CASE 418AJ

MARKING DIAGRAM



- \$Y = ON Semiconductor Logo
- &Z = Assembly Plant Code
- &3 = Data Code (Year & Week)
- &K = Lot
- NVB125N65S3 = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

NVB125N65S3

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

Symbol	Parameter	Value	Unit
V _{DSS}	Drain to Source Voltage	650	V
V _{GSS}	Gate to Source Voltage	- DC	±30
		- AC (f > 1 Hz)	±30
I _D	Drain Current	- Continuous (T _C = 25°C)	24
		- Continuous (T _C = 100°C)	15
I _{DM}	Drain Current	- Pulsed (Note 1)	60
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	115	mJ
I _{AS}	Avalanche Current (Note 2)	3.7	A
E _{AR}	Repetitive Avalanche Energy (Note 1)	1.81	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	20	
P _D	Power Dissipation	(T _C = 25°C)	181
		- Derate Above 25°C	1.45
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = 3.7 A, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 12 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 400 V, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max.	0.69	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, Max.	40	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Reel Size	Tape Width	Shipping†
NVB125N65S3	NVB125N65S3	D ² -PAK	330 mm	24 mm	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NVB125N65S3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	V _{GS} = 0 V, I _D = 1 mA, T _J = 25°C	650			V
		V _{GS} = 0 V, I _D = 1 mA, T _J = 150°C	700			V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 1 mA, Referenced to 25°C		0.68		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0 V			1	μA
		V _{DS} = 520 V, T _C = 125°C		1.35		
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±30 V, V _{DS} = 0 V			±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 0.59 mA	2.5		4.5	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 12 A		105	125	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 12 A		16		S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 400 V, V _{GS} = 0 V, f = 1 MHz		1940		pF
C _{oss}	Output Capacitance			40		pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		439		pF
C _{oss(er.)}	Energy Related Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		62		pF
Q _{g(tot)}	Total Gate Charge at 10 V	V _{DS} = 400 V, I _D = 12 A, V _{GS} = 10 V (Note 4)		46		nC
Q _{gs}	Gate to Source Gate Charge			12		nC
Q _{gd}	Gate to Drain "Miller" Charge			19		nC
ESR	Equivalent Series Resistance	f = 1 MHz		0.5		Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 400 V, I _D = 12 A, V _{GS} = 10 V, R _g = 4.7 Ω (Note 4)		21		ns
t _r	Turn-On Rise Time			19		ns
t _{d(off)}	Turn-Off Delay Time			48		ns
t _f	Turn-Off Fall Time			4.6		ns

SOURCE-DRAIN DIODE CHARACTERISTICS

I _S	Maximum Continuous Source to Drain Diode Forward Current			24		A
I _{SM}	Maximum Pulsed Source to Drain Diode Forward Current			60		A
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 12 A			1.2	V
t _{rr}	Reverse Recovery Time	V _{DD} = 400 V, I _{SD} = 12 A, dI _F /dt = 100 A/μs		339		ns
Q _{rr}	Reverse Recovery Charge				5.7	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS

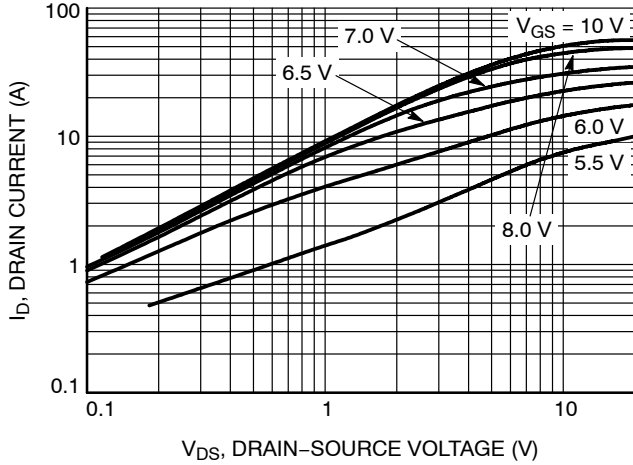


Figure 1. On-Region Characteristics
25°C

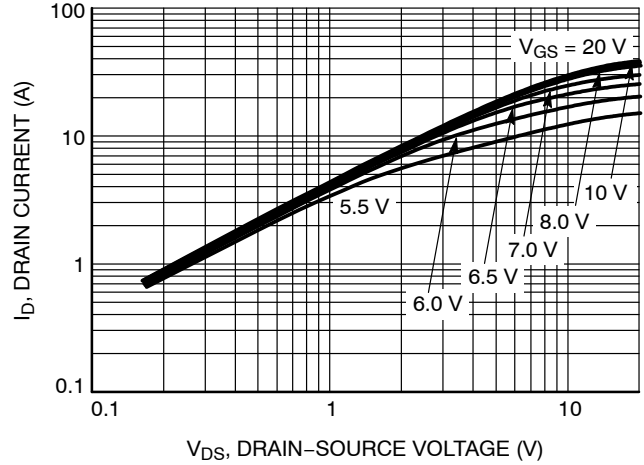


Figure 2. On-Region Characteristics
150°C

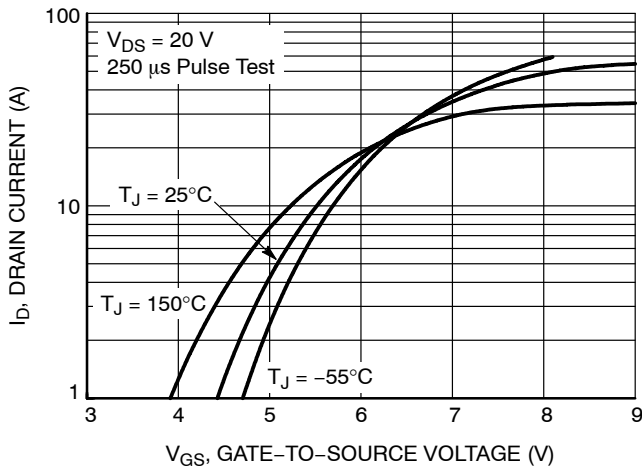


Figure 3. Transfer Characteristics

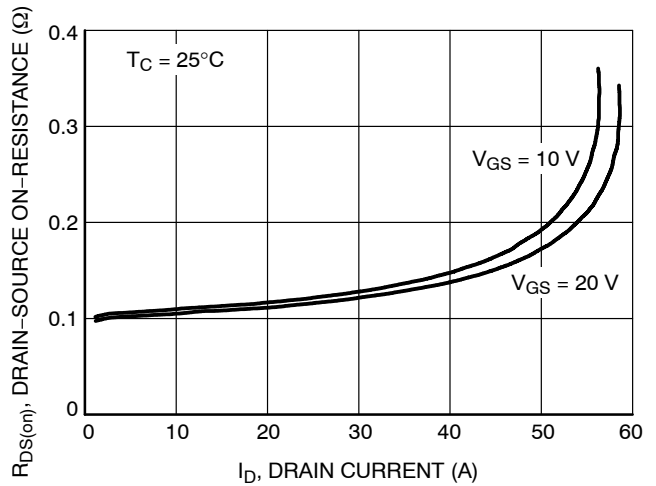


Figure 4. On-Resistance Variation vs. Drain Current and Gate Voltage

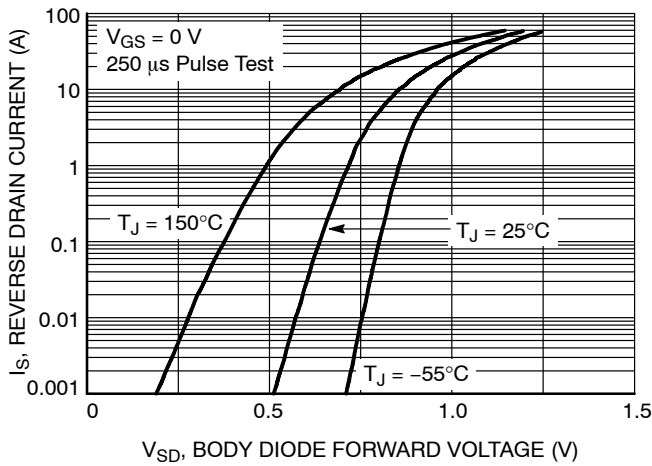


Figure 5. Body Diode Forward Voltage Variation vs. Source Current and Temperature

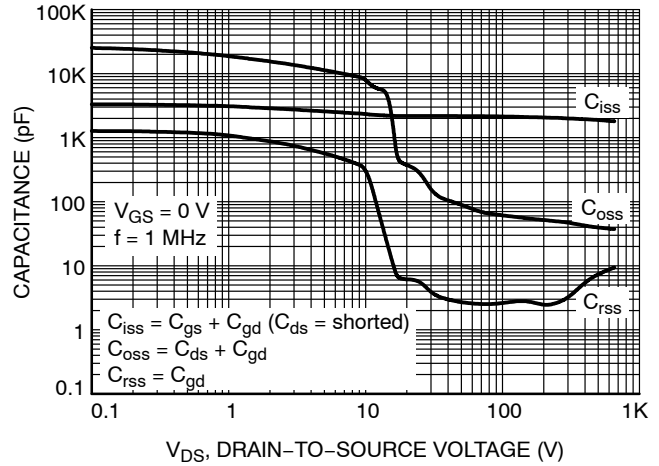


Figure 6. Capacitance Characteristics

TYPICAL CHARACTERISTICS

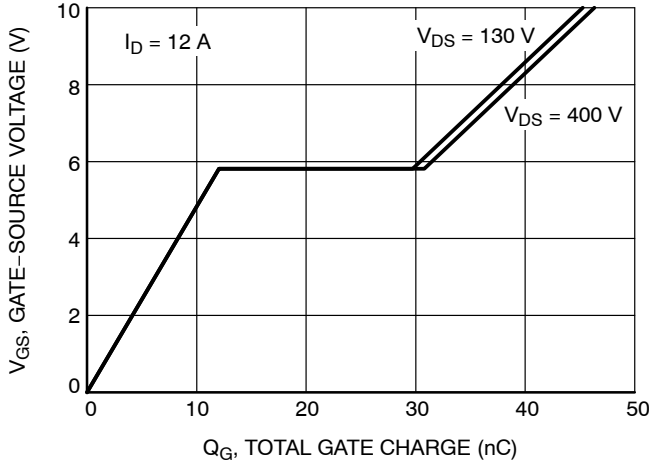


Figure 7. Gate Charge Characteristics

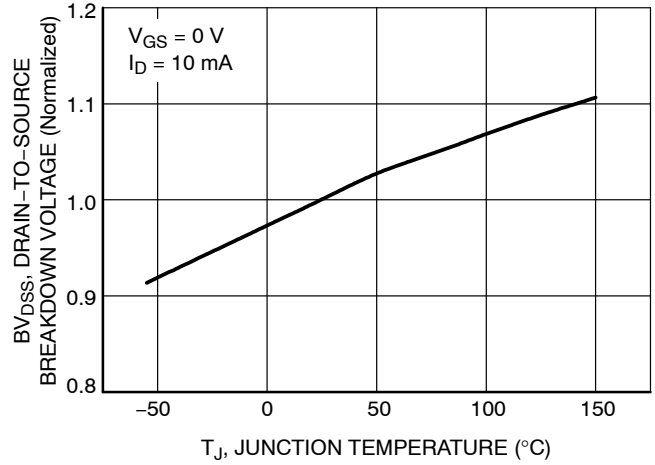


Figure 8. Breakdown Voltage Variation vs. Temperature

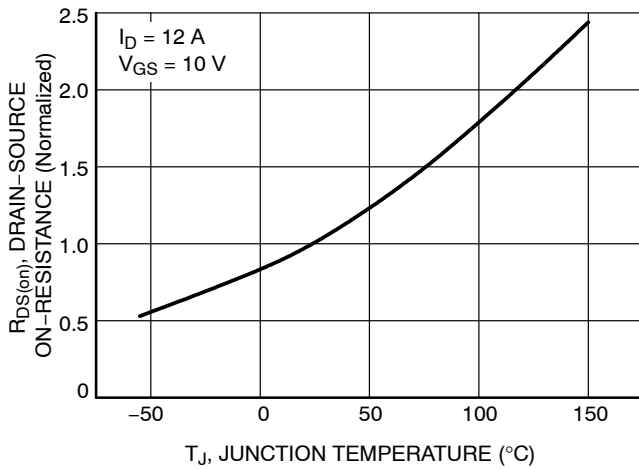


Figure 9. On-Resistance Variation vs. Temperature

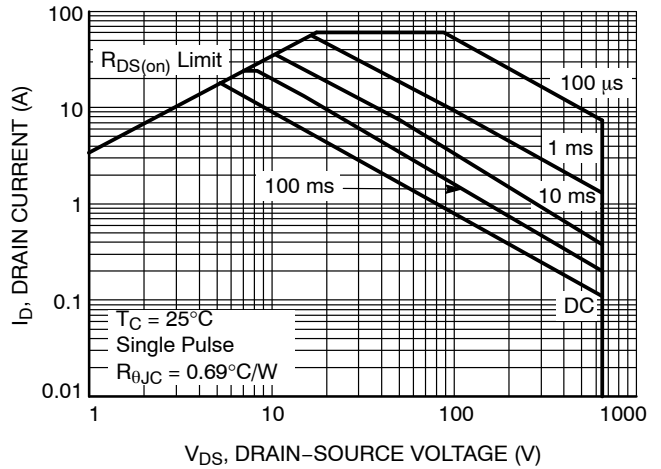


Figure 10. Maximum Safe Operating Area

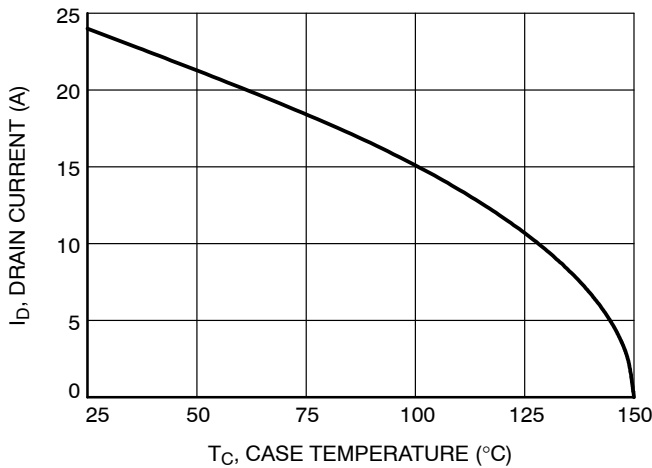


Figure 11. Maximum Drain Current vs. Case Temperature

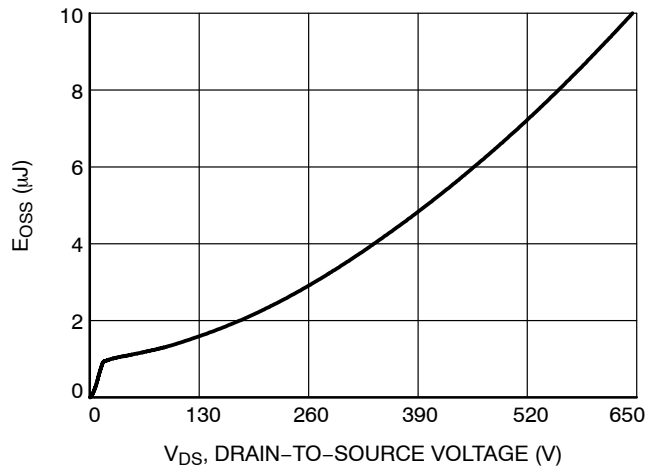


Figure 12. E_{oss} vs. Drain-to-Source Voltage

TYPICAL CHARACTERISTICS

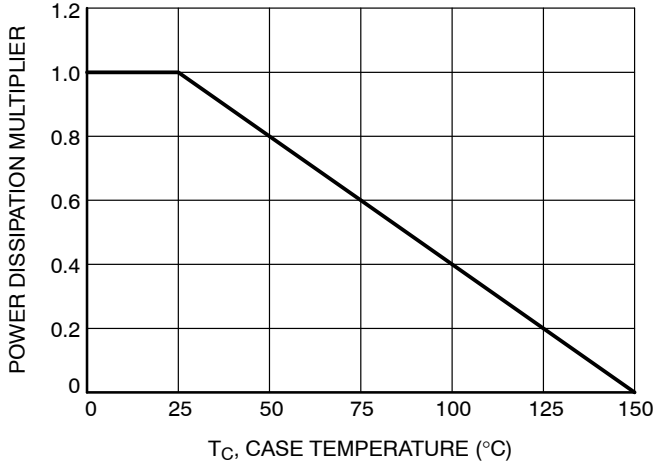


Figure 13. Normalized Power Dissipation vs. Case Temperature

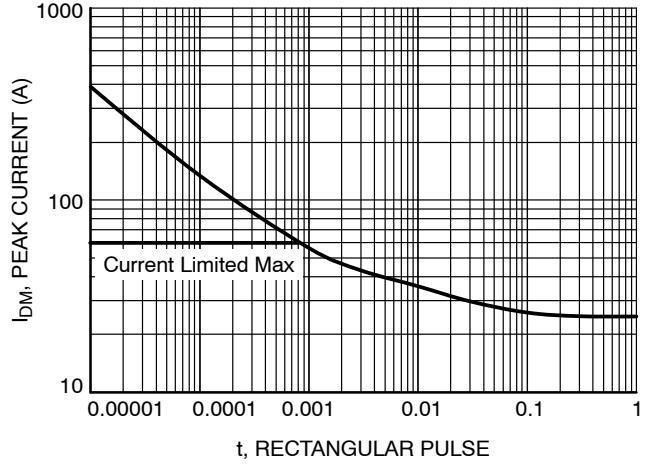


Figure 14. Peak Current Capability

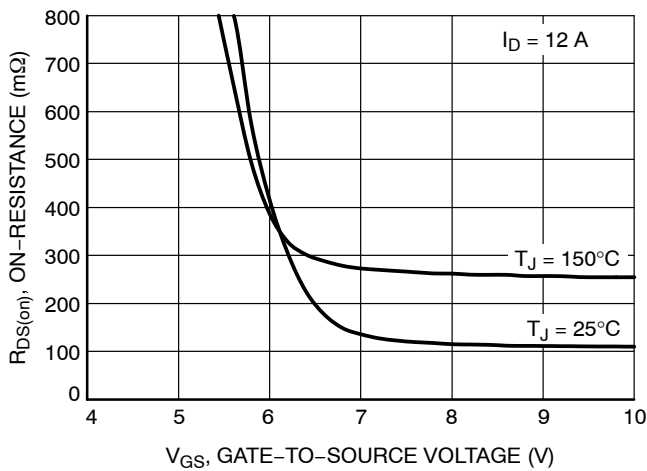


Figure 15. $R_{DS(on)}$ vs. Gate Voltage

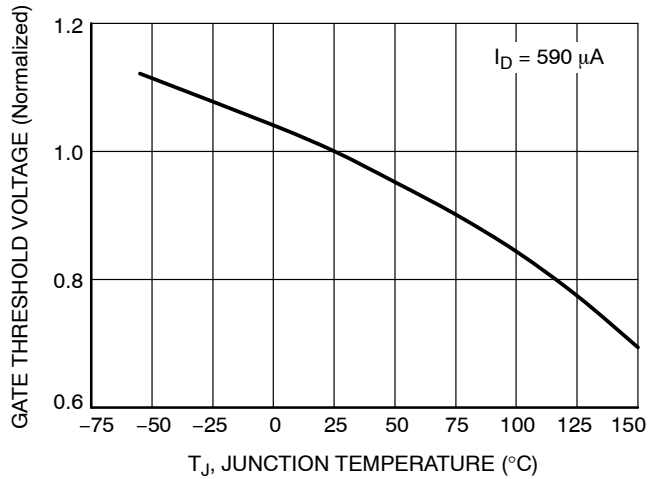


Figure 16. Normalized Gate Threshold Voltage vs. Temperature

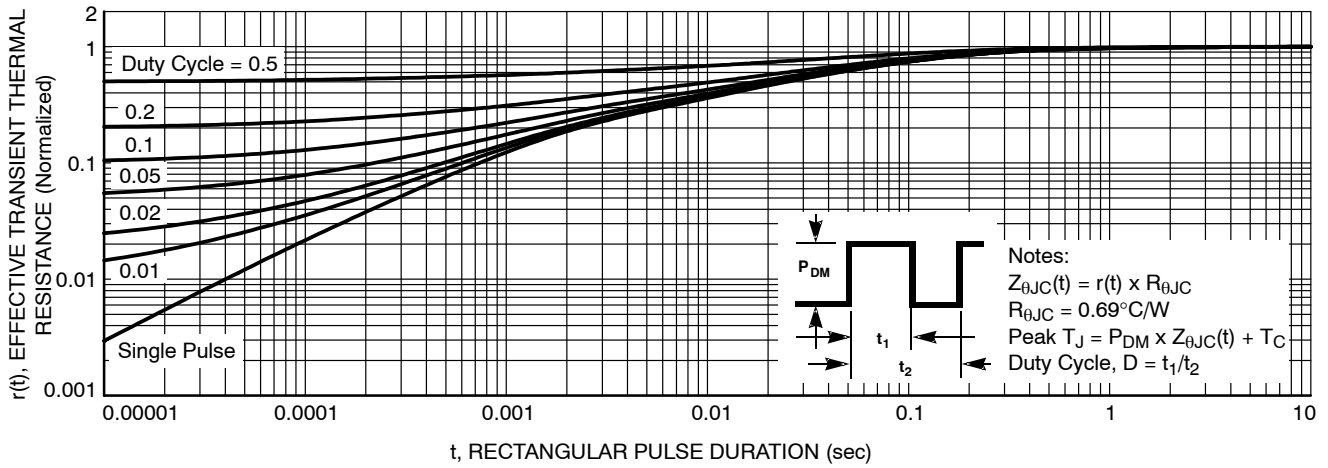


Figure 17. Transient Thermal Response



Figure 18. Gate Charge Test Circuit & Waveform



Figure 19. Resistive Switching Test Circuit & Waveforms



Figure 20. Unclamped Inductive Switching Test Circuit & Waveforms

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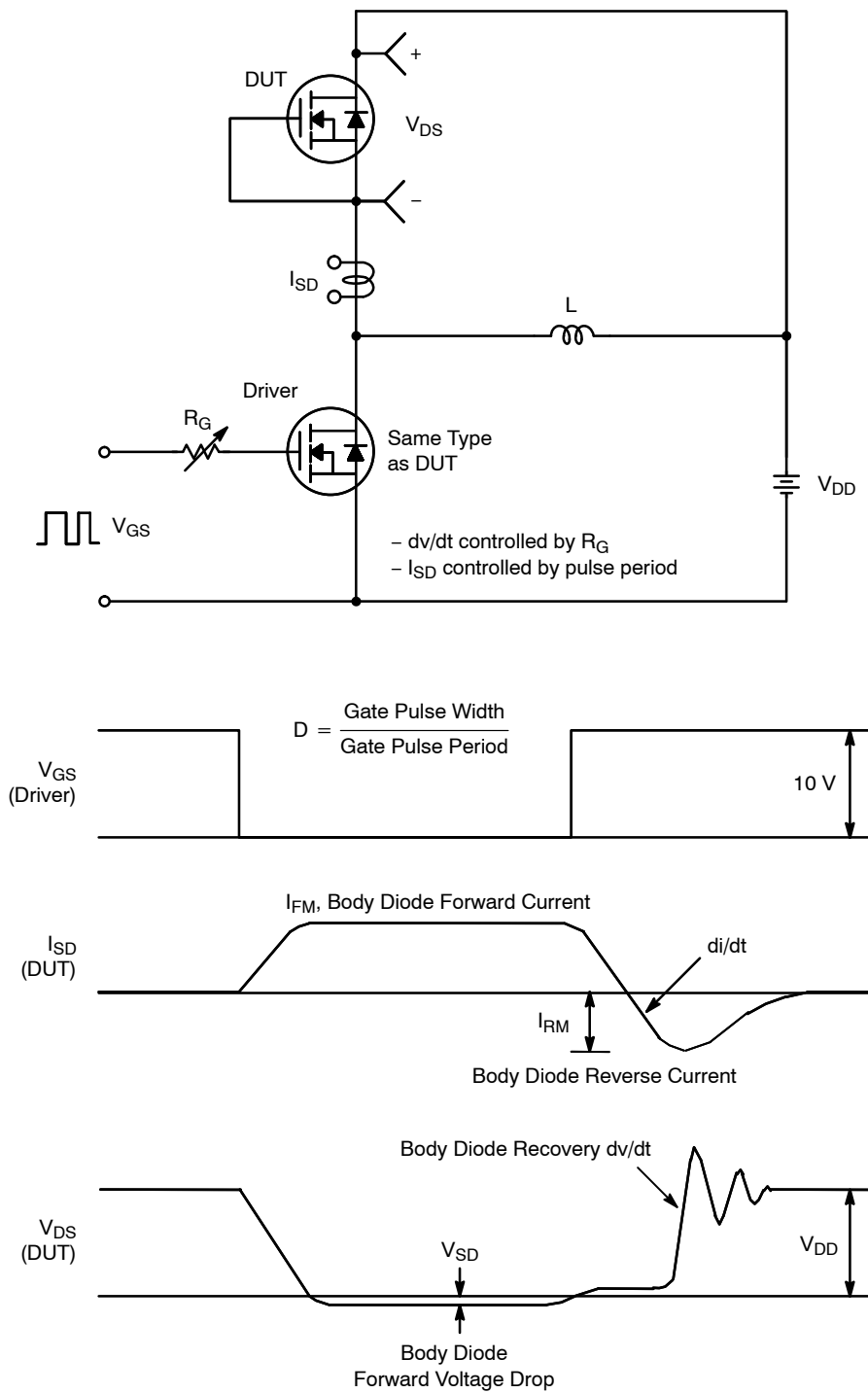
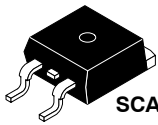


Figure 21. Peak Diode Recovery dv/dt Test Circuit & Waveforms

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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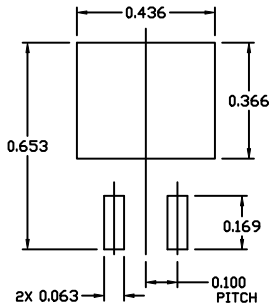
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D²PAK-3 (TO-263, 3-LEAD)

CASE 418AJ

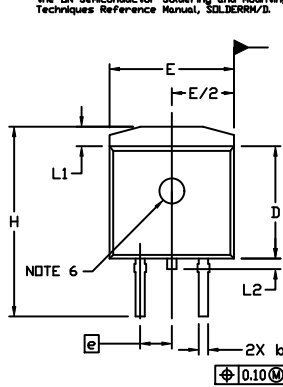
ISSUE F

DATE 11 MAR 2021



RECOMMENDED MOUNTING FOOTPRINT

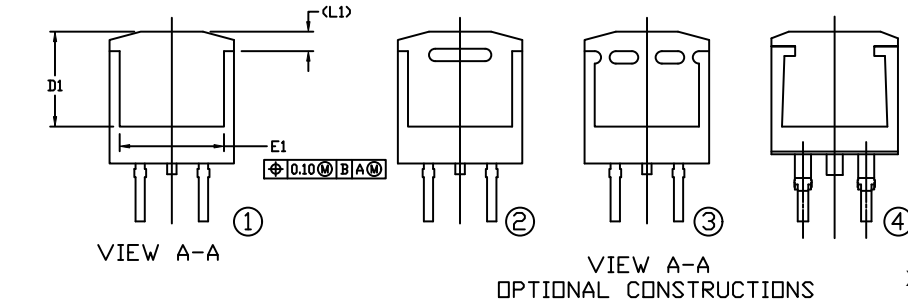
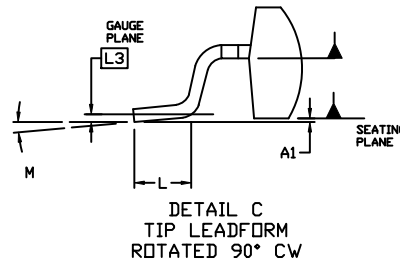
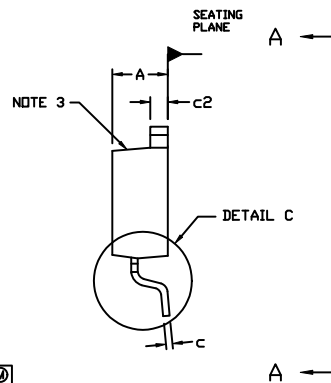
■ For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/1.



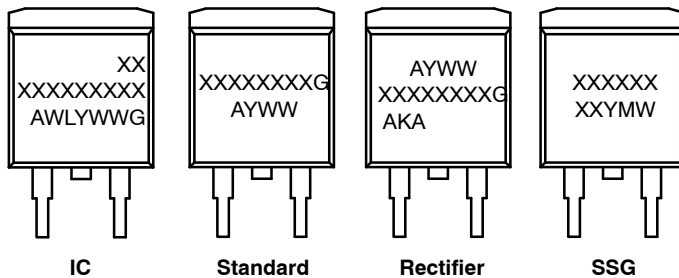
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. CHAMFER OPTIONAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
6. OPTIONAL MOLD FEATURE.
7. Ⓛ, Ⓜ ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100	BSC	2.54	BSC
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010	BSC	0.25	BSC
M	0*	8*	0*	8*



GENERIC MARKING DIAGRAMS*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- W = Week Code (SSG)
- M = Month Code (SSG)
- G = Pb-Free Package
- AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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