MOSFET - Power, N-Channel, Shielded Gate

80 V, 8.3 mΩ, 61 A

NTTFS8D1N08H

General Description

This N−Channel MOSFET is produced using **onsemi**'s advanced MOSFET process that incorporates Shielded Gate technology. This process has been optimized to minimize on−state resistance and yet maintain superior switching performance with best in class soft body diode.

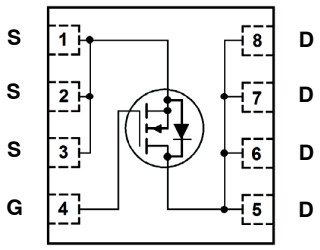
Features

- Shielded Gate MOSFET Technology
- Max $R_{DS(on)}$ = 8.3 mΩ at V_{GS} = 10 V, I_D = 16 A
- Max $R_{DS(on)}$ = 12.6 mΩ at V_{GS} = 6 V, I_D = 13 A
- Lowers Switching Noise/EMI
- MSL1 Robust Package Design
- 100% UIL Tested
- RoHS Compliant

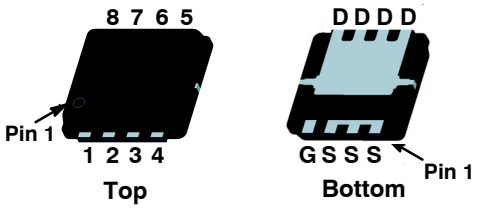
Applications

- Primary DC−DC MOSFET
- Synchronous Rectifier in DC−DC and AC−DC
- Motor Drive

ELECTRICAL CONNECTION



N-Channel MOSFET



WDFN8
(3.3x3.3, 0.65 P)
CASE 511DY

MARKING DIAGRAM

1N08	= Device Code
A	= Assembly Location
Y	= Year Code
WW	= Work Week Code

ORDERING INFORMATION

Device	Package	Shipping†
NTTFS8D1N08H	WDFN8 (Pb−Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter				Ratings	Unit
V_{DS}	Drain to Source Voltage				80	V
V_{GS}	Gate to Source Voltage				±20	V
I_D	Drain Current	–Continuous	T_C = 25°C	(Note 5)	61	A
		–Continuous	T_C = 100°C	(Note 5)	39	
		–Continuous	T_A = 25°C	(Note 1a)	14	
		–Pulsed		(Note 4)	216	
E_{AS}	Single Pulse Avalanche Energy			(Note 3)	113	mJ
P_D	Power Dissipation		T_C = 25°C		63	W
	Power Dissipation		T_A = 25°C	(Note 1a)	3.2	
T_J, T_{STG}	Operating and Storage Junction Temperature Range				–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter		Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case		2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	39	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	80	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	52	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 64 V, V_{GS} = 0 V	–	–	10	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = +20 V, V_{DS} = 0 V	–	–	100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 80 μA	2.0	2.8	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 80 μA, referenced to 25°C	–	–7.2	–	mV/°C
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 16 A	–	6.4	8.3	mΩ
		V_{GS} = 6 V, I_D = 13 A	–	9	12.6	
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	–	1450	–	pF
C_{OSS}	Output Capacitance		–	776	–	
C_{RSS}	Reverse Transfer Capacitance		–	46	–	
R_G	Gate Resistance		–	0.6	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(ON)}$	Turn – On Delay Time	V_{DD} = 40 V, I_D = 16 A, V_{GS} = 10 V, R_{GEN} = 2.5 Ω	–	9.1	–	ns
$t_{rd(ON)}$	Rise Time		–	13	–	
$t_{d(OFF)}$	Turn – Off Delay Time		–	23.8	–	
t_f	Fall Time		–	2.5	–	

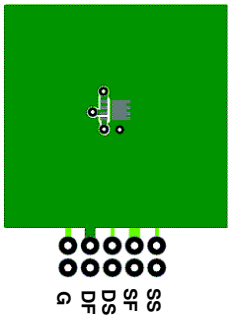
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
SWITCHING CHARACTERISTICS							
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V	V_{DD} = 40 V I_D = 16 A	–	23	–	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 6 V		–	9	–	
Q_{gs}	Gate to Source Charge			–	7.2	–	
Q_{gd}	Gate to Drain “Miller” Charge			–	4.2	–	
DRAIN−SOURCE DIODE CHARACTERISTICS							
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 16 A (Note 2)		–	0.81	1.2	V
		V_{GS} = 0 V, I_S = 16 A (Note 2)		–	0.64	1.3	
t_{rr}	Reverse Recovery Time	I_F = 16 A, di/dt = 100 A/μs		–	40.5	–	ns
Q_{rr}	Reverse Recovery Charge			–	46.8	–	nC

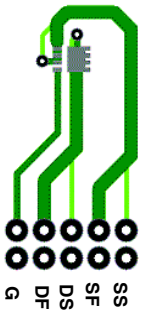
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{\theta CA}$ is determined by the user’s board design.



a) 53°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b) 125°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. E_{AS} of TBD mJ is based on starting T_J = 25°C; L = 1 mH, I_{AS} = 15 A, V_{DD} = 64 V, V_{GS} = 10 V. 100% test at L = 1 mH, I_{AS} = 15 A.
4. Pulsed I_D please refer to SOA graph for more details.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro−mechanical application board design.

TYPICAL CHARACTERISTICS

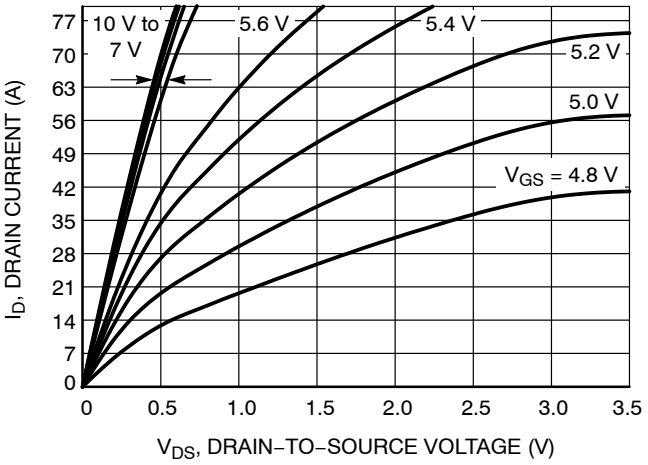


Figure 1. On−Region Characteristics

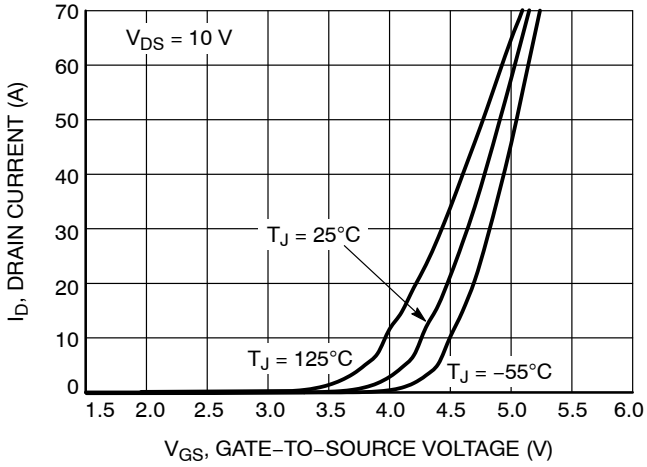


Figure 2. Transfer Characteristics

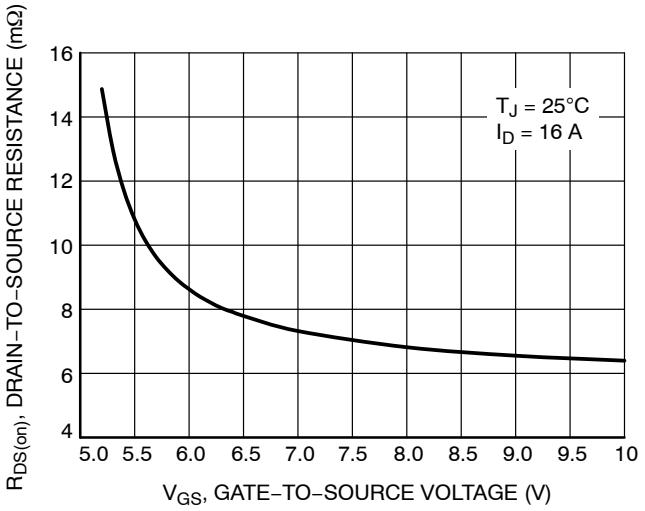


Figure 3. On−Resistance vs. Gate−to−Source Voltage

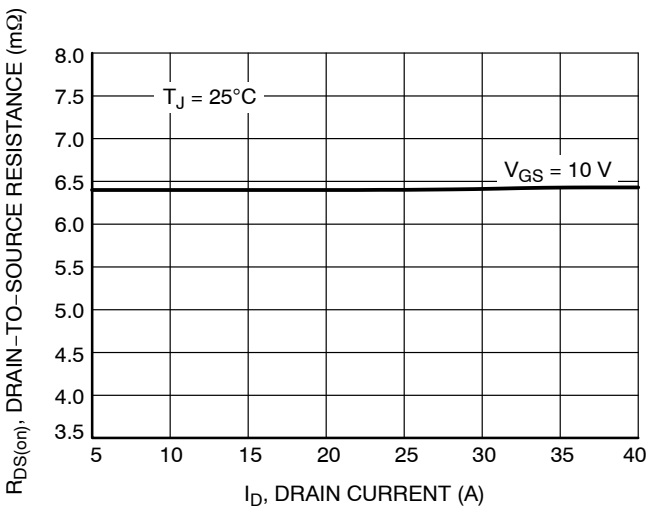


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

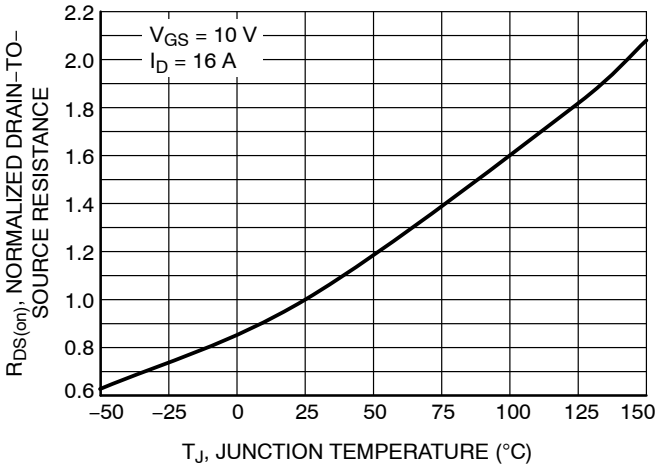


Figure 5. On−Resistance Variation with Temperature

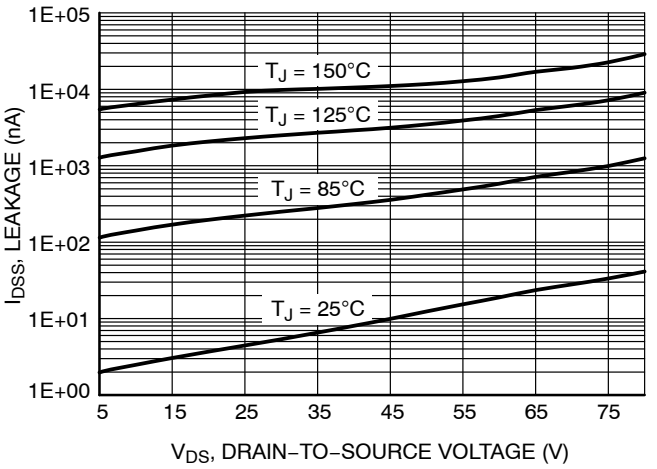


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

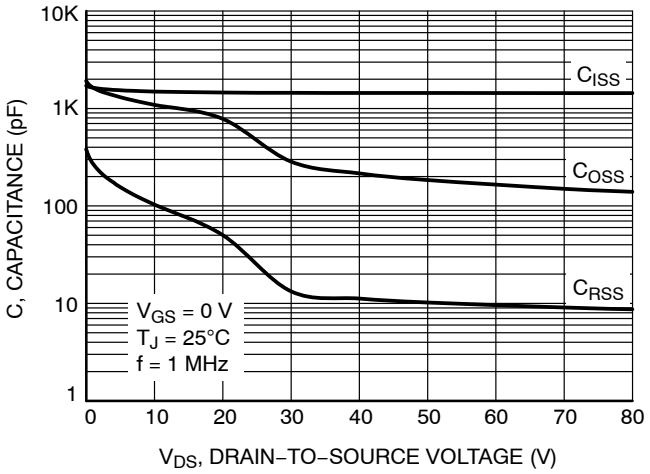


Figure 7. Capacitance Variation

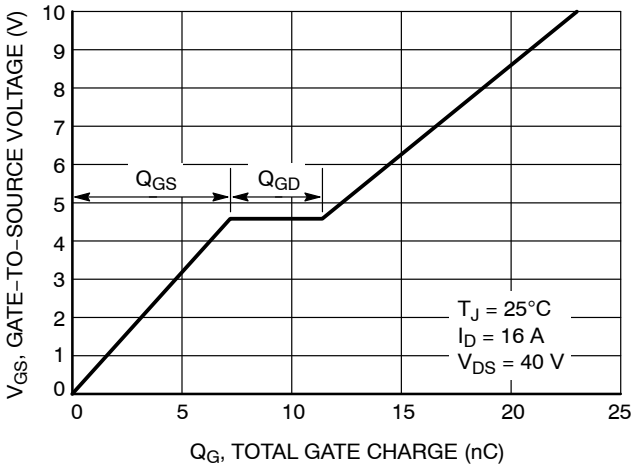


Figure 8. Gate−to−Source Voltage vs. Total Charge

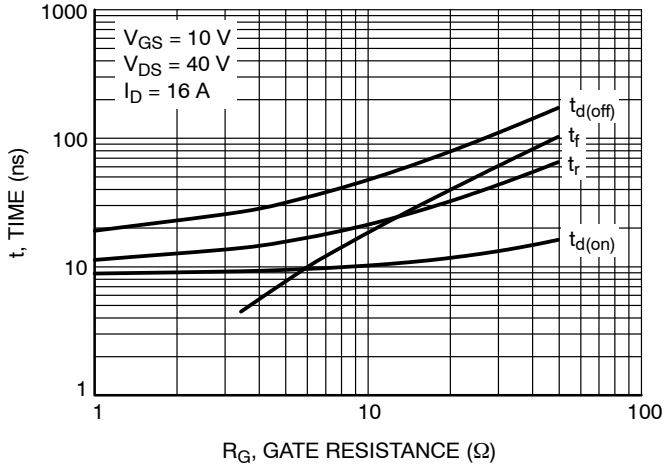


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

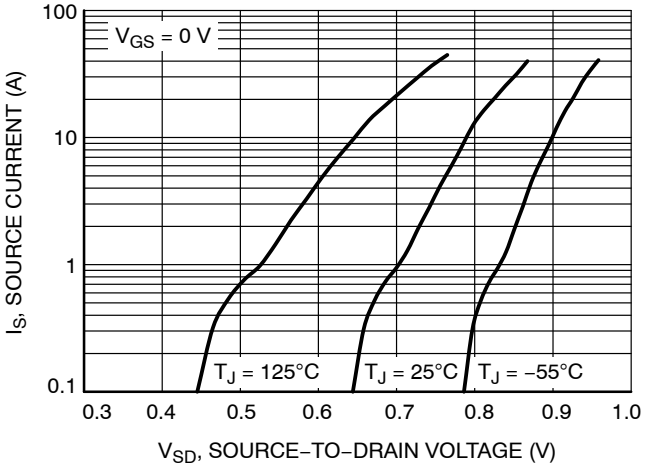


Figure 10. Diode Forward Voltage vs. Current

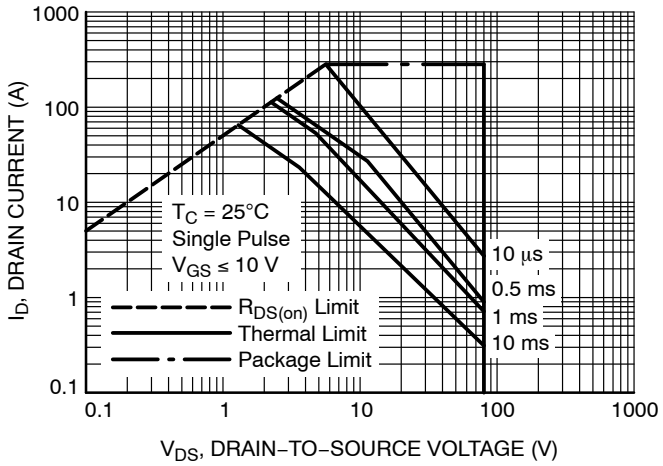


Figure 11. Maximum Rated Forward Biased Safe Operating Area

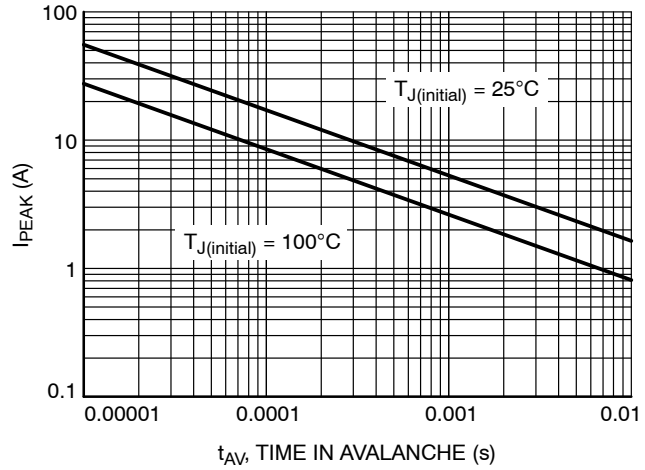


Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS

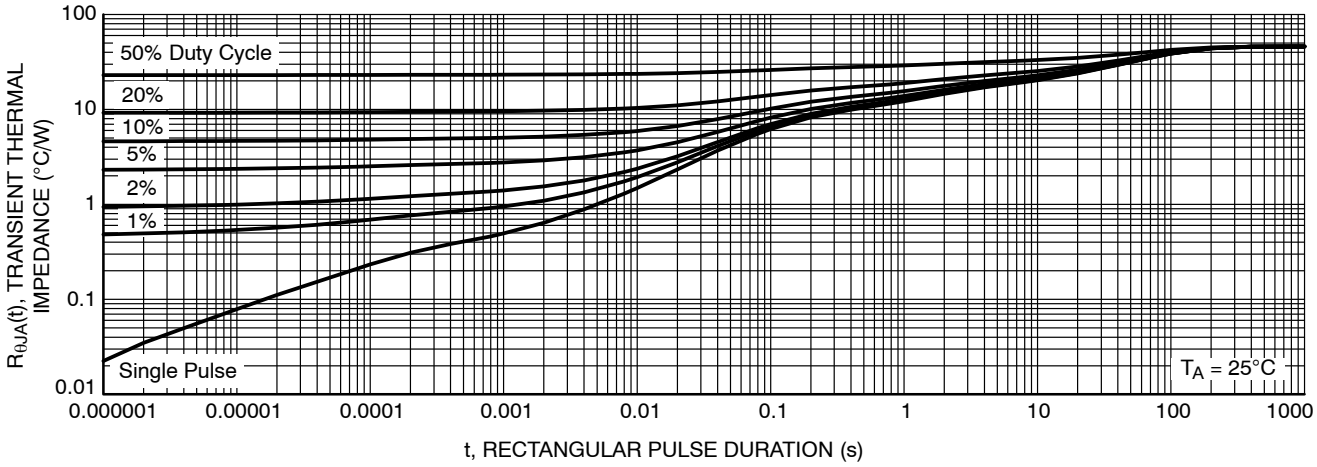


Figure 13. Thermal Response

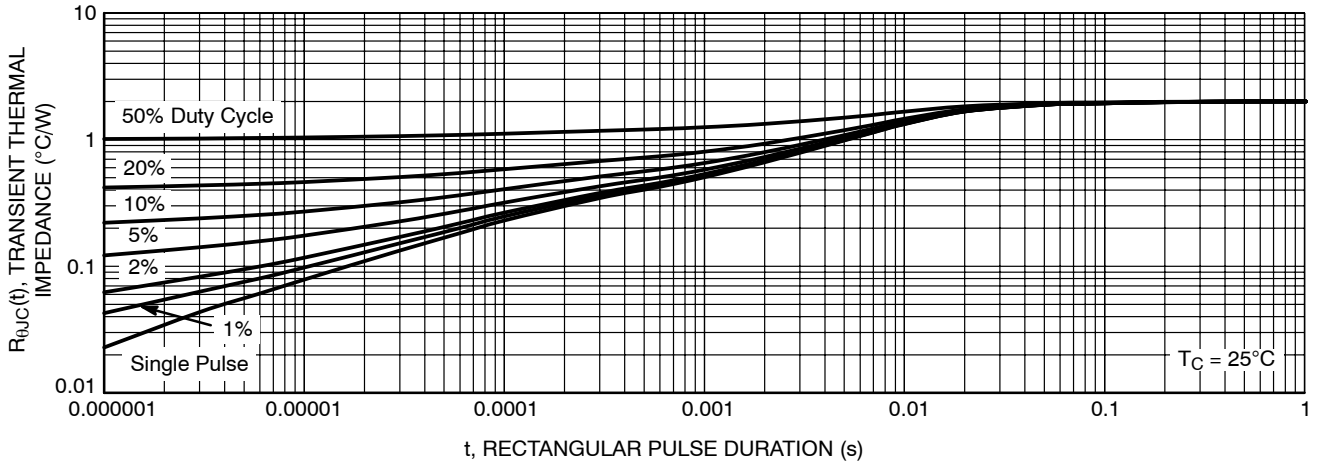
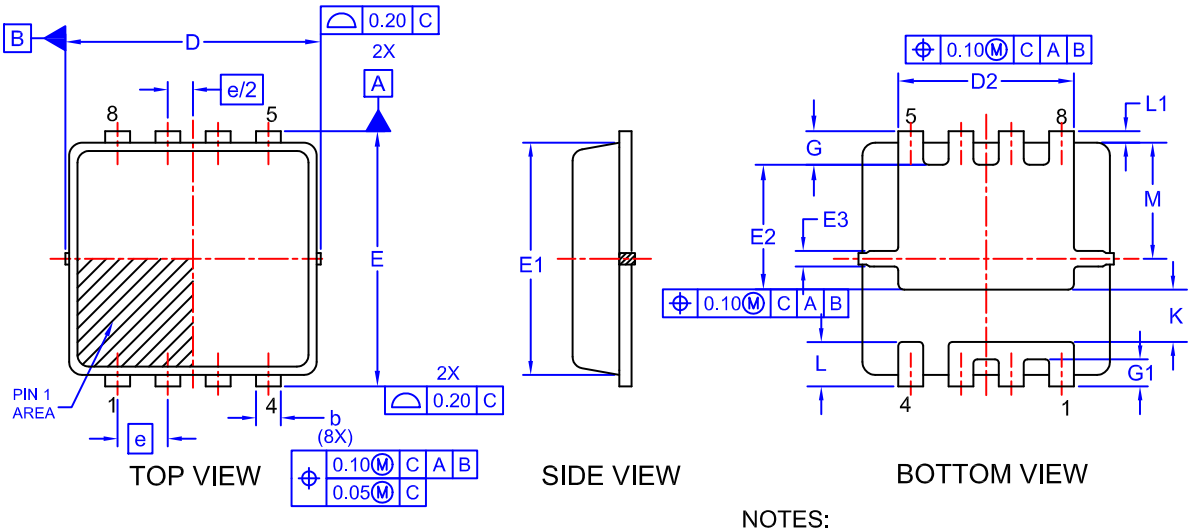


Figure 14. Thermal Response

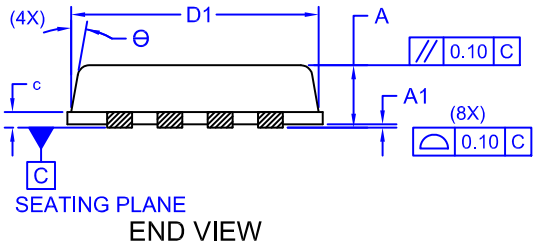
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

WDFN8 3.3x3.3, 0.65P
CASE 511DY
ISSUE A

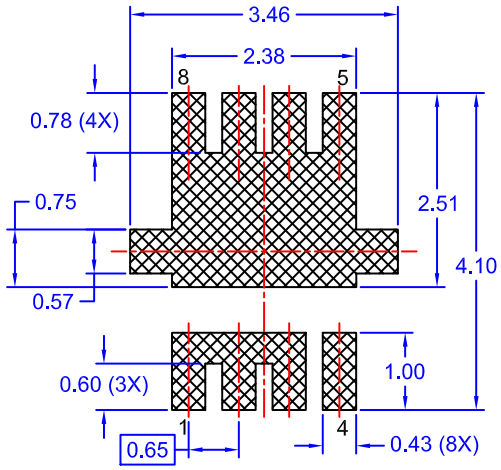
DATE 21 AUG 2018



NOTES:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS D1 & E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS.



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
b	0.23	0.33	0.43
c	0.15	0.20	0.25
D	3.20	3.30	3.40
D1	2.95	3.13	3.30
D2	1.98	2.20	2.40
E	3.20	3.30	3.40
E1	2.80	3.00	3.15
E2	1.40	1.60	1.80
E3	0.15	0.25	0.40
e	0.65 BSC		
G	0.30	0.43	0.55
G1	0.25	0.35	0.45
K	0.55	0.75	0.95
L	0.35	0.52	0.65
L1	0.06	0.15	0.30
M	1.35	1.50	1.60
Θ	0	-	12



RECOMMENDED LAND PATTERN

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
Y = Year Code
WW = Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON90827G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**WDFN8 3.3x3.3, 0.65P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales