

MOSFET – Power, Single N-Channel, Logic Level, DUAL COOL[®] DFN8 5x6 40 V, 0.7 mΩ, 349 A

Product Preview NTMFSC0D7N04XL

Features

- Low $R_{DS(on)}$ to Minimize Conduction Loss
- Low Q_{RR} with Soft Recovery to Minimize E_{RR} Loss and Voltage Spike
- Low Q_G and Capacitance to Minimize Driving and Switching Loss
- Advanced Dual-Sided Cooled Packaging
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- High Switching Frequency DC-DC Conversion
- Synchronous Rectification

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

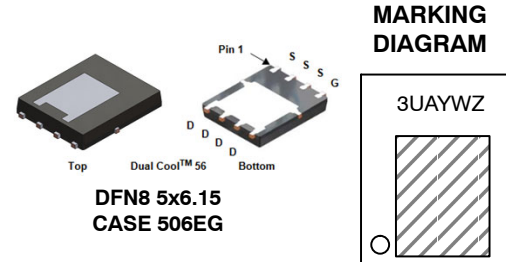
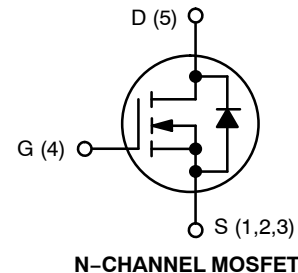
Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V _{DSS}	40	V
Gate-to-Source Voltage	DC	V _{GS}	±20	V
Continuous Drain Current (Note 2)	T _C = 25°C	I _D	349	A
	T _C = 100°C		247	
Power Dissipation (Note 2)	T _C = 25°C	P _D	167	W
	T _C = 100°C		83	
Pulsed Drain Current	T _C = 25°C, t _p = 100 μs	I _{DM}	1667	A
Pulsed Source Current (Body Diode)		I _{SM}	1667	
Operating Junction and Storage Temperature Range		T _J , T _{STG}	−55 to +175	°C
Source Current (Body Diode)		I _S	256	A
Single Pulse Avalanche Energy (I _{PK} = 97 A) (Note 3)		E _{AS}	470	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 in² pad size, 1 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
3. E_{AS} of 470 mJ is based on started $T_J = 25^\circ\text{C}$, $I_{AS} = 97 \text{ A}$, $V_{DD} = 32 \text{ V}$, $V_{GS} = 10 \text{ V}$, 100% avalanche tested.

This document contains information on a product under development. onsemi reserves the right to change or discontinue this product without notice.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
40 V	0.7 mΩ @ 10 V	349 A
	1.1 mΩ @ 4.5 V	



- 3U = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
Z = Assembly Lot Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 6 of this data sheet.

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THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case, Bottom	$R_{\theta JC}$	0.9	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Case, Top	$R_{\theta JT}$	1.4	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	38	$^{\circ}\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 1\text{ mA}$, Referenced to 25°C		16.6		$\text{mV}/^{\circ}\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40\text{ V}, T_J = 25^{\circ}\text{C}$			10	μA
		$V_{DS} = 40\text{ V}, T_J = 125^{\circ}\text{C}$			100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA

ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 49\text{ A}$		0.58	0.7	$\text{m}\Omega$
		$V_{GS} = 6\text{ V}, I_D = 49\text{ A}$		0.66	0.9	
		$V_{GS} = 4.5\text{ V}, I_D = 39\text{ A}$		0.77	1.1	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1.3		2.2	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)} / \Delta T_J$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$		-5.35		$\text{mV}/^{\circ}\text{C}$
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 49\text{ A}$		245		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}, f = 1\text{ MHz}$		7090		pF
Output Capacitance	C_{OSS}			1860		
Reverse Transfer Capacitance	C_{RSS}			40		
Output Charge	Q_{OSS}	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$		72		nC
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DD} = 20\text{ V}; I_D = 49\text{ A}$		42		
		$V_{GS} = 6\text{ V}, V_{DD} = 20\text{ V}; I_D = 49\text{ A}$		57		
		$V_{GS} = 10\text{ V}, V_{DD} = 20\text{ V}; I_D = 49\text{ A}$		96		
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 10\text{ V}, V_{DD} = 20\text{ V}; I_D = 49\text{ A}$		11		
Gate-to-Source Charge	Q_{GS}			20		
Gate-to-Drain Charge	Q_{GD}			6		
Gate Plateau Voltage	V_{GP}			2.89		V
Gate Resistance	R_G	$f = 1\text{ MHz}$		0.5		Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	Resistive Load, $V_{GS} = 0/10\text{ V}, V_{DD} = 20\text{ V},$ $I_D = 49\text{ A}, R_G = 2.5\text{ }\Omega$		25		ns
Rise Time	t_r			7		
Turn-Off Delay Time	$t_{d(OFF)}$			64		
Fall Time	t_f			5		

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SOURCE-TO-DRAIN DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 49\text{ A}, T_J = 25^\circ\text{C}$		0.8	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 49\text{ A}, T_J = 125^\circ\text{C}$		0.65		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dl/dt = 300\text{ A}/\mu\text{s},$ $I_S = 49\text{ A}, V_{DD} = 20\text{ V}$		39		ns
Charge Time	t_a			21		
Discharge Time	t_b			18		
Reverse Recovery Charge	Q_{RR}			87		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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TYPICAL CHARACTERISTICS

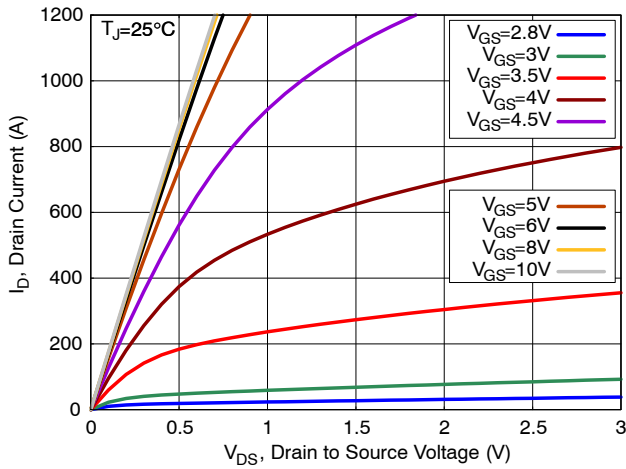


Figure 1. On-Region Characteristics

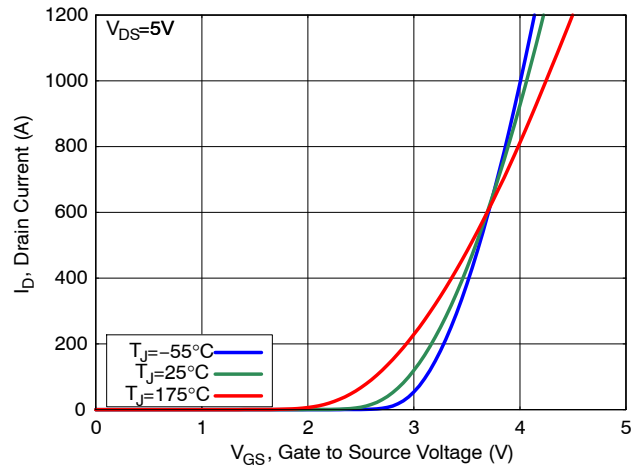


Figure 2. Transfer Characteristics

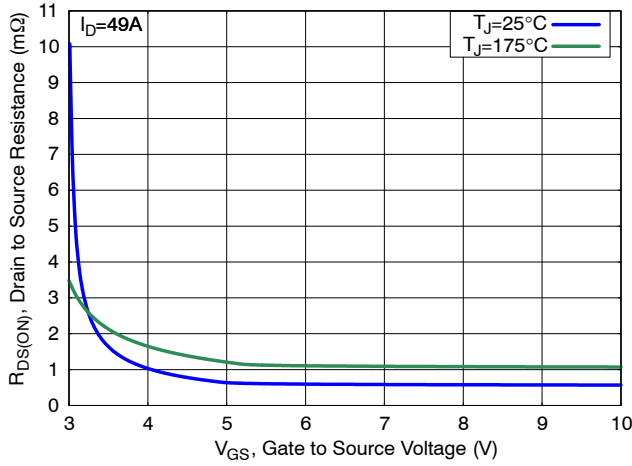


Figure 3. On-Resistance vs. Gate Voltage

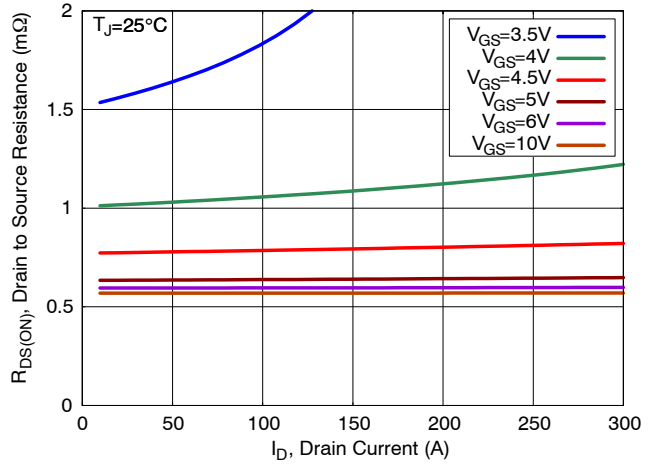


Figure 4. On-Resistance vs. Drain Current

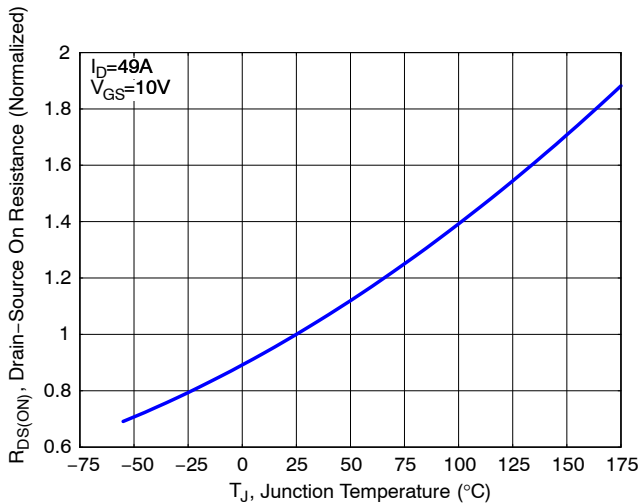


Figure 5. Normalized ON Resistance vs. Junction Temperature

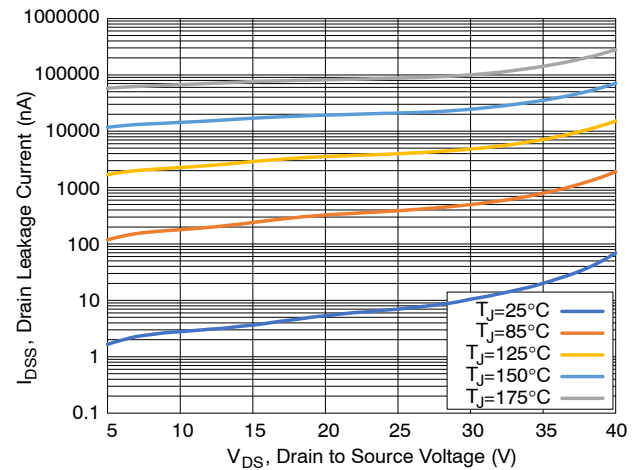


Figure 6. Drain Leakage Current vs. Drain Voltage

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TYPICAL CHARACTERISTICS (continued)

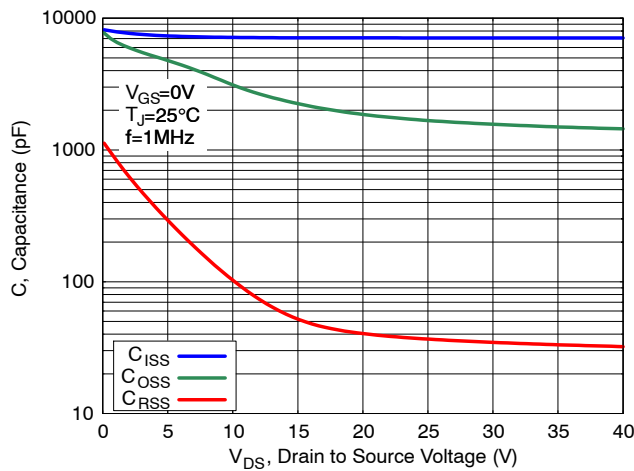


Figure 7. Capacitance Characteristics

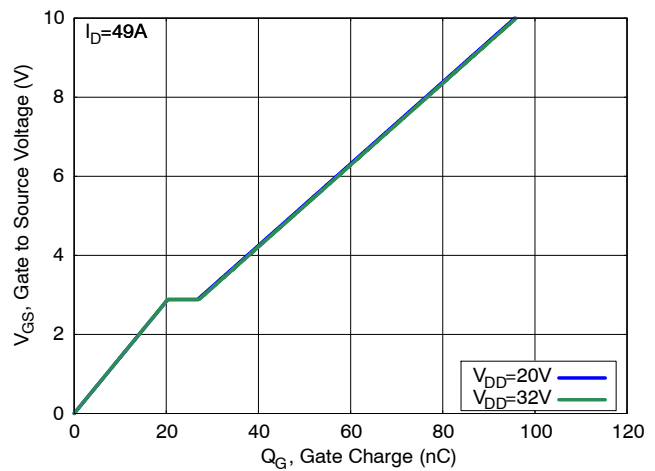


Figure 8. Gate Charge Characteristics

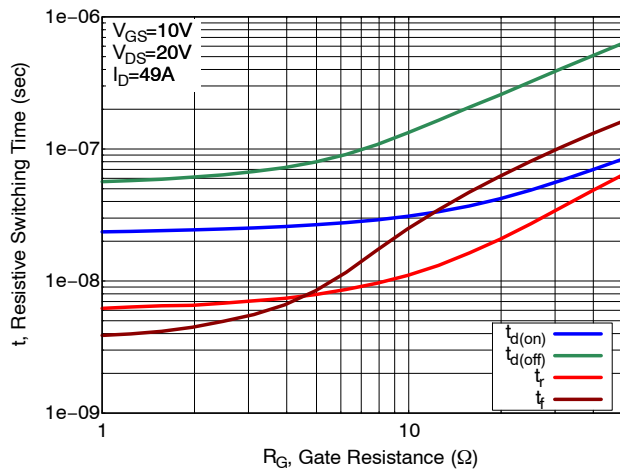


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

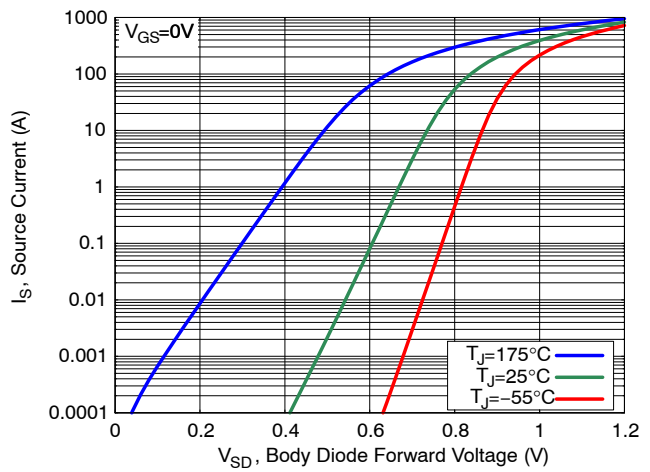


Figure 10. Diode Forward Characteristics

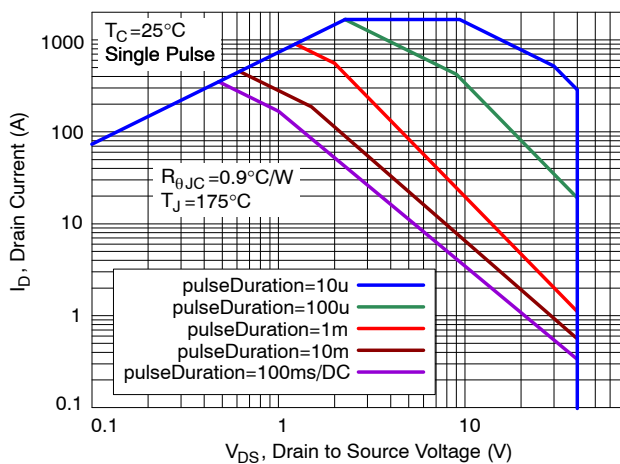


Figure 11. Safe Operating Area (SOA)

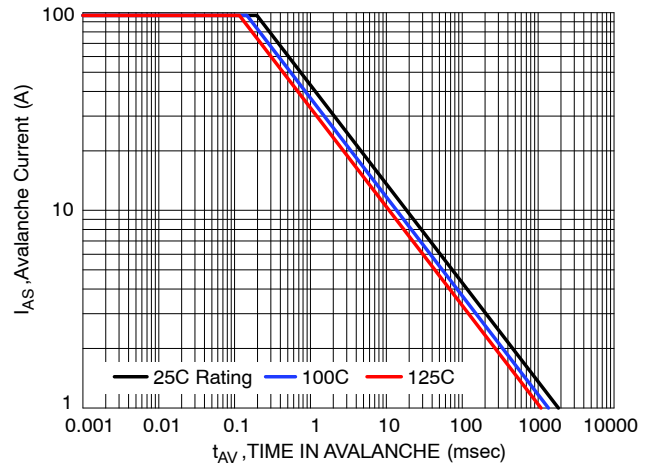


Figure 12. Avalanche Current vs. Pulse Time (UIS)

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TYPICAL CHARACTERISTICS (continued)

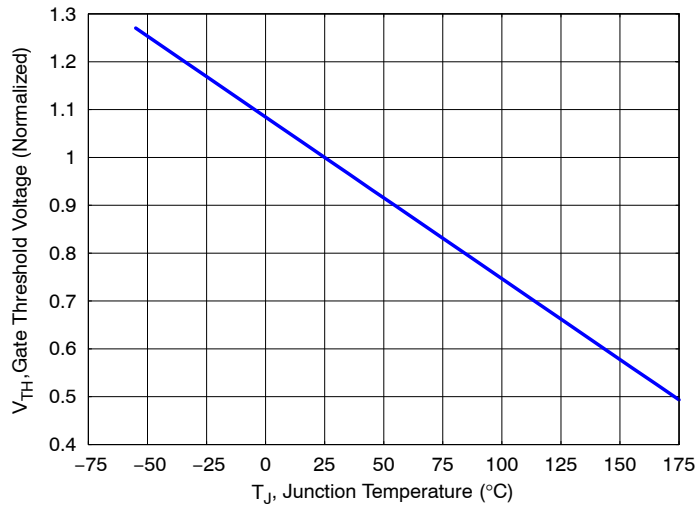


Figure 13. Gate Threshold Voltage vs. Junction Temperature

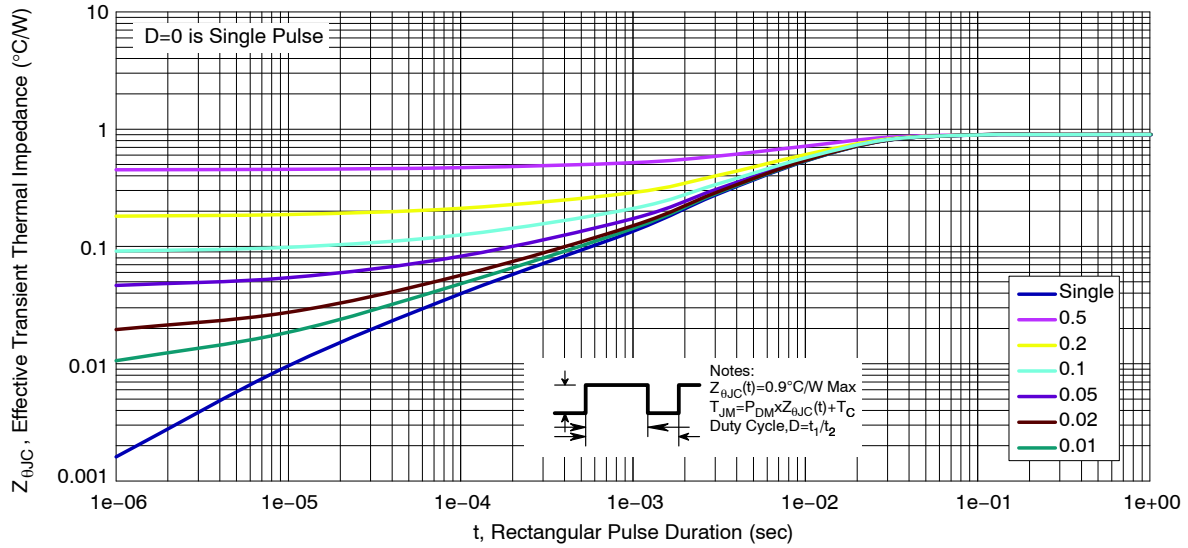


Figure 14. Thermal Characteristics

DEVICE ORDERING INFORMATION

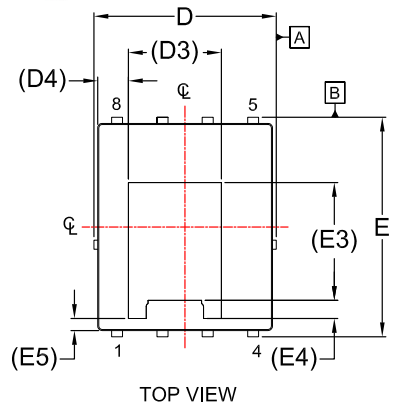
Device	Marking	Package	Shipping†
NTMFSC0D7N04XLTWG	3U	DFN8 5x6 (Pb-Free/Halogen Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

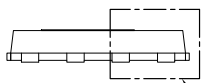
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CASE 506EG
ISSUE D

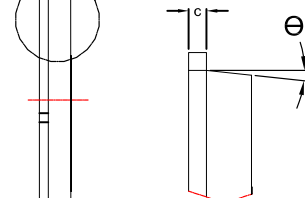
DATE 25 AUG 2020



TOP VIEW



FRONT VIEW

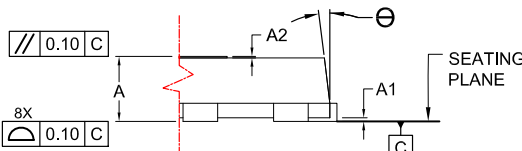
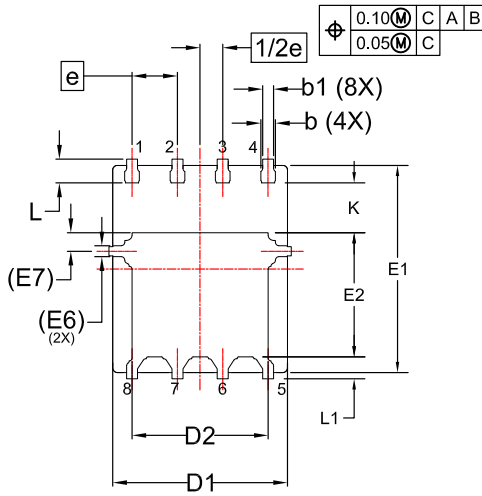
SEE
DETAIL "A"


SIDE VIEW

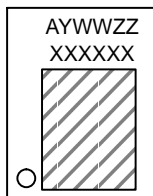
DETAIL "A"
SCALE: 2:1

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.


DETAIL "B"
SCALE: 2:1


BOTTOM VIEW

**GENERIC
MARKING DIAGRAM***


XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.85	0.90	0.95
A1	-	-	0.05
A2	-	-	0.05
b	0.31	0.41	0.51
b1	0.21	0.31	0.41
c	0.20	0.25	0.30
D	4.90	5.00	5.10
D1	4.80	4.90	5.00
D2	3.67	3.82	3.97
D3	2.60 REF		
D4	0.86 REF		
E	6.05	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.58
E3	3.30 REF		
E4	0.50 REF		
E5	0.34 REF		
E6	0.30 REF		
E7	0.52 REF		
e	1.27 BSC		
1/2e	0.635 BSC		
K	1.30	1.40	1.50
L	0.56	0.66	0.76
L1	0.52	0.62	0.72
Θ	0°	---	12°

LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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DESCRIPTION: DFN8 5x6.15, 1.27P, DUAL COOL

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