

# Silicon Carbide (SiC) MOSFET – EliteSiC, 33 mohm, 650 V, M2, TOLL

## NTBL045N065SC1

### Features

- Typ.  $R_{DS(on)} = 33\text{ m}\Omega @ V_{GS} = 18\text{ V}$   
Typ.  $R_{DS(on)} = 45\text{ m}\Omega @ V_{GS} = 15\text{ V}$
- Ultra Low Gate Charge ( $Q_{G(tot)} = 105\text{ nC}$ )
- Low Effective Output Capacitance ( $C_{oss} = 162\text{ pF}$ )
- 100% Avalanche Tested
- $T_J = 175^\circ\text{C}$
- RoHS Compliant

### Typical Applications

- SMPS (Switching Mode Power Supplies)
- Solar Inverters
- UPS (Uninterruptable Power Supplies)
- Energy Storage

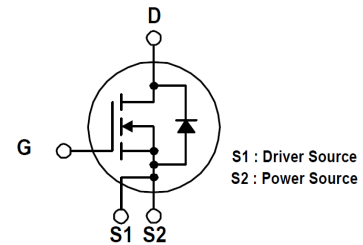
### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		$V_{DSS}$	650	V
Gate-to-Source Voltage		$V_{GS}$	-8/+22.6	V
Recommended Operation Values of Gate – Source Voltage		$T_C < 175^\circ\text{C}$ $V_{GSop}$	-5/+18	V
Continuous Drain Current (Note 2)	Steady State $T_C = 25^\circ\text{C}$	$I_D$	73	A
Power Dissipation (Note 2)		$P_D$	348	W
Continuous Drain Current (Notes 1, 2)	Steady State $T_C = 100^\circ\text{C}$	$I_D$	51	A
Power Dissipation (Notes 1, 2)		$P_D$	174	W
Pulsed Drain Current (Note 3)		$T_C = 25^\circ\text{C}$ $I_{DM}$	182	A
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)		$I_S$	75	A
Single Pulse Drain-to-Source Avalanche Energy ( $I_L = 12\text{ A}_{pk}$ , $L = 1\text{ mH}$ ) (Note 4)		$E_{AS}$	72	mJ
Maximum Lead Temperature for Soldering, 1/8" from Case for 10 Seconds		$T_L$	260	$^\circ\text{C}$

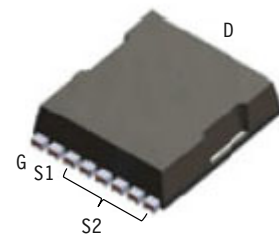
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface mounted on a FR-4 board using 1 in 2 pad of 2 oz copper.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
3. Repetitive rating, limited by max junction temperature.
4.  $E_{AS}$  of 72 mJ is based on starting  $T_J = 25^\circ\text{C}$ ;  $L = 1\text{ mH}$ ,  $I_{AS} = 12\text{ A}$ ,  $V_{DD} = 50\text{ V}$ ,  $V_{GS} = 18\text{ V}$ .

$V_{DSS}$	$R_{DS(on)}\text{ MAX}$	$I_D\text{ MAX}$
650 V	50 m $\Omega$ @ 18 V	73 A

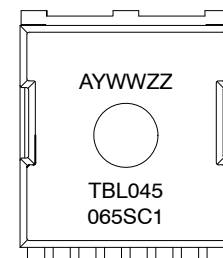


N-Channel MOSFET



H-PSOF8L  
CASE 100DC

### MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- WW = Work Week
- ZZ = Assembly Lot Code
- TBL045065SC1 = Specific Device Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

# NTBL045N065SC1

## THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Units
Junction-to-Case – Steady State (Note 2)	$R_{\theta JC}$	0.43	°C/W
Junction-to-Ambient – Steady State (Notes 1, 2)	$R_{\theta JA}$	43	°C/W

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	650			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 20\text{ mA}$ , refer to $25^\circ\text{C}$		0.15		V/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}$ $V_{DS} = 650\text{ V}$	$T_J = 25^\circ\text{C}$		10	$\mu\text{A}$
			$T_J = 175^\circ\text{C}$		1	mA
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{GS} = +18/-5\text{ V}, V_{DS} = 0\text{ V}$			250	nA

## ON CHARACTERISTICS

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 8\text{ mA}$	1.8	2.8	4.3	V
Recommended Gate Voltage	$V_{GOP}$		-5		+18	V
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 15\text{ V}, I_D = 25\text{ A}, T_J = 25^\circ\text{C}$		45		m $\Omega$
		$V_{GS} = 18\text{ V}, I_D = 25\text{ A}, T_J = 25^\circ\text{C}$		33	50	
		$V_{GS} = 18\text{ V}, I_D = 25\text{ A}, T_J = 175^\circ\text{C}$		40		
Forward Transconductance	$g_{FS}$	$V_{DS} = 10\text{ V}, I_D = 25\text{ A}$		16		S

## CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz},$ $V_{DS} = 325\text{ V}$		1870		pF
Output Capacitance	$C_{OSS}$			162		
Reverse Transfer Capacitance	$C_{RSS}$			14		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -5/18\text{ V}, V_{DS} = 520\text{ V},$ $I_D = 25\text{ A}$		105		nC
Gate-to-Source Charge	$Q_{GS}$			27		
Gate-to-Drain Charge	$Q_{GD}$			30		
Gate-Resistance	$R_G$	$f = 1\text{ MHz}$		3.1		$\Omega$

## SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -5/18\text{ V}, V_{DS} = 400\text{ V},$ $I_D = 25\text{ A}, R_G = 2.2\ \Omega,$ Inductive Load		13		ns
Rise Time	$t_r$			14		
Turn-Off Delay Time	$t_{d(OFF)}$			26		
Fall Time	$t_f$			7		
Turn-On Switching Loss	$E_{ON}$			47		$\mu\text{J}$
Turn-Off Switching Loss	$E_{OFF}$			33		
Total Switching Loss	$E_{TOT}$			80		

## SOURCE-DRAIN DIODE CHARACTERISTICS

Continuous Source-Drain Diode Forward Current	$I_{SD}$	$V_{GS} = -5\text{ V}, T_J = 25^\circ\text{C}$			75	A
Pulsed Source-Drain Diode Forward Current (Note 3)	$I_{SDM}$	$V_{GS} = -5\text{ V}, T_J = 25^\circ\text{C}$			182	A
Forward Diode Voltage	$V_{SD}$	$V_{GS} = -5\text{ V}, I_{SD} = 25\text{ A}, T_J = 25^\circ\text{C}$		4.4		V

# NTBL045N065SC1

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise stated)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### SOURCE-DRAIN DIODE CHARACTERISTICS

Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = -5/18 V, I <sub>SD</sub> = 25 A, dI <sub>S</sub> /dt = 1000 A/μs		20		ns
Reverse Recovery Charge	Q <sub>RR</sub>			108		nC
Reverse Recovery Energy	E <sub>REC</sub>			4.5		μJ
Peak Reverse Recovery Current	I <sub>RRM</sub>			11		A
Charge time	T <sub>a</sub>			11		ns
Discharge time	T <sub>b</sub>			8.5		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

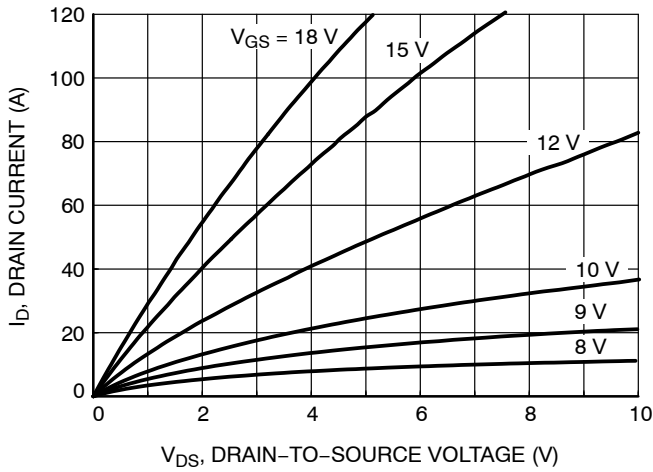


Figure 1. On-Region Characteristics

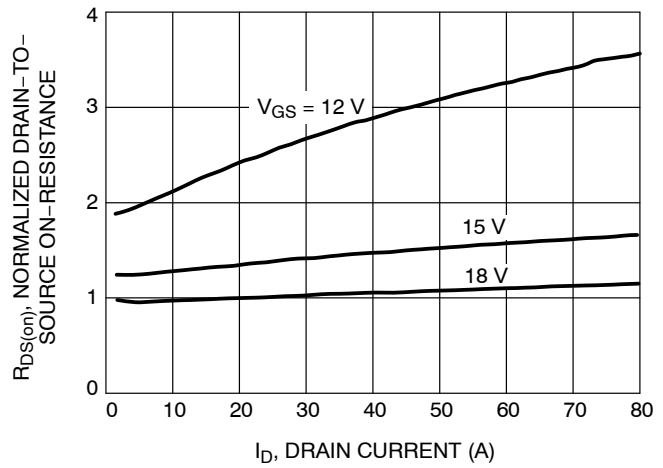


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

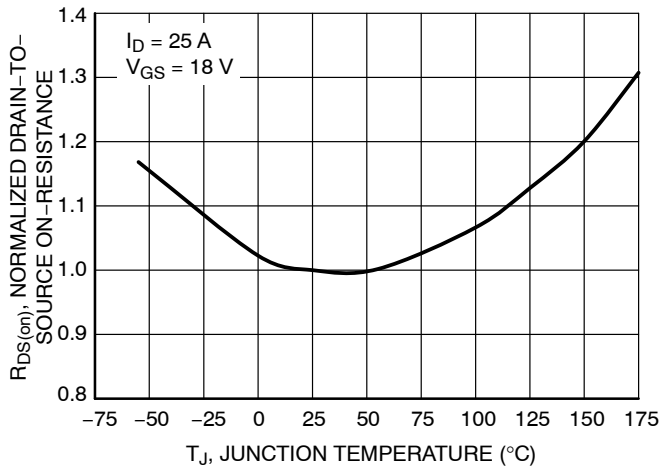


Figure 3. On-Resistance Variation with Temperature

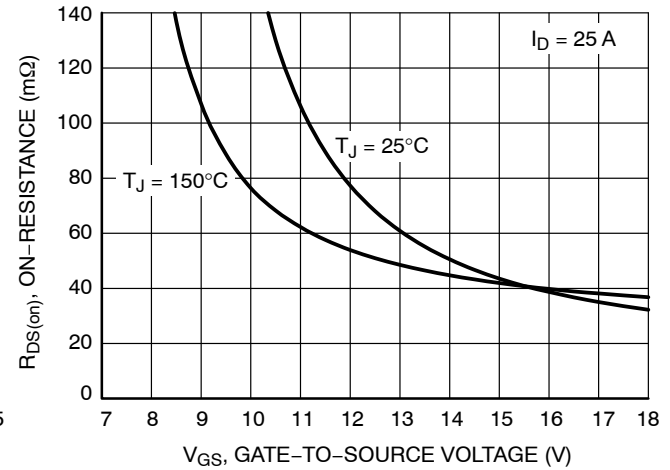


Figure 4. On-Resistance vs. Gate-to-Source Voltage

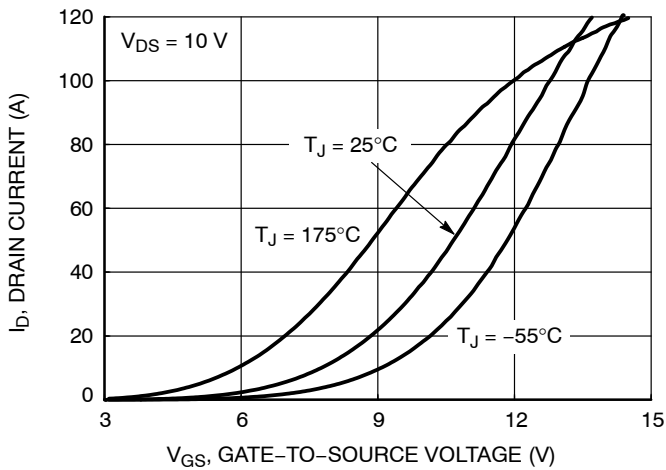


Figure 5. Transfer Characteristics

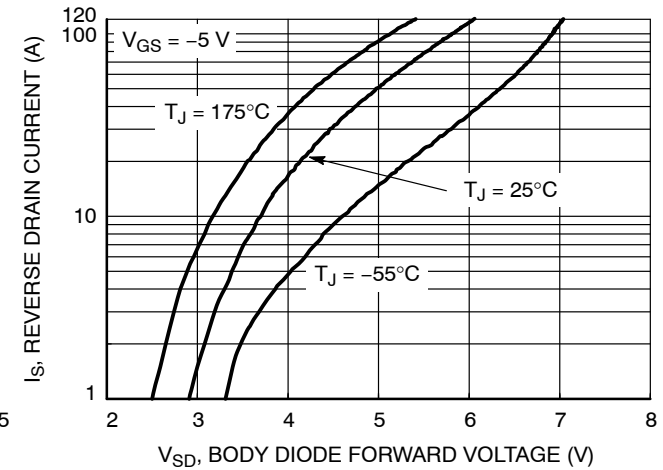


Figure 6. Diode Forward Voltage vs. Current

TYPICAL CHARACTERISTICS

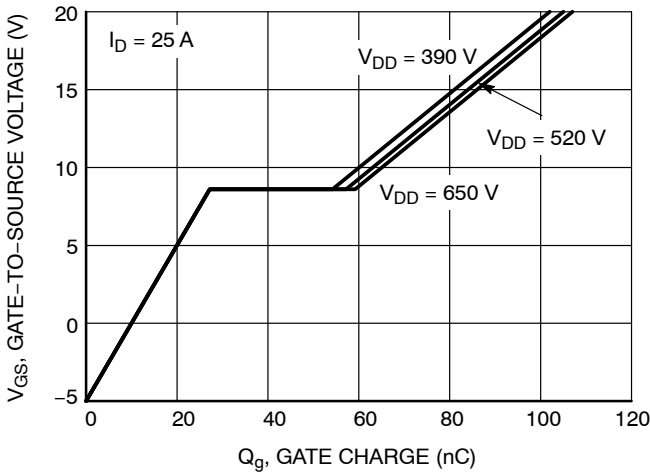


Figure 7. Gate-to-Source Voltage vs. Total Charge

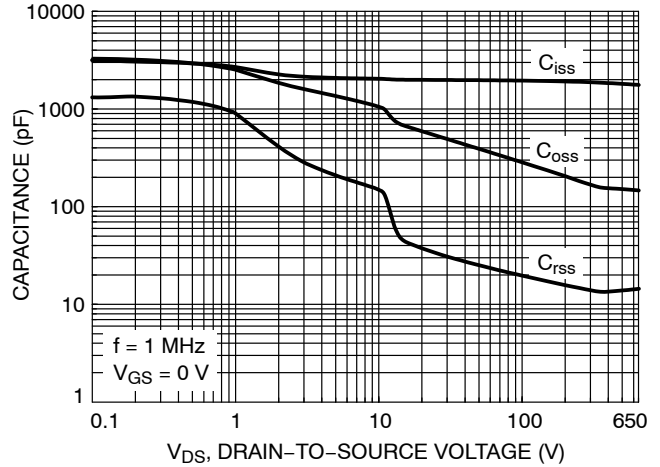


Figure 8. Capacitance vs. Drain-to-Source Voltage

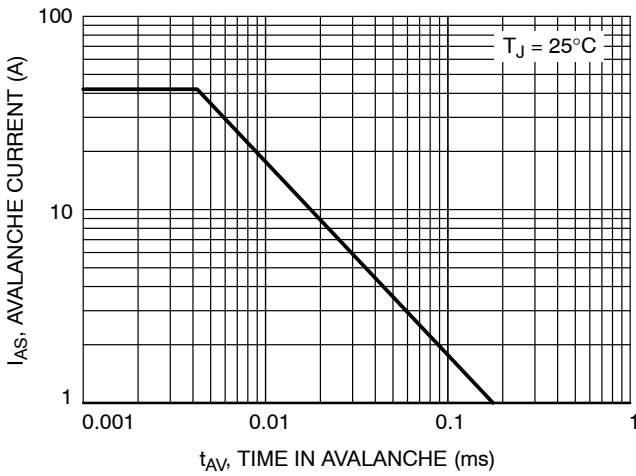


Figure 9. Unclamped Inductive Switching Capability

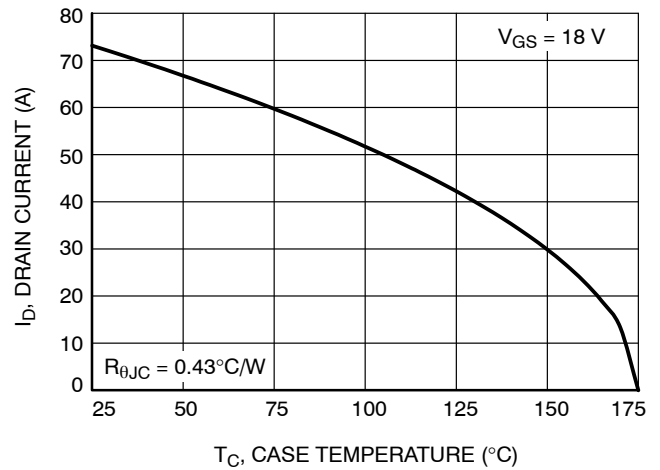


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

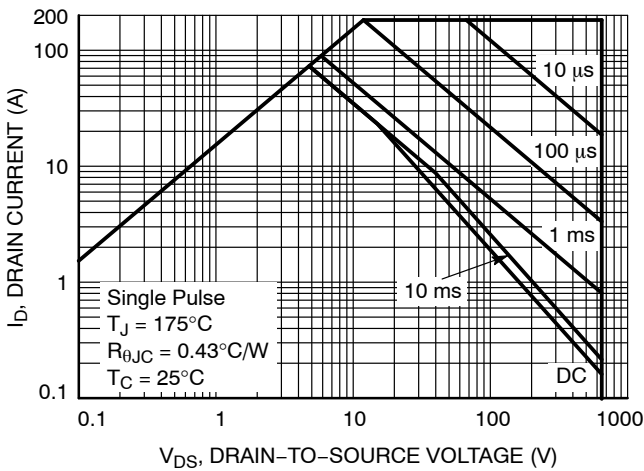


Figure 11. Safe Operating Area

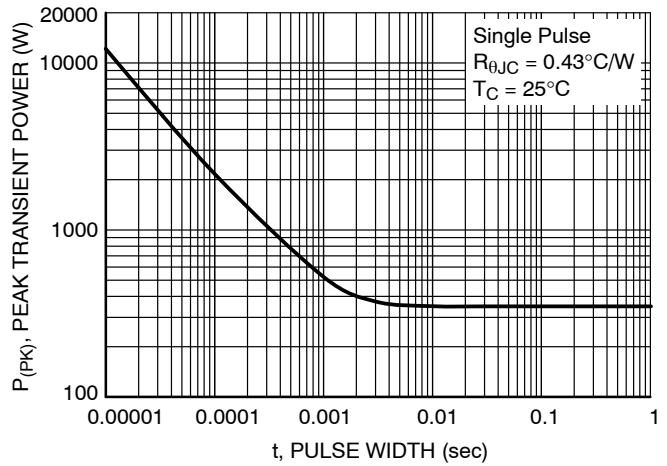
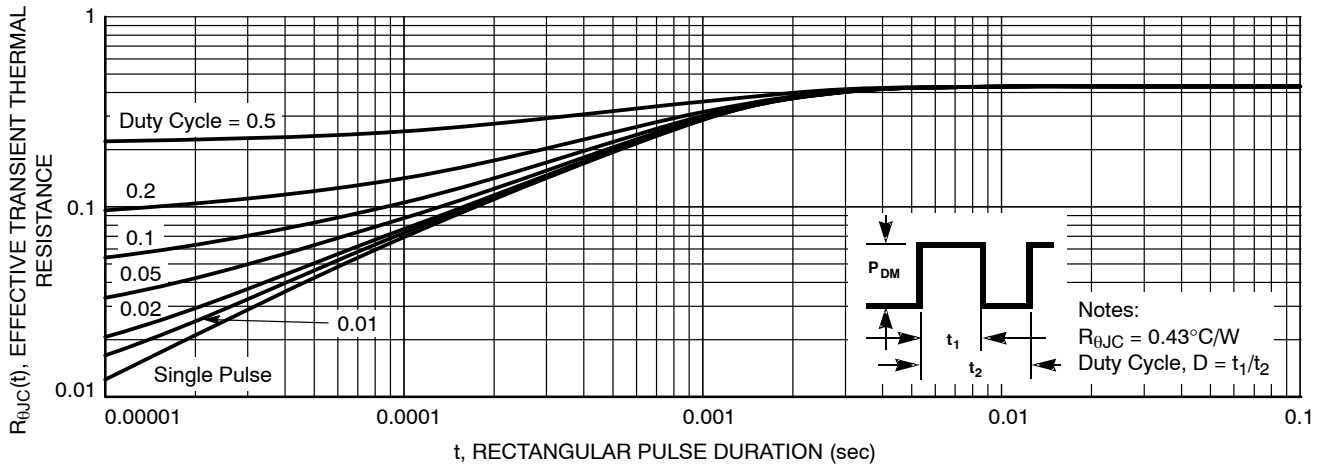


Figure 12. Single Pulse Maximum Power Dissipation

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## TYPICAL CHARACTERISTICS



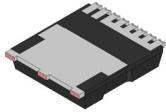
**Figure 13. Transient Thermal Impedance**

### DEVICE ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NTBL045N065SC1	H-PSOF8L	2000 / Tape & Reel

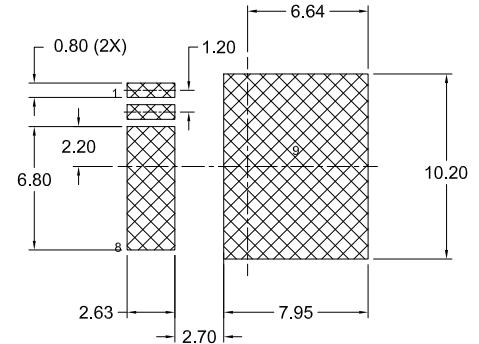
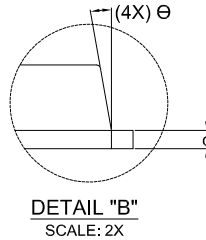
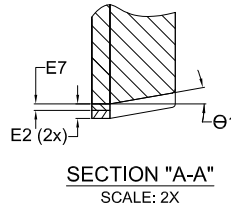
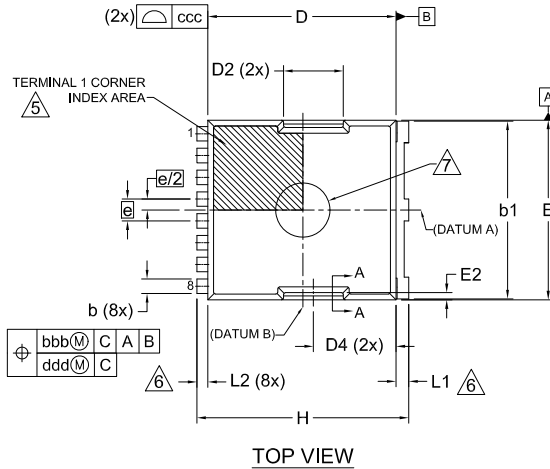
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



## H-PSOF8L 9.90x10.38x2.30, 1.20P CASE 100DC ISSUE C

DATE 31 MAY 2024

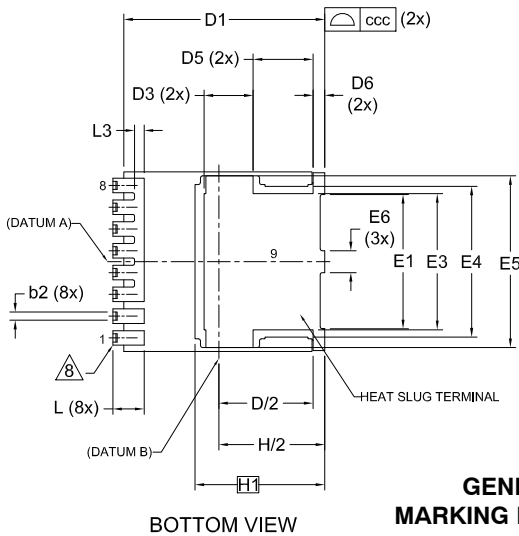
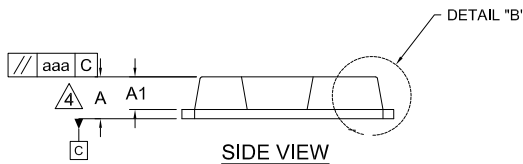


**LAND PATTERN  
RECOMMENDATION**

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERMD.

**NOTES:**

1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE B.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
3. "e" REPRESENTS THE TERMINAL PITCH.
4. THIS DIMENSION INCLUDES ENCAPSULATION THICKNESS "A1", AND PACKAGE BODY THICKNESS, BUT DOES NOT INCLUDE ATTACHED FEATURES, e.g., EXTERNAL OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AS ATTACHED FEATURE.
5. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE HATCHED AREA.
6. DIMENSIONS b1, L1, L2 APPLY TO PLATED TERMINALS.
7. THE LOCATION AND SIZE OF EJECTOR MARKS ARE OPTIONAL.
8. THE LOCATION AND NUMBER OF FUSED LEADS ARE OPTIONAL.



**GENERIC  
MARKING DIAGRAM\***



XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
ZZ = Assembly Lot Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "μ", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	7.40	7.50	7.60
E4	8.20	8.30	8.40

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E5	9.36	9.46	9.47
E6	1.10	1.20	1.30
E7	0.15	0.18	0.21
e	1.20 BSC		
e/2	0.60 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.63	1.73	1.83
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.43	0.53	0.63
theta	10° REF		
theta 1	10° REF		
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

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<b>DESCRIPTION:</b>	<b>H-PSOF8L 9.90x10.38x2.30, 1.20P</b>	<b>PAGE 1 OF 1</b>

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