Dual-Chip NPN General-Purpose Amplifier

NSVT5551DW1

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1
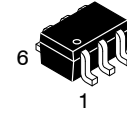
SOT−363/SC−88/
SC70−6
CASE 419B

Features

- This Device is Designed for General−purpose High Voltage Amplifier
- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Available in 8 mm, 7−inch/3,000 Unit Tape and Reel
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

(T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	160	V
Collector−Base Voltage	V_{CBO}	180	V
Emitter−Base Voltage	V_{EBO}	6.0	V
Collector Current − Continuous	I_C	200	mA
Operating and Storage Junction Temperature Range	T_J, T_{STG}	−55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. These ratings are based on a maximum junction temperature of 150°C.
2. These are steady−state limits. **onsemi** should be consulted on applications involving pulsed or low duty−cycle operations.

## THERMAL CHARACTERISTICS (Note 3)

(T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Max	Unit
Total Device Dissipation	P_D	200	mW
Derate Above 25°C		1.6	mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	625	°C/W

3. PCB size: FR−4, 76 mm x 114 mm x 1.57 mm (3.0 inch x 4.5 inch x 0.062 inch) with minimum land pattern size.

MARKING DIAGRAM

P1 M

1

P1 = Specific Device Code
M = Date Code

PIN ASSIGNMENT

(3) (2) (1)

Q_1 Q_2

(4) (5) (6)
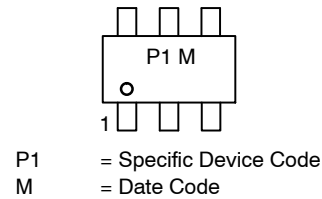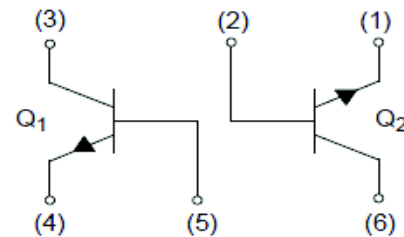
ORDERING INFORMATION

Device	Package	Shipping[†]
NSVT5551DW1T1G	SC88−6L (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NSVT5551DW1

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Max	Unit
Collector–Emitter Breakdown Voltage (Note 4)	BV_{CEO}	I_C = 1.0 mA, I_B = 0	160		V
Collector–Base Breakdown Voltage	BV_{CBO}	I_C = 100 μA, I_E = 0	180		V
Emitter–Base Breakdown Voltage	BV_{EBO}	I_E = 10 μA, I_C = 0	6.0		V
Collector Cut–Off Current	I_{CBO}	V_{CB} = 120 V, I_E = 0		50	nA
		V_{CB} = 120 V, I_E = 0, T_A = 100°C		50	μA
Emitter Cut–Off Current	I_{EBO}	V_{EB} = 4.0 V, I_C = 0		50	nA
DC Current Gain (Note 4)	h_{FE}	V_{CE} = 5 V, I_C = 1.0 mA	80		
		V_{CE} = 5 V, I_C = 10 mA	80	250	
		V_{CE} = 5 V, I_C = 50 mA	30		
Collector–Emitter Saturation Voltage (Note 4)	$V_{CE}(sat)$	I_C = 10 mA, I_B = 1.0 mA		0.15	V
		I_C = 50 mA, I_B = 5.0 mA		0.20	
Base–Emitter Saturation Voltage (Note 4)	$V_{BE}(sat)$	I_C = 10 mA, I_B = 1.0 mA		1.0	V
		I_C = 50 mA, I_B = 5.0 mA		1.0	
Current Gain Bandwidth Product	f_T	V_{CE} = 10 V, I_C = 10 mA, f = 100 MHz	100	300	MHz
Output Capacitance	C_{obo}	V_{CB} = 10 V, I_E = 0, f = 1.0 MHz		6.0	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
4. Pulse test: pulse width ≤ 300 μs, duty cycle ≤ 2.0%.
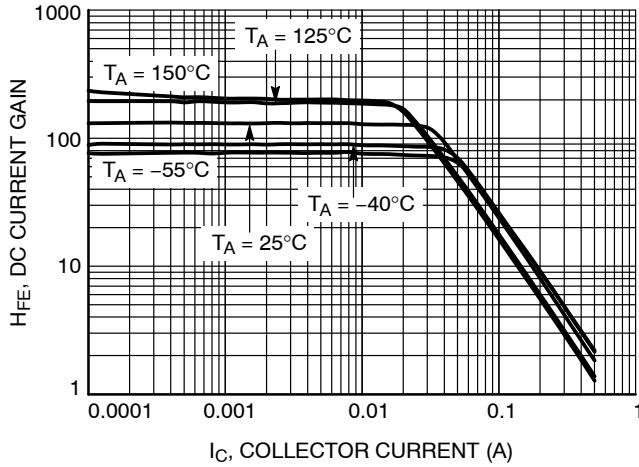
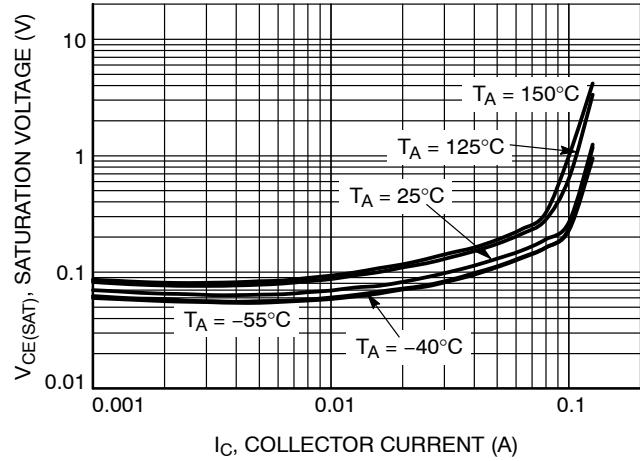## TYPICAL CHARACTERISTICS

Figure 1. DC Current Gain

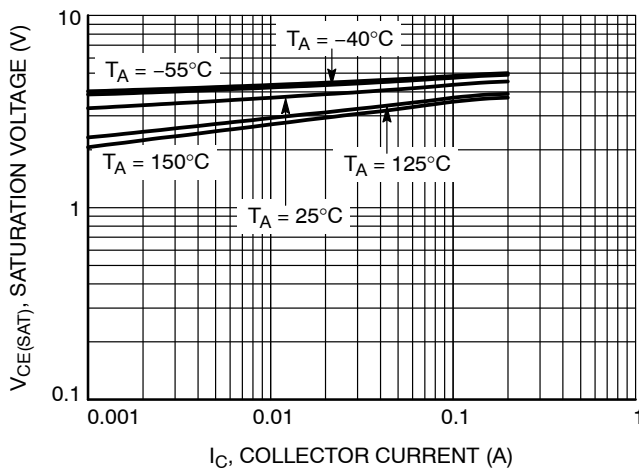**Figure 2. Collector−Emitter Saturation Voltage**

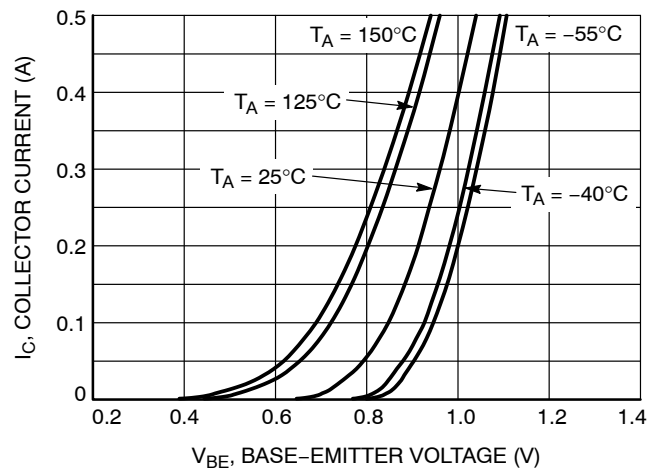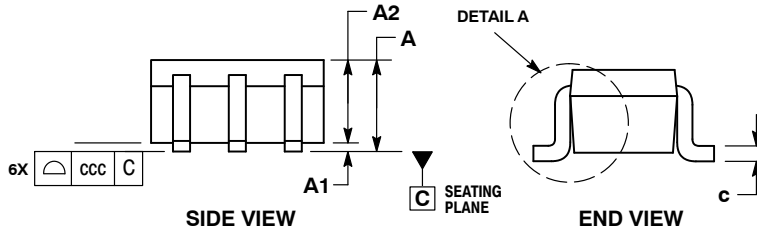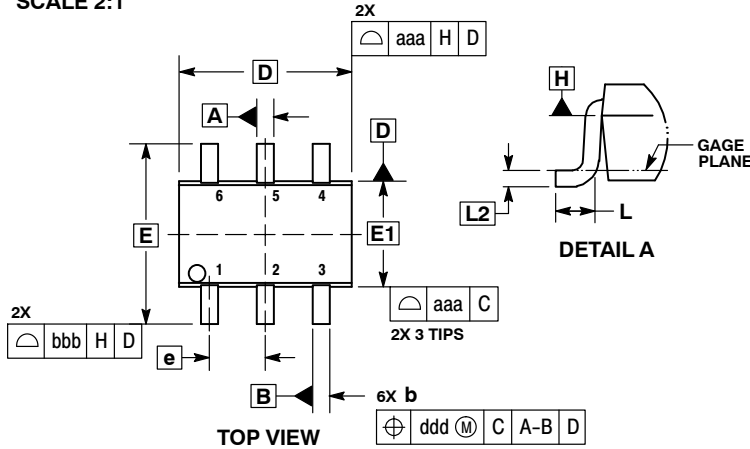
Figure 3. Base−Emitter Saturation Voltage

Figure 4. Base−Emitter ON Voltage

PACKAGE DIMENSIONS

SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE Y

DATE 11 DEC 2012

1
SCALE 2:1

2X
△ aaa H D

H

GAGE
PLANE

L2

L

DETAIL A

D

A

D

6 5 4

E

E1

1 2 3

2X
△ bbb H D

e

B

6X **b**

⊕ ddd Ⓜ C A−B D

△ aaa C

2X 3 TIPS

TOP VIEW

A2

A

DETAIL A

6X △ ccc C

A1

Ⓒ SEATING
PLANE

SIDE VIEW

DETAIL A

c

END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRU- SIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDI- TION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

**GENERIC
MARKING DIAGRAM***

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XXXM▪

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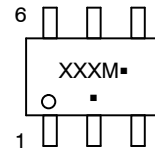
XXX = Specific Device Code

M   = Date Code*

▪   = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**RECOMMENDED
SOLDERING FOOTPRINT***

6X
0.30

6X
0.66

2.50

0.65
PITCH

DIMENSIONS: MILLIMETERS
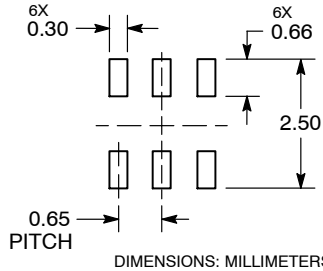
*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

NSVT5551DW1

PACKAGE DIMENSIONS

SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE Y

DATE 11 DEC 2012

STYLE 1:	STYLE 2:	STYLE 3:	STYLE 4:	STYLE 5:	STYLE 6:
PIN 1. EMITTER 2	CANCELLED	CANCELLED	PIN 1. CATHODE	PIN 1. ANODE	PIN 1. ANODE 2
2. BASE 2			2. CATHODE	2. ANODE	2. N/C
3. COLLECTOR 1			3. COLLECTOR	3. COLLECTOR	3. CATHODE 1
4. EMITTER 1			4. EMITTER	4. EMITTER	4. ANODE 1
5. BASE 1			5. BASE	5. BASE	5. N/C
6. COLLECTOR 2			6. ANODE	6. CATHODE	6. CATHODE 2

STYLE 7:	STYLE 8:	STYLE 9:	STYLE 10:	STYLE 11:	STYLE 12:
PIN 1. SOURCE 2	CANCELLED	PIN 1. EMITTER 2	PIN 1. SOURCE 2	PIN 1. CATHODE 2	PIN 1. ANODE 2
2. DRAIN 2		2. EMITTER 1	2. SOURCE 1	2. CATHODE 2	2. ANODE 2
3. GATE 1		3. COLLECTOR 1	3. GATE 1	3. ANODE 1	3. CATHODE 1
4. SOURCE 1		4. BASE 1	4. DRAIN 1	4. CATHODE 1	4. ANODE 1
5. DRAIN 1		5. BASE 2	5. DRAIN 2	5. CATHODE 1	5. ANODE 1
6. GATE 2		6. COLLECTOR 2	6. GATE 2	6. ANODE 2	6. CATHODE 2

STYLE 13:	STYLE 14:	STYLE 15:	STYLE 16:	STYLE 17:	STYLE 18:
PIN 1. ANODE	PIN 1. VREF	PIN 1. ANODE 1	PIN 1. BASE 1	PIN 1. BASE 1	PIN 1. VIN1
2. N/C	2. GND	2. ANODE 2	2. EMITTER 2	2. EMITTER 1	2. VCC
3. COLLECTOR	3. GND	3. ANODE 3	3. COLLECTOR 2	3. COLLECTOR 2	3. VOUT2
4. EMITTER	4. IOUT	4. CATHODE 3	4. BASE 2	4. BASE 2	4. VIN2
5. BASE	5. VEN	5. CATHODE 2	5. EMITTER 1	5. EMITTER 2	5. GND
6. CATHODE	6. VCC	6. CATHODE 1	6. COLLECTOR 1	6. COLLECTOR 1	6. VOUT1

STYLE 19:	STYLE 20:	STYLE 21:	STYLE 22:	STYLE 23:	STYLE 24:
PIN 1. I OUT	PIN 1. COLLECTOR	PIN 1. ANODE 1	PIN 1. D1 (i)	PIN 1. Vn	PIN 1. CATHODE
2. GND	2. COLLECTOR	2. N/C	2. GND	2. CH1	2. ANODE
3. GND	3. BASE	3. ANODE 2	3. D2 (i)	3. Vp	3. CATHODE
4. V CC	4. EMITTER	4. CATHODE 2	4. D2 (c)	4. N/C	4. CATHODE
5. V EN	5. COLLECTOR	5. N/C	5. VBUS	5. CH2	5. CATHODE
6. V REF	6. COLLECTOR	6. CATHODE 1	6. D1 (c)	6. N/C	6. CATHODE

STYLE 25:	STYLE 26:	STYLE 27:	STYLE 28:	STYLE 29:	STYLE 30:
PIN 1. BASE 1	PIN 1. SOURCE 1	PIN 1. BASE 2	PIN 1. DRAIN	PIN 1. ANODE	PIN 1. SOURCE 1
2. CATHODE	2. GATE 1	2. BASE 1	2. DRAIN	2. ANODE	2. DRAIN 2
3. COLLECTOR 2	3. DRAIN 2	3. COLLECTOR 1	3. GATE	3. COLLECTOR	3. DRAIN 2
4. BASE 2	4. SOURCE 2	4. EMITTER 1	4. SOURCE	4. EMITTER	4. SOURCE 2
5. EMITTER	5. GATE 2	5. EMITTER 2	5. DRAIN	5. BASE/ANODE	5. GATE 1
6. COLLECTOR 1	6. DRAIN 1	6. COLLECTOR 2	6. DRAIN	6. CATHODE	6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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