# SPM 49 Series
# Smart Power Module (SPM)
# Inverter, 1200 V, 50 A

# NFAL5012L5B

**ON Semiconductor®**

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### General Description

The NFAL5012L5B is a smart power module providing a fully−featured, high−performance inverter output stage for AC induction, BLDC, and PMSM motors. These modules integrate optimized gate drive of the built−in IGBTs to minimize EMI and losses, while also providing multiple on−module protection features: under−voltage lockouts, over−current shutdown, temperature sensing, and fault reporting. The built−in, high−speed HVIC requires only a single supply voltage and translates the incoming logic−level gate inputs to high−voltage, high−current drive signals to properly drive the module's internal IGBTs. Separate negative IGBT terminals are available for each phase to support the widest variety of control algorithms.

### Features

- 1200 V – 50 A 3−Phase IGBT Inverter, Including Control ICs for Gate Drive and Protections
- Low−Loss, Short−Circuit-Rated IGBTs
- Very Low Thermal Resistance Using $Al_2O_3$ DBC Substrate
- Built−In Bootstrap Diodes/Resistors
- Separate Open-Emitter Pins from Low−Side IGBTs for Three−Phase Current Sensing
- Adjustable Over−Current Protection via Integrated Sense−IGBTs
- Isolation Rating of 2500 Vrms/1 min
- These Devices are RoHS Compliant

### Typical Applications

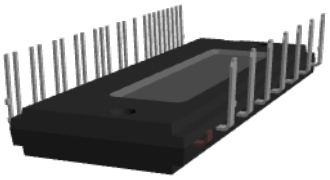
- Motion Control − Industrial Motor (AC 400 V Class)

### Integrated Power Functions

- 1200 V – 50 A IGBT Inverter for Three−Phase DC/AC Power Conversion (Refer to Figure 2)

### Integrated Drive, Protection, and System Control Functions

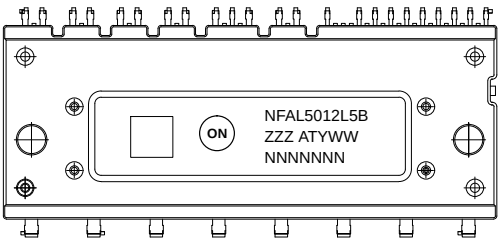
- For Inverter High−Side IGBTs: gate−drive circuit, high−voltage isolated high−speed level−shifting control circuit, Under−Voltage Lock−Out protection (UVLO), available bootstrap circuit example is given in Figures 4 and 15
- For Inverter Low−Side IGBTs: gate−drive circuit, Short−Circuit Protection (SCP) control circuit, Under−Voltage Lock−Out protection (UVLO)
- Fault Signaling: corresponding to UV (low−side supply) and SC faults
- Input Interface: active−HIGH interface, works with 3.3 V/5 V logic, Schmitt−trigger input



3D Package Drawing
(Click to Activate 3D Content)

**SPM49−CAA**
**CASE MODGR**

### MARKING DIAGRAM




| | |
|---|---|
| NFAL5012L5B | = Specific Device Code |
| ZZZ | = Lot ID |
| AT | = Assembly & Test Location |
| Y | = Year |
| WW | = Work Week |
| NNNNNNN | = Serial Number |

### ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

## PIN CONFIGURATION

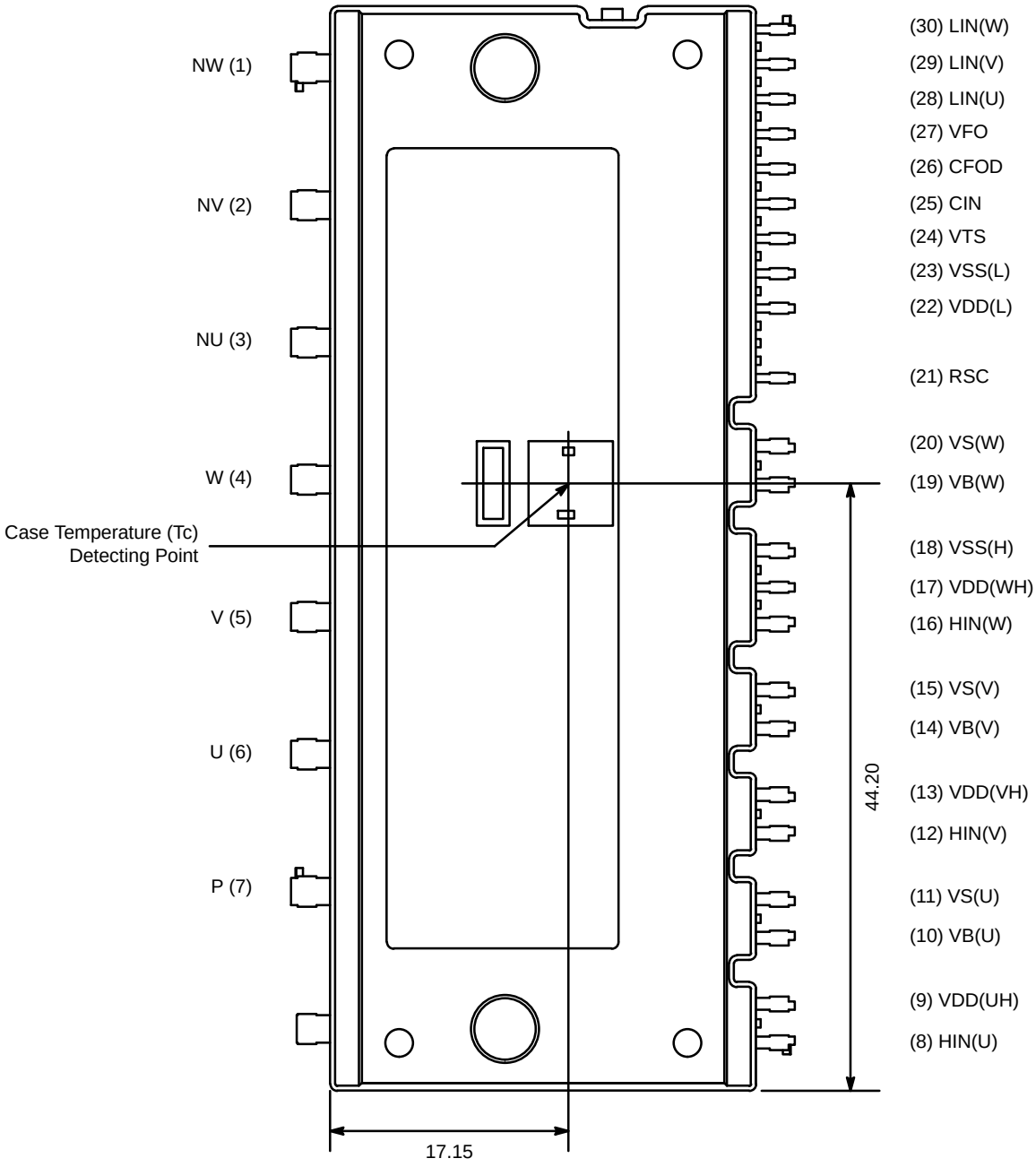
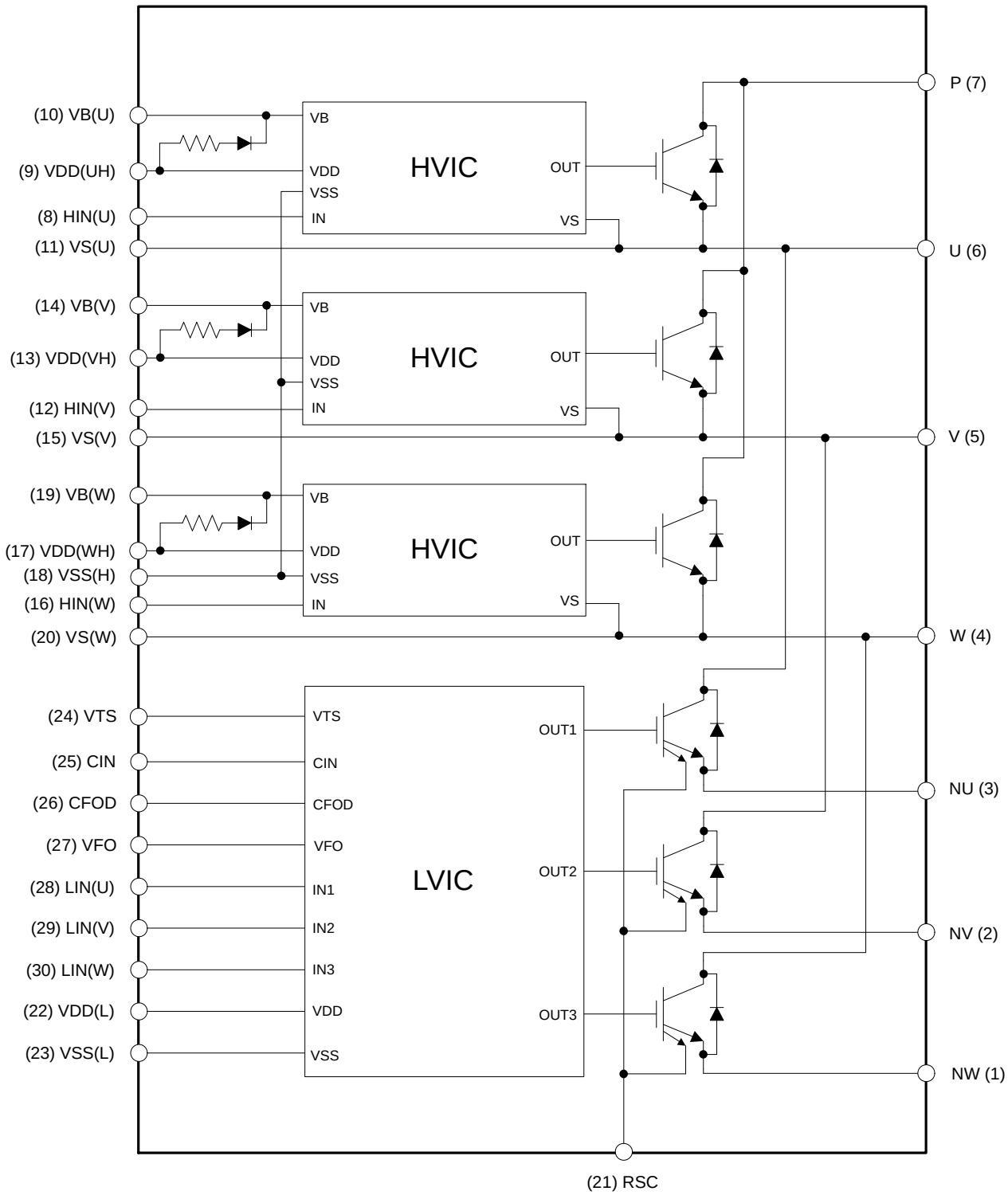



**Figure 1. Pin Configuration − Top View**

**PIN DESCRIPTION**

| Pin Number | Pin Name | Pin Description |
|---|---|---|
| 1 | NW | Negative DC−Link Input for W Phase |
| 2 | NV | Negative DC−Link Input for V Phase |
| 3 | NU | Negative DC−Link Input for U Phase |
| 4 | W | Output for W Phase |
| 5 | V | Output for V Phase |
| 6 | U | Output for U Phase |
| 7 | P | Positive DC−Link Input |
| 8 | HIN(U) | Signal Input for High−Side U Phase |
| 9 | VDD(UH) | High−Side Bias Voltage for U Phase IC |
| 10 | VB(U) | High−Side Bias Voltage for U Phase IGBT Driving |
| 11 | VS(U) | High−Side Bias Voltage GND for U Phase IGBT Driving |
| 12 | HIN(V) | Signal Input for High−Side V Phase |
| 13 | VDD(VH) | High−Side Bias Voltage for V Phase IC |
| 14 | VB(V) | High−Side Bias Voltage for V Phase IGBT Driving |
| 15 | VS(V) | High−Side Bias Voltage GND for V Phase IGBT Driving |
| 16 | HIN(W) | Signal Input for High−Side W Phase |
| 17 | VDD(WH) | High−Side Bias Voltage for W Phase IC |
| 18 | VSS(H) | High−Side Common Supply Ground, connected to HVIC |
| 19 | VB(W) | High−Side Bias Voltage for W Phase IGBT Driving |
| 20 | VS(W) | High−Side Bias Voltage GND for W Phase IGBT Driving |
| 21 | RSC | Resistor for Over and Short−Circuit Current Detection |
| 22 | VDD(L) | Low−Side Bias Voltage for IC and IGBTs Driving |
| 23 | VSS(L) | Low−Side Common Supply Ground, connected to LVIC |
| 24 | VTS | Voltage Output for LVIC Temperature Sensing Unit |
| 25 | CIN | Input for Current Protection |
| 26 | CFOD | Capacitor for Fault Output Duration Selection |
| 27 | VFO | Fault Output |
| 28 | LIN(U) | Signal Input for Low−Side U Phase |
| 29 | LIN(V) | Signal Input for Low−Side V Phase |
| 30 | LIN(W) | Signal Input for Low−Side W Phase |

## INTERNAL EQUIVALENT CIRCUIT AND INPUT/OUTPUT PINS




NOTES:

1. Inverter high−side is composed of three normal−IGBTs, freewheeling diodes, and one control IC for each IGBT.
2. Inverter low−side is composed of three sense−IGBTs, freewheeling diodes, and one control IC for each IGBT. It has gate drive and protection functions.
3. Inverter power side is composed of four inverter DC−link input terminals and three inverter output terminals.

**Figure 2. Internal Block Diagram**

**ABSOLUTE MAXIMUM RATINGS** (Tj = 25°C unless otherwise noted)

| Symbol | Rating | Conditions | Rating | Unit |
|---|---|---|---|---|
| **INVERTER PART** | | | | |
| VPN | Supply Voltage | Applied between P − NU, NV, NW | 900 | V |
| VPN(surge) | Supply Voltage (Surge) | Applied between P − NU, NV, NW | 1000 | V |
| Vces | Collector−Emitter Voltage | | 1200 | V |
| ±Ic | Each IGBT Collector Current | Tc = 25°C, Tj ≤ 150°C | 50 | A |
| ±Icp | Each IGBT Collector Current (Peak) | Tc = 25°C, Tj ≤ 150°C, Under 1 ms Pulse Width (Note 4) | 100 | A |
| Pc | Collector Dissipation | Tc = 25°C per One Chip (Note 4) | 219 | W |
| Tj | Operating Junction Temperature | | −40~150 | °C |
| **CONTROL PART** | | | | |
| VDD | Control Supply Voltage | Applied between VDD(H), VDD(L) − VSS | 20 | V |
| VBS | High−Side Control Bias Voltage | Applied between VB(U) − VS(U), VB(V) − VS(V), VB(W) − VS(W) | 20 | V |
| VIN | Input Signal Voltage | Applied between HIN(U), HIN(V), HIN(W), LIN(U), LIN(V), LIN(W) − VSS | −0.5~VDD+0.5 | V |
| VFO | Fault Output Supply Voltage | Applied between VFO − VSS | −0.5~VDD+0.5 | V |
| IFO | Fault Output Current | Sink Current at VFO pin | 5 | mA |
| VCIN | Current Sensing Input Voltage | Applied between CIN − VSS | −0.5~VDD+0.5 | V |
| Tj | Operating Junction Temperature | | −40~150 | °C |
| **BOOSTSTRAP DIODE PART** | | | | |
| VRRM | Maximum Repetitive Reverse Voltage | | 1200 | V |
| Tj | Operating Junction Temperature | | −40~150 | °C |
| **TOTAL SYSTEM** | | | | |
| VPN(PROT) | Self−Protection Supply Voltage Limit (Short−Circuit Protection Capability) | VDD = VBS = 13.5~16.5 V, Tj = 150°C, Vces < 1200 V, Non-Repetitive, < 2 μs | 800 | V |
| Tc | Module Case Operation Temperature | See Figure 1 | −40~125 | °C |
| Tstg | Storage Temperature | | −40~125 | °C |
| Viso | Isolation Voltage | 60 Hz, Sinusoidal, AC 1 Minute, Connection Pins to Heat Sink Plate | 2500 | Vrms |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. These values had been made an acquisition by the calculation considered to design factor.

**THERMAL RESISTANCE**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Rth(j-c)Q | Junction−to−Case Thermal Resistance (Note 5) | Inverter IGBT Part (per 1/6 module) | − | − | 0.57 | °C/W |
| Rth(j-c)F | | Inverter FWDi Part (per 1/6 module) | − | − | 1.15 | °C/W |

5. For the measurement point of case temperature (Tc), please refer to Figure 1. DBC discoloration and Picker Circle Printing allowed, please refer to application note AN−9190 (Impact of DBC Oxidation on SPM® Module Performance).

**ELECTRICAL CHARACTERISTICS** (Tj = 25°C unless otherwise specified.)

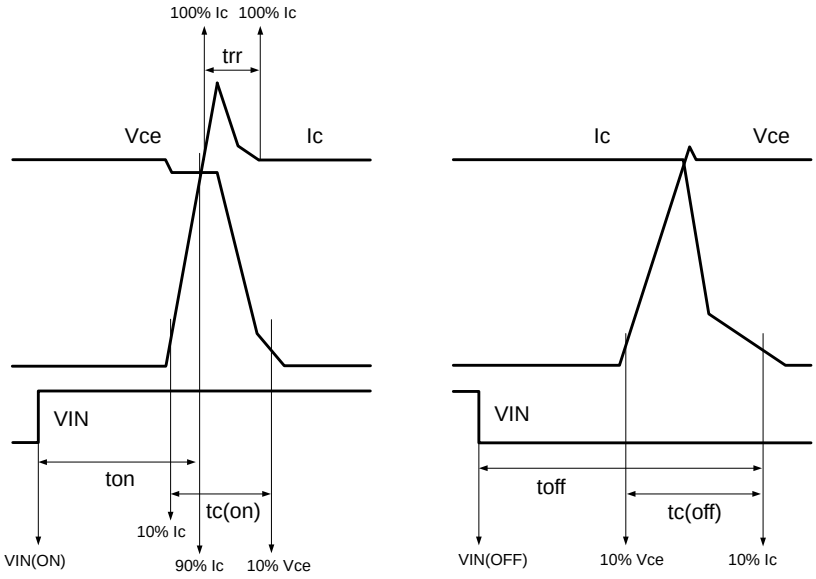
| Symbol | | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| **INVERTER PART** | | | | | | | | |
| VCE(sat) | | Collector−Emitter Saturation Voltage | VDD = VBS = 15 V<br>IN = 5 V | Ic = 50 A, Tj = 25°C | − | 2.00 | 2.50 | V |
| VF | | FWDi Forward Voltage | IN = 0 V | Ic = −50 A, Tj = 25°C | − | 2.30 | 2.90 | V |
| HS | ton | Switching Times | VPN = 600 V, VDD = 15 V, Ic = 50 A<br>Tj = 25°C<br>IN = 0 V ↔ 5 V, Inductive Load<br>See Figure 3<br>(Note 6) | | 1.10 | 1.70 | 2.30 | μs |
| | tc(on) | | | | − | 0.25 | 0.55 | μs |
| | toff | | | | − | 1.50 | 2.10 | μs |
| | tc(off) | | | | − | 0.15 | 0.45 | μs |
| | trr | | | | − | 0.25 | − | μs |
| LS | ton | | VPN = 600 V, VDD = 15 V, Ic = 50 A<br>Tj = 25°C<br>IN = 0 V ↔ 5 V, Inductive Load<br>See Figure 3<br>(Note 6) | | 1.00 | 1.60 | 2.20 | μs |
| | tc(on) | | | | − | 0.25 | 0.55 | μs |
| | toff | | | | − | 1.40 | 2.00 | μs |
| | tc(off) | | | | − | 0.15 | 0.45 | μs |
| | trr | | | | − | 0.25 | − | μs |
| Ices | | Collector−Emitter Leakage Current | Vce = Vces | | − | − | 1 | mA |
| **CONTROL PART** | | | | | | | | |
| IQDDH | | Quiescent VDD Supply Current | VDD(UH,VH,WH) = 15 V,<br>HIN(U,V,W) = 0 V | VDD(UH) − VSS(H),<br>VDD(VH) − VSS(H),<br>VDD(WH) − VSS(H) | − | − | 0.30 | mA |
| IQDDL | | | VDD(L) = 15 V,<br>LIN(U,V,W) = 0 V | VDD(L) − VSS(L) | − | − | 3.50 | mA |
| IPDDH | | Operating VDD Supply Current | VDD(UH,VH,WH) = 15 V,<br>FPWM = 20 kHz,<br>Duty = 50%, Applied to one PWM Signal Input for High−Side | VDD(UH) − VSS(H),<br>VDD(VH) − VSS(H),<br>VDD(WH) − VSS(H) | − | − | 0.40 | mA |
| IPDDL | | | VDD(L) = 15 V,<br>FPWM = 20 kHz,<br>Duty = 50%, Applied to one PWM Signal Input for Low−Side | VDD(L) − VSS(L) | − | − | 7.50 | mA |
| IQBS | | Quiescent VBS Supply Current | VDD = VBS = 15 V,<br>HIN(U,V,W) = 0 V | VB(U) − VS(U),<br>VB(V) − VS(V),<br>VB(W) − VS(W) | − | − | 0.30 | mA |
| IPBS | | Operating VBS Supply Current | VDD = VBS = 15 V,<br>FPWM = 20 kHz,<br>Duty = 50%, Applied to one PWM Signal Input for High−Side | VB(U) − VS(U),<br>VB(V) − VS(V),<br>VB(W) − VS(W) | − | − | 6.50 | mA |
| VFOH | | Fault Output Voltage | VDD = 15 V, CIN = 0 V,<br>VFO Circuit: 10 kΩ to 5 V Pull−up | | 4.90 | − | − | V |
| VFOL | | | VDD = 15 V, CIN = 1 V, IFO = 1 mA | | − | − | 0.95 | V |
| ISEN | | Sensing Current of Each Sense IGBT | VDD = 15 V, LIN = 5 V,<br>Rsc = 0 Ω,<br>No Connection of Shunt Resistor at NU, NV, NW Terminal | Ic = 50 A | − | 22 | − | mA |
| VSC(ref) | | Short Circuit Trip Level | VDD = 15 V | CIN − VSS(L) | 0.46 | 0.48 | 0.50 | V |
| ISC | | Short Circuit Current Level for Trip | Rsc = 18 Ω (±1%), No Connection of Shunt Resistor at NU, NV, NW Terminal (Note 7) | | 75 | − | − | A |

**ELECTRICAL CHARACTERISTICS** (Tj = 25°C unless otherwise specified.) (continued)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **CONTROL PART** | | | | | | |
| UVDDD | Supply Circuit Under−Voltage Protection | Detection Level | 10.3 | − | 12.5 | V |
| UVDDR | | Reset Level | 10.8 | − | 13.0 | V |
| UVBSD | | Detection Level | 10.0 | − | 12.0 | V |
| UVBSR | | Reset Level | 10.5 | − | 12.5 | V |
| VIN(ON) | ON Threshold Voltage | Applied between HIN(U,V,W) − VSS(H), LIN(U,V,W) − VSS(L) | − | − | 2.6 | V |
| VIN(OFF) | OFF Threshold Voltage | | 0.8 | − | − | V |
| VTS | Voltage Output for LVIC Temperature Sensing Unit | VDD(L) = 15 V, TLVIC = 25°C See Figure 6 and 7 (Note 8) | 0.909 | 1.030 | 1.151 | V |
| tFOD | Fault-Out Pulse Width | CFOD = 22 nF (Note 9) | 1.6 | − | − | ms |
| **BOOTSTRAP DIODE/RESISTOR PART** | | | | | | |
| VF | Forward Voltage | If = 0.1 A, Tj = 25°C, See Figure 8 | 2.1 | 2.5 | 2.9 | V |
| RBOOT | Bootstrap Resistor | | 12.5 | 15.5 | 18.5 | Ω |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. ton and toff include the propagation delay of the internal drive IC. tc(on) and tc(off) are the switching times of IGBT under the given gate-driving condition internally. For the detailed information, please see Figure 3.
7. Short-circuit current protection functions only at the low-sides because the sense current is divided from main current at low-side IGBTs. Inserting the shunt resistor for monitoring the phase current at NU, NV, NW terminal, the trip level of the short-circuit current is changed.
8. TLVIC is the temperature of LVIC itself. VTS is only for sensing temperature of LVIC and cannot shutdown IGBTs automatically. The relationship between VTS voltage output and LVIC temperature is described in Figure 6. It is recommended to add a ceramic capacitor of 10 nF or more between VTS and VSS (Signal Ground) to make the VTS more stable as described in Figure 7. Refer to the application note for this products about usage of VTS.
9. The fault-out pulse width tFOD depends on the capacitance value of CFOD according to the following approximate equation: $tFOD = 0.1 \times 10^6 \times CFOD$ [s].




**(a) turn-on** **(b) turn-off**

**Figure 3. Switching Time Definition**

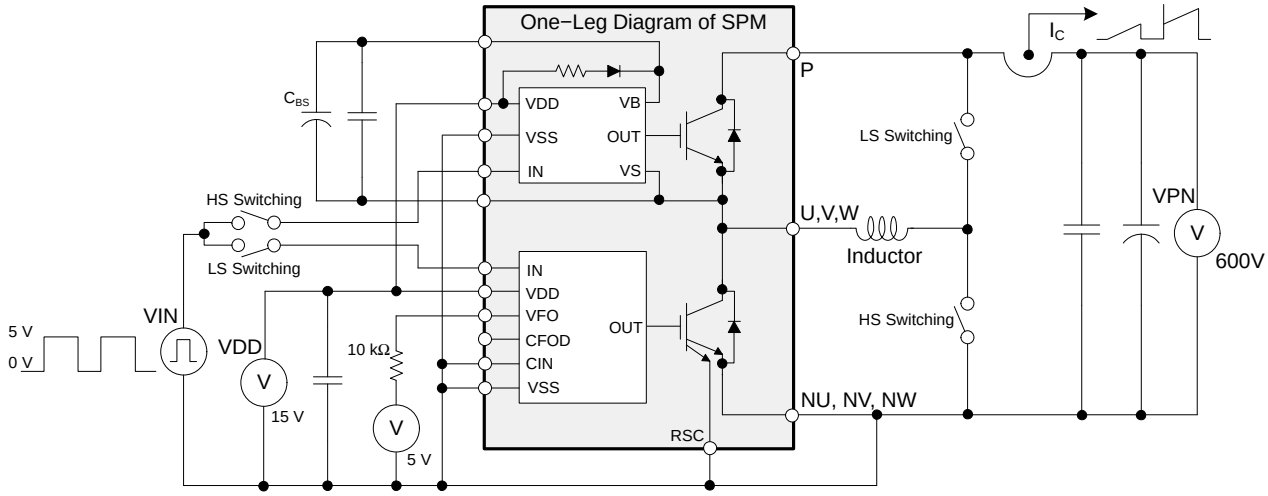



**Figure 4. Example Circuit of Switching Test**

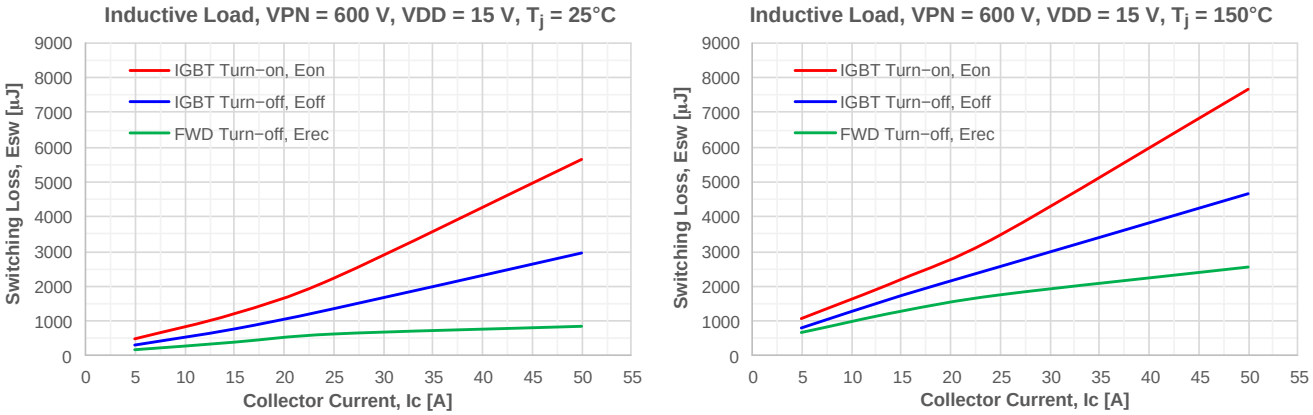



**Figure 5. Switching Loss Characteristics**

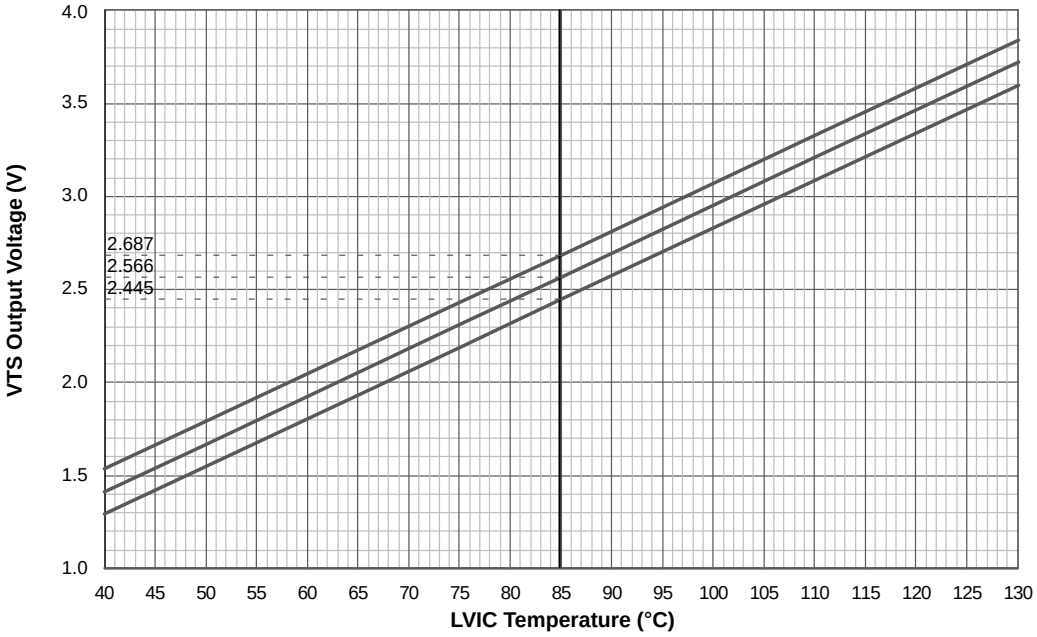



**Figure 6. Temperature Profile of VTS**

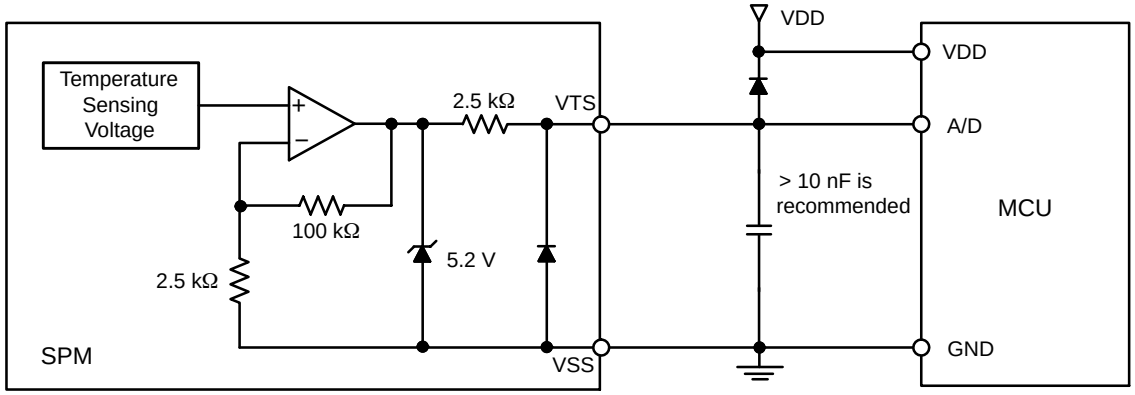



**Figure 7. Internal Block Diagram and Interface Circuit of VTS**

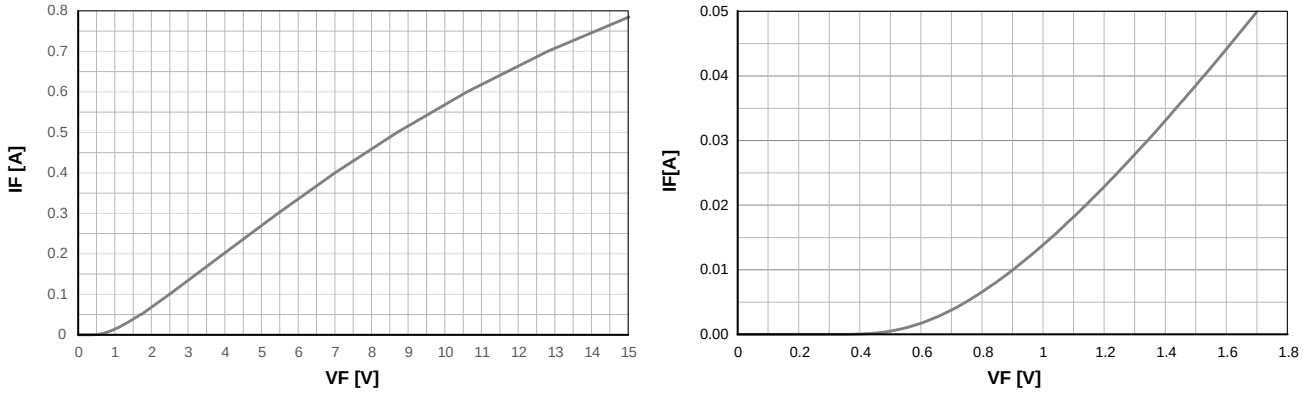



**Figure 8. Characteristics of Bootstrap Diode/Resistor (Right Figure is Enlarged Figure)**

**RECOMMENDED OPERATING RANGES**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| VPN | Supply Voltage | Applied between P−NU, NV, NW | | 350 | 600 | 800 | V |
| VDD | Control Supply Voltage | Applied between VDD(UH,VH,WH)−VSS(H), VDD(L)−VSS(L) | | 13.5 | 15.0 | 16.5 | V |
| VBS | High−Side Control Bias Voltage | Applied between VB(U)−VS(U), VB(V)−VS(V), VB(W)−VS(W) | | 13.0 | 15.0 | 18.5 | V |
| dVDD/dt, dVBS/dt | Control Supply Variation | | | −1 | − | +1 | V/μs |
| tdead | Blanking Time for Preventing Arm − Short | For Each Input Signal | | 2.0 | − | − | μs |
| FPWM | PWM Input Signal | −40°C ≤ Tc ≤ 125°C, −40°C ≤ Tj ≤ 150°C | | − | − | 20 | kHz |
| Io | Allowable r.m.s. Output Current | VPN = 600 V, VDD = VBS = 15 V, P.F = 0.8, Sinusoidal PWM Tc ≤ 125°C, Tj ≤ 150°C (Note 10) | FPWM = 5 kHz | − | − | 25 | Arms |
| | | | FPWM = 15 kHz | − | − | 14 | |
| VSEN | Voltage for Current Sensing | Applied between NU, NV, NW − VSS (Including Surge Voltage) | | −5.0 | − | +5.0 | V |
| PWIN(ON) | Minimum Input Pulse Width | (Note 11) | | 1.5 | − | − | μs |
| PWIN(OFF) | | VDD = VBS = 15 V, Ic ≤ 100 A, Wiring Inductance between NU, NV, NW and DC Link N < 10 nH (Note 11) | | 2.0 | − | − | |
| Tj | Junction Temperature | | | −40 | − | +150 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

10. This allowable output current value is the reference data for the safe operation of this product. This may be different from the actual application and operating condition.
11. This product might not make output response if input pulse width is less than the recommended value.

## PACKAGE MARKING AND ORDERING INFORMATION

| Device | Device Marking | Package | Shipping |
|---|---|---|---|
| NFAL5012L5B | NFAL5012L5B | SPM49−CAA | 6 Units/Tube |

## MECHANICAL CHARACTERISTICS AND RATINGS

| Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Device Flatness | See Figure 9 | | −50 | − | 100 | μm |
| Mounting Torque | Mounting Screw: M4<br>See Figure 10 | Recommended 1.18 N · m | 0.98 | 1.18 | 1.47 | N · m |
| | | Recommended 12.03 kg · cm | 10.00 | 12.03 | 14.98 | kg · cm |
| Terminal Pulling Strength | Load 19.6 N | | 10 | − | − | s |
| Terminal Bending Strength | Load 9.8 N, 90 degrees Bend | | 2 | − | − | times |
| Weight | | | − | 44.5 | − | g |

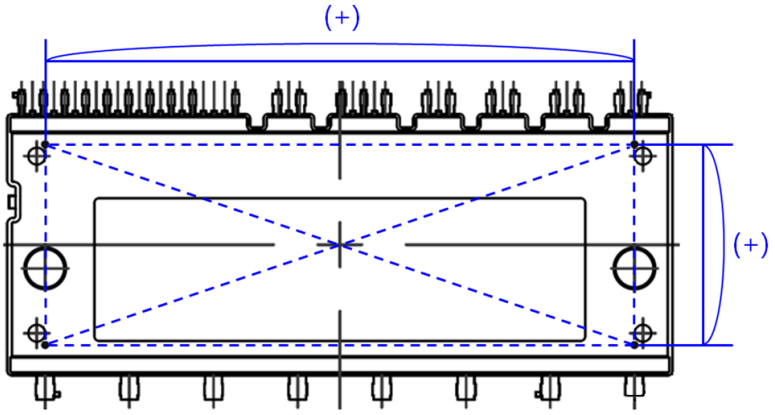
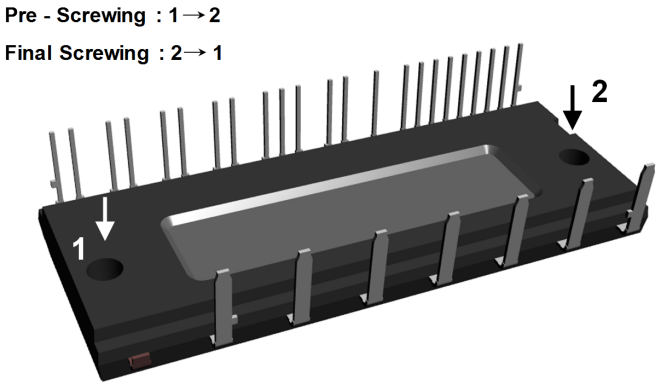



**Figure 9. Flatness Measurement Position**

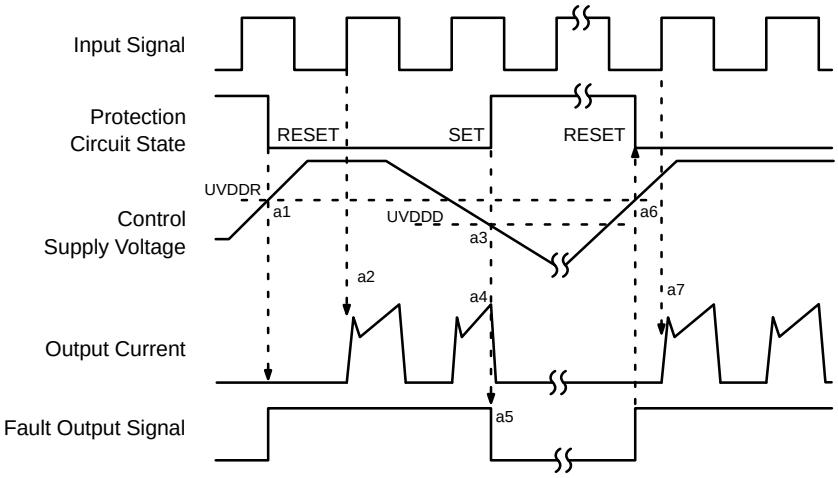



NOTES:

12. Do not over torque when mounting screws. Too much mounting torque may cause DBC cracks, as well as bolts and Al heat−sink destruction.
13. Avoid one−sided tightening stress. Figure 10 shows the recommended torque order for the mounting screws. Uneven mounting can cause the DBC substrate of package to be damaged. The pre−screwing torque is set to 20~30% of maximum torque rating.

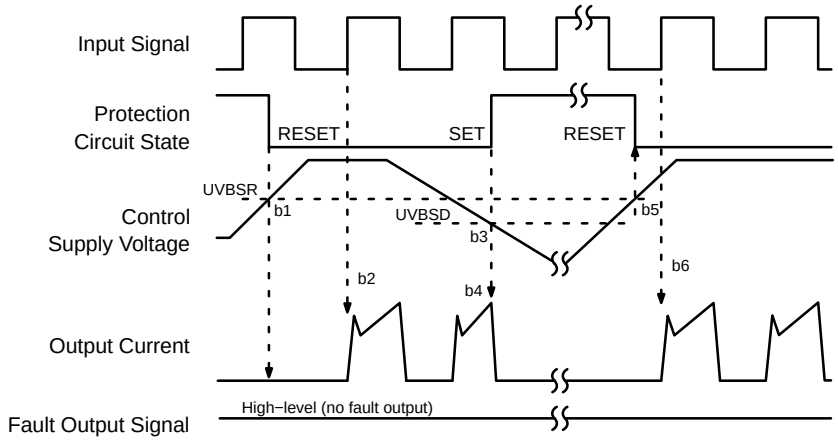
**Figure 10. Mounting Screws Torque Order**

## TIME CHARTS OF SPMs PROTECTIVE FUNCTION



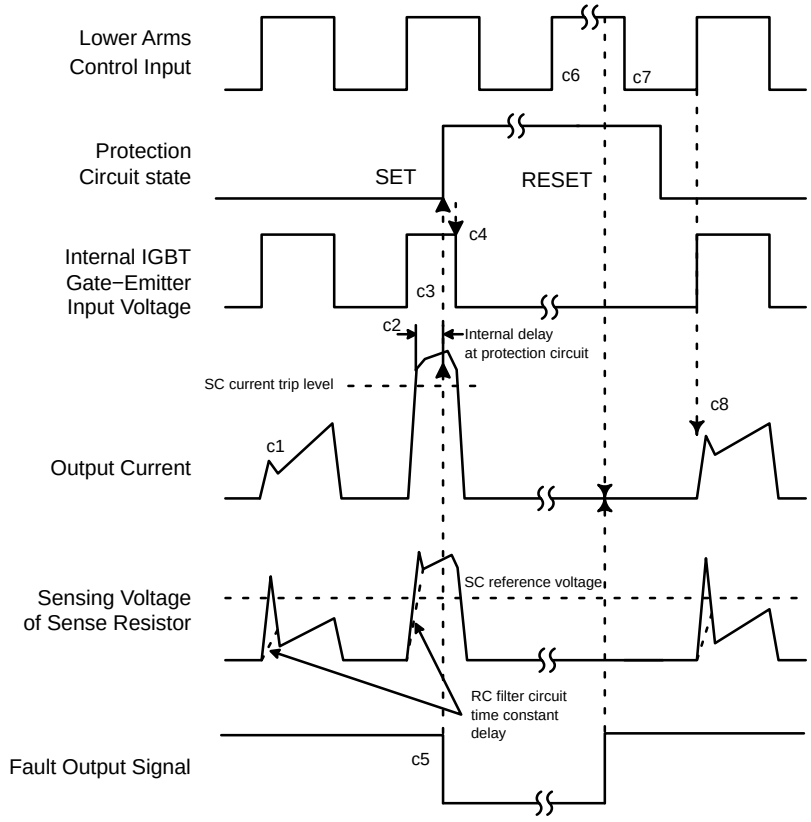

a1: Control supply voltage rises: after the voltage rises UVDDR, the circuits start to operate when the next input is applied.
a2: Normal operation: IGBT ON and carrying current.
a3: Under−voltage detection (UVDDD).
a4: IGBT OFF in spite of control input condition.
a5: Fault output operation starts with a fixed pulse width according to the condition of the external capacitor CFOD.
a6: Under−voltage reset (UVDDR).
a7: Normal operation: IGBT ON and carrying current by triggering next signal from LOW to HIGH.

**Figure 11. Under-voltage Protection (Low-side)**




b1: Control supply voltage rises: after the voltage reaches UVBSR, the circuits start to operate when the next input is applied.
b2: Normal operation: IGBT ON and carrying current.
b3: Under−voltage detection (UVBSD).
b4: IGBT OFF in spite of control input condition, but there is no fault output signal.
b5: Under−voltage reset (UVBSR).
b6: Normal operation: IGBT ON and carrying current by triggering next signal from LOW to HIGH.

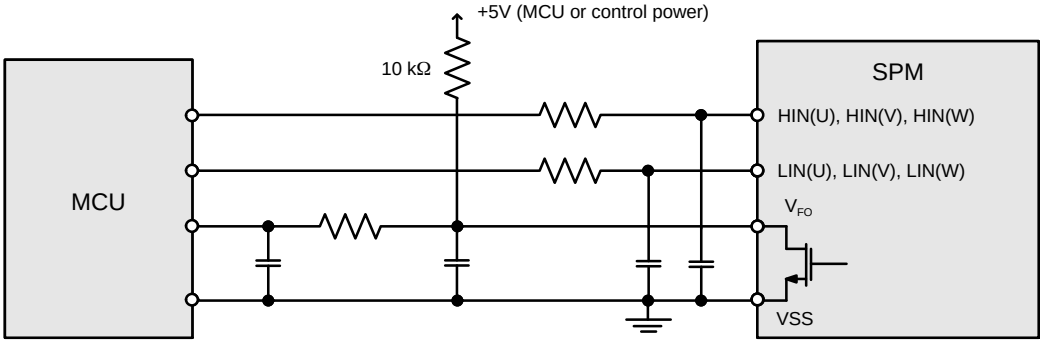
**Figure 12. Under-voltage Protection (High-side)**




(With the external sense resistance and RC filter connection)
c1: Normal operation: IGBT ON and carrying current.
c2: Short−circuit current detection (SC trigger).
c3: All low−side IGBTs gate are hard interrupted.
c4: All low−side IGBTs turn OFF.
c5: Fault output operation starts with a fixed pulse width according to the condition of the external capacitor CFOD.
c6: Input HIGH − IGBT ON state, but during the active period of fault output, the IGBT doesn't turn ON.
c7: Fault output operation finishes, but IGBT doesn't turn on until triggering the next signal from LOW to HIGH.
c8: Normal operation: IGBT ON and carrying current.

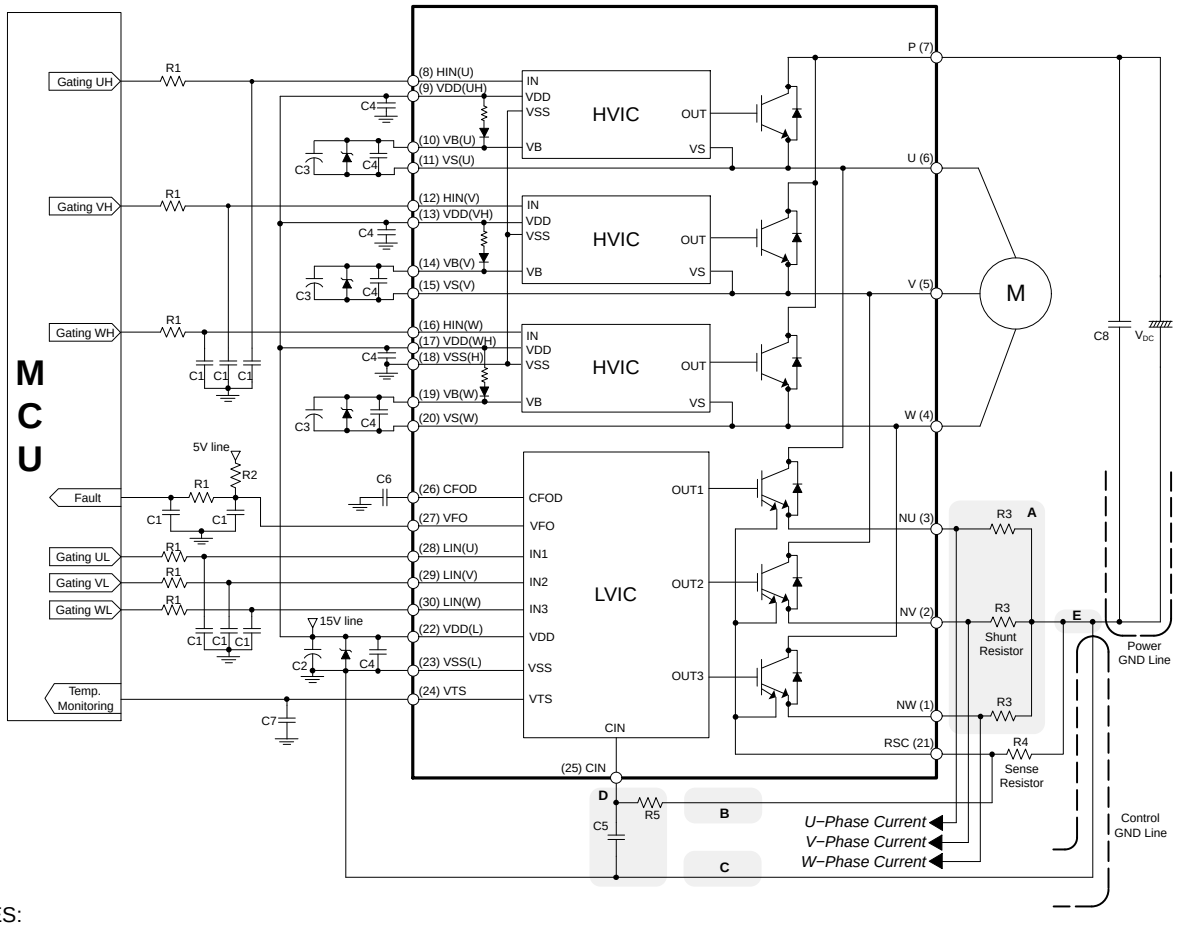
**Figure 13. Short-circuit Current Protection (Low-side Operation Only)**

## INPUT/OUTPUT INTERFACE CIRCUIT




NOTE:
14. RC coupling at each input might change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board. The input signal section of the SPM49 product integrates 5 kΩ (typ.) pull−down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

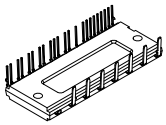
**Figure 14. Recommended MCU I/O Interface Circuit**




NOTES:

15. To avoid malfunction, the wiring of each input should be as short as possible (less than 2−3 cm).
16. VFO output is an open−drain type. This signal line should be pulled up to the positive side of the MCU or control power supply with a resistor that makes IFO up to 1 mA. Please refer to Figure 14.
17. Fault out pulse width can be adjusted by capacitor C6 connected to the CFOD terminal.
18. Input signal is active−HIGH type. There is a 5 kΩ resistor inside the IC to pull−down each input signal line to GND. RC coupling circuits should be adopted for the prevention of input signal oscillation. R1C1 time constant should be selected in the range 50~150 ns (recommended R1 = 100 Ω, C1 = 1 nF).
19. Each wiring pattern inductance of point A should be minimized (recommend less than 10 nH). Use the shunt resistor R3 of surface mounted (SMD) type to reduce wiring inductance. To prevent malfunction, wiring of point E should be connected to the terminal of the shunt resistor R3 as close as possible.
20. To insert the shunt resistor to measure each phase current at NU, NV, NW terminal, it makes to change the trip level ISC about the short-circuit current.
21. To prevent errors of the protection function, the wiring of points B, C, and D should be as short as possible. The wiring of B between CIN filter and RSC terminal should be divided at the point that is close to the terminal of sense resistor R4.
22. For stable protection function, use the sense resistor R4 with resistance variation within 1% and low inductance value.
23. In the short−circuit protection circuit, select the R5C5 time constant in the range 1.5~2.0 μs. R5 should be selected with a minimum of 10 times larger resistance than sense resistor R4. Do enough evaluation on the real system because short-circuit protection time may vary wiring pattern layout and value of the R5C5 time constant.
24. Each capacitor should be mounted as close to the pins of the SPM product as possible.
25. To prevent surge destruction, the wiring between the smoothing capacitor C8 and the P & GND pins should be as short as possible. The use of a high−frequency non−inductive capacitor of around 0.1~0.22 μF between the P & GND pins is recommended.
26. Relays are used in most systems of electrical equipment in industrial application. In these cases, there should be sufficient distance between the MCU and the relays.
27. The Zener diode or transient voltage suppressor should be adopted for the protection of ICs from the surge destruction between each pair of control supply terminals (recommended Zener diode is 20~22 V/1 W, which has the lower Zener impedance characteristic than about 15 Ω).
28. C2 of around seven times larger than bootstrap capacitor C3 is recommended.
29. Please choose the electrolytic capacitor with good temperature characteristic in C3. Choose 0.1~0.2 μF R−category ceramic capacitors with good temperature and frequency characteristics in C4.

**Figure 15. Typical Application Circuit**



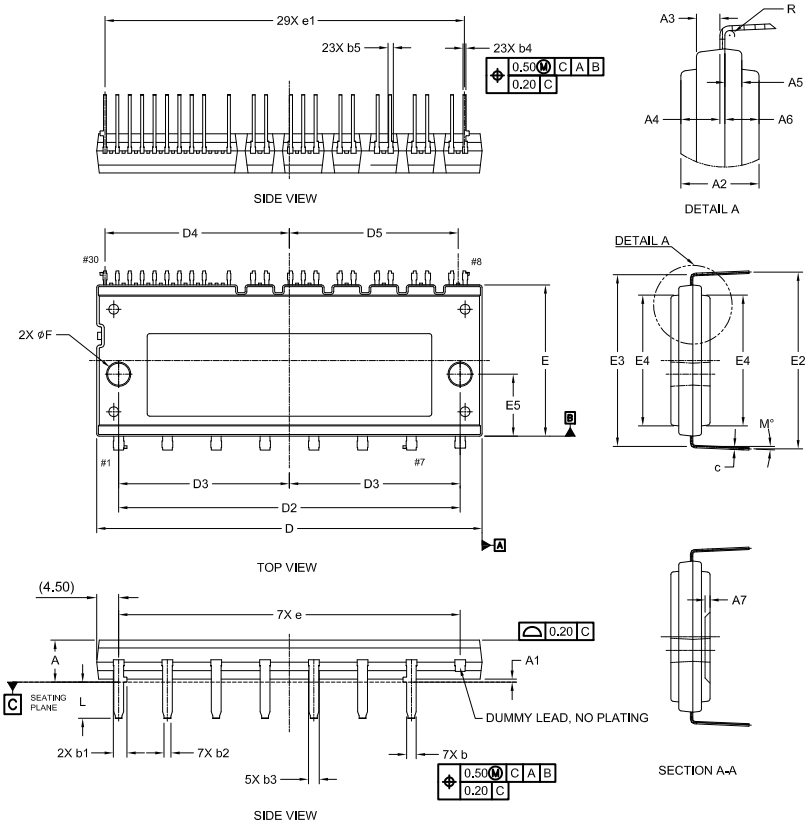
**DIP30, 79x30/SPM49 CAA**
CASE MODGR
ISSUE A

DATE 27 JUN 2019

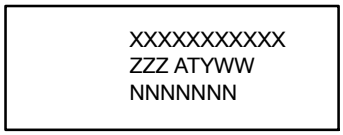
NOTES:
1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b and c APPLY TO THE PLATED LEADS AND ARE MEASURED BETWEEN 1.00 AND 2.00 FROM THE LEAD TIP.
4. POSITION OF THE LEAD IS DETERMINED AT THE ROOT OF THE LEAD WHERE IT EXITS THE PACKAGE BODY.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 8.40 | 8.60 | 8.80 |
| A1 | 0.40 | 0.60 | 0.80 |
| A2 | 7.90 | 8.00 | 8.10 |
| A3 | 2.30 | 2.40 | 2.50 |
| A4 | 3.90 | 4.00 | 4.10 |
| A5 | 1.65 | 1.75 | 1.85 |
| A6 | 3.40 | 3.50 | 3.60 |
| A7 | | 1.00 REF | |
| b | 1.90 | 2.00 | 2.10 |
| b1 | — | — | 2.80 |
| b2 | | 1.40 REF | |
| b3 | — | — | 2.20 |
| b4 | 0.50 | 0.60 | 0.70 |
| b5 | — | — | 0.80 |
| c | 0.45 | 0.50 | 0.60 |
| D | 78.80 | 79.00 | 79.20 |
| D1 | 49.50 | 49.70 | 49.90 |
| D2 | 69.85 | 70.00 | 70.15 |
| D3 | 34.80 | 35.00 | 35.20 |
| D4 | 37.60 | 37.80 | 38.00 |
| D5 | 35.66 | 35.86 | 36.06 |

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| E | 30.80 | 31.00 | 31.20 |
| E1 | 12.30 | 12.50 | 12.70 |
| E2 | 35.75 | 36.20 | 36.65 |
| E3 | | 35.17 REF | |
| E4 | 26.60 | 26.80 | 27.00 |
| E5 | 12.55 | 12.70 | 12.85 |
| E6 | 6.80 | 7.00 | 7.20 |
| e | | 10.00 BSC | |
| e1 | | 2.54 BSC | |
| F | 4.40 | 4.50 | 4.60 |
| L | | 7.40 REF | |
| M | — | — | 5.0° |
| R | | 0.50 REF | |




## GENERIC MARKING DIAGRAM*




XXXX = Specific Device Code
ZZZ = Assembly Lot Code
AT = Assembly & Test Location
Y = Year
W = Work Week
NNN = Serial Number

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
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