

# Linear Voltage Regulator - Bias Rail, Very Low Dropout, Programmable Soft-Start

3 A

## NCV59744

The NCV59744 is dual-rail very low dropout voltage regulator that is capable of providing an output current in excess of 3.0 A with a dropout voltage of 115 mV typ. at full load current. The devices are stable with ceramic and other low ESR output capacitors. This series contains adjustable output voltage version with output voltage down to 0.8 V. Internal protection features consist of built-in thermal shutdown and output current limiting protection. User-programmable Soft-Start and Power Good pins are available. The NCV59744 is available in QFN20-5x5-0.65P package.

### Features

- Output Current in Excess of 3.0 A
- 0.25% Typical Accuracy Over Line and Load
- $V_{IN}$  Range: 0.8 V to 5.5 V
- $V_{BIAS}$  Range: 2.2 V to 5.5 V
- Output Voltage Range: 0.8 V to 3.6 V
- Dropout Voltage: 115 mV at 3 A
- Programmable Soft Start
- Open Drain Power Good Output
- Excellent Transient Response
- Current Limit and Thermal Shutdown Protection
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These are Pb-Free Devices

### Applications

- Automotive, Telecom and Industrial Equipment Point of Load Regulation
- FPGA, DSP and Logic Power Supplies
- Switching Power Supply Post Regulation
- Applications with Specific Start-up Time or Sequencing Requirements

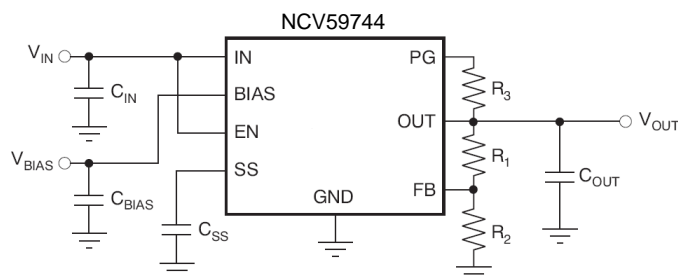
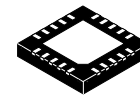
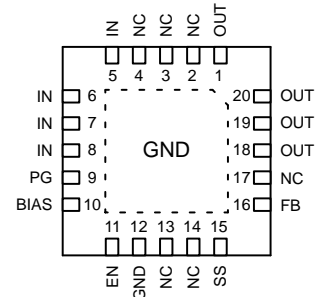


Figure 1. Typical Application Schematic



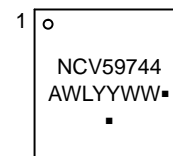
QFN20  
CASE 485DB

### PIN CONNECTIONS



QFN20, 5x5, 0.65P

### MARKING DIAGRAM



QFN20

- A = Assembly Location
  - L/WL = Wafer Lot
  - Y/YY = Year
  - W/WW = Work Week
  - = Pb-Free Package
- (Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 10 of this data sheet.

# NCV59744

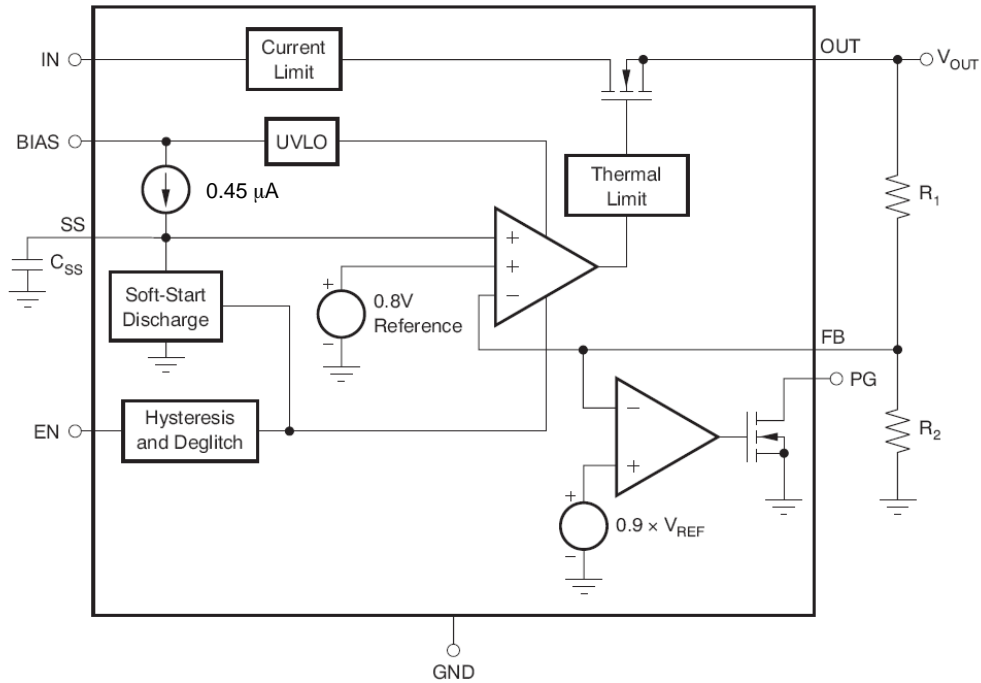


Figure 2. Simplified Schematic Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Name	QFN20	Description
IN	5–8	Unregulated input to the device.
EN	11	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. This pin must not be left floating.
SS	15	Soft–Start pin. A capacitor connected on this pin to ground sets the start–up time. If this pin is left floating, the regulator output soft–start ramp time is typically 200 $\mu$ s.
BIAS	10	Bias input voltage for error amplifier, reference, and internal control circuits.
PG	9	Power–Good (PG) is an open–drain, active–high output that indicates the status of $V_{OUT}$ . When $V_{OUT}$ exceeds the PG trip threshold, the PG pin goes into a high–impedance state. When $V_{OUT}$ is below this threshold the pin is driven to a low–impedance state. A pull–up resistor from 10 k $\Omega$ to 1 M $\Omega$ should be connected from this pin to a supply up to 5.5 V. The supply can be higher than the input voltage. Alternatively, the PG pin can be left floating if output monitoring is not necessary.
FB	16	This pin is the feedback connection to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating.
OUT	1, 18–20	Regulated output voltage. It is recommended that the output capacitor $\geq 2.2 \mu$ F.
NC	2–4, 13, 14, 17	No connection. This pin can be left floating or connected to GND to allow better thermal contact to the top–side plane.
GND	12	Ground
PAD/TAB		Should be soldered to the ground plane for increased thermal performance

**Table 2. ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Value	Unit
Input Voltage Range	$V_{IN}$	-0.3 to +6	V
Input Voltage Range	$V_{BIAS}$	-0.3 to +6	V
Enable Voltage Range	$V_{EN}$	-0.3 to +6	V
Power-Good Voltage Range	$V_{PG}$	-0.3 to +6	V
PG Sink Current	$I_{PG}$	0 to +1.5	mA
SS Pin Voltage Range	$V_{SS}$	-0.3 to +6	V
Feedback Pin Voltage Range	$V_{FB}$	-0.3 to +6	V
Output Voltage Range	$V_{OUT}$	$-0.3 \text{ to } (V_{IN} + 0.3) \leq 6$	V
Maximum Output Current	$I_{OUT}$	Internally Limited	
Output Short Circuit Duration		Indefinite	
Continuous Total Power Dissipation	$P_D$	See Thermal Characteristics Table and Formula	
Maximum Junction Temperature	$T_{JMAX}$	+150	°C
Storage Junction Temperature Range	$T_{STG}$	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:  
 ESD Human Body Model tested per AEC-Q100-002  
 ESD Machine Model tested per AEC-Q100-003  
 Latch-up Current Maximum Rating  $\leq 150$  mA per AEC-Q100-004.

**Table 3. THERMAL CHARACTERISTICS**

Rating	Symbol	Value	Unit
Thermal Characteristics, QFN20, 5x5, 0.65P package			
Thermal Resistance, Junction-to-Ambient (Note 5)	$R_{\theta JA}$	35.4	°C/W
Thermal Resistance, Junction-to-Board (Note 6)	$R_{\theta JB}$	14.7	°C/W
Thermal Resistance, Junction-to-Case (bottom) (Note 7)	$R_{\theta JC}$	3.9	°C/W

3. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
4. Thermal data are derived by thermal simulations based on methodology specified in the JEDEC JESD51 series standards. The following assumptions are used in the simulations:
  - These data were generated with only a single device at the center of a high-K (2s2p) board with 3 in x 3 in copper area which follows the JEDEC51.7 guidelines. Top and Bottom layer 2 oz. copper, inner planes 1 oz. copper.
  - The exposed pad is connected to the PCB ground inner layer through a 4x4 thermal via array. Vias are 0.3 mm diameter, plated.
  - Each of top and bottom copper layers has a dedicated pattern for 20% copper coverage.
5. The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a high-K board, following the JEDEC51.7 guidelines with assumptions as above, in an environment described in JESD51-2a.
6. The junction-to-board thermal resistance is simulated in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
7. The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the IC exposed pad. Test description can be found in the ANSI SEMI standard G30-88.

**Table 4. RECOMMENDED OPERATING CONDITIONS** (Note 8)

Rating	Symbol	Min	Max	Unit
Input Voltage	$V_{IN}$	$V_{OUT} + V_{DO}$	5.5	V
Bias Voltage	$V_{BIAS}$	2.2	5.5	V
Junction Temperature	$T_J$	-40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

8. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

**Table 5. ELECTRICAL CHARACTERISTICS**

(At  $V_{EN} = 1.1\text{ V}$ ,  $V_{IN} = V_{OUT} + 0.3\text{ V}$ ,  $C_{BIAS} = C_{IN} = 0.1\ \mu\text{F}$ ,  $C_{OUT} = 10\ \mu\text{F}$ ,  $I_{OUT} = 50\text{ mA}$ ,  $V_{BIAS} = 5.0\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_J = +25^\circ\text{C}$ .)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{IN}$	Input voltage range		$V_{OUT} + V_{DO}$		5.5	V
$V_{BIAS}$	Bias pin voltage range		2.2		5.5	V
UVLO	Undervoltage Lock-out	$V_{BIAS}$ Rising Hysteresis	1.2 –	1.6 0.4	1.9 –	V
$V_{REF}$	Internal reference (Adj.)	$T_J = +25^\circ\text{C}$	0.796	0.8	0.804	V
$V_{OUT}$	Output voltage range	$V_{IN} = 5\text{ V}$ , $I_{OUT} = 1.5\text{ A}$ , $V_{BIAS} = 5\text{ V}$	$V_{REF}$		3.6	V
	Accuracy (Note 1)	$2.97\text{ V} \leq V_{BIAS} \leq 5.25\text{ V}$ , $V_{OUT} + 1.62\text{ V} \leq V_{BIAS}$ $50\text{ mA} \leq I_{OUT} \leq 3.0\text{ A}$	–1.0	$\pm 0.25$	+1.0	%
$V_{OUT}/V_{IN}$	Line regulation	$V_{OUT(NOM)} + 0.3 \leq V_{IN} \leq 5.5\text{ V}$		0.0006		%/V
$V_{OUT}/I_{OUT}$	Load regulation	$0\text{ mA} \leq I_{OUT} \leq 50\text{ mA}$		0.005		%/mA
		$50\text{ mA} \leq I_{OUT} \leq 3.0\text{ A}$		0.01		%/A
$V_{DO}$	$V_{IN}$ dropout voltage (Note 2)	$I_{OUT} = 3.0\text{ A}$ , $V_{BIAS} - V_{OUT(NOM)} \geq 1.62\text{ V}$		115	195	mV
	$V_{BIAS}$ dropout voltage (Note 2)	$I_{OUT} = 3.0\text{ A}$ , $V_{IN} = V_{BIAS}$		1.13	1.5	V
$I_{CL}$	Current limit	$V_{OUT} = 80\% \times V_{OUT(NOM)}$	3.5	4.6	7	A
$I_{BIAS}$	Bias pin current	$0\text{ mA} \leq I_{OUT} \leq 3.0\text{ A}$		1.3	2	mA
$I_{SHDN}$	Shutdown supply current	$V_{EN} \leq 0.4\text{ V}$		1	15	$\mu\text{A}$
$I_{FB}$	Feedback pin current	$0\text{ mA} \leq I_{OUT} \leq 3.0\text{ A}$	–250	95	250	nA
PSRR	Power-supply rejection ( $V_{IN}$ to $V_{OUT}$ )	1 kHz, $I_{OUT} = 1.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$		72		dB
		1 MHz, $I_{OUT} = 1.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$		50		
	Power-supply rejection ( $V_{BIAS}$ to $V_{OUT}$ )	1 kHz, $I_{OUT} = 1.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$		80		dB
		1 MHz, $I_{OUT} = 1.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$		48		
Noise	Output noise voltage	100 Hz to 100 kHz, $I_{OUT} = 3\text{ A}$ $C_{SS} = 1.0\text{ nF}$		$18 \times V_{OUT}$		$\mu\text{Vrms}$
$V_{TRAN}$	% $V_{OUT}$ droop during load transient	$I_{OUT} = 50\text{ mA}$ to $3.0\text{ A}$ at $1\text{ A}/\mu\text{s}$ , $C_{OUT} = 10\ \mu\text{F}$ , $V_{OUT} = 3.3\text{ V}$		$\pm 1.5$		% $V_{OUT}$
$t_{STRT}$	Minimum startup time	$I_{OUT} = 1.5\text{ A}$ , $C_{SS} = \text{open}$		200		$\mu\text{s}$
$I_{SS}$	Soft-start charging current	$V_{SS} = 0.4\text{ V}$		0.45		$\mu\text{A}$
$V_{EN, HI}$	Enable input high level		1.1		5.5	V
$V_{EN, LO}$	Enable input low level		0		0.4	V
$V_{EN, HYS}$	Enable pin hysteresis			100		mV
$V_{EN, DG}$	Enable pin deglitch time			20		$\mu\text{s}$
$I_{EN}$	Enable pin current	$V_{EN} = 5\text{ V}$		0.3	1	$\mu\text{A}$
$V_{IT}$	PG trip threshold	$V_{OUT}$ decreasing	86.5	90	93.5	% $V_{OUT}$
$V_{HYS}$	PG trip hysteresis			3		% $V_{OUT}$
$V_{PG, LO}$	PG output low voltage	$I_{PG} = 1\text{ mA}$ (sinking), $V_{OUT} < V_{IT}$			0.3	V
$I_{PG, LKG}$	PG leakage current	$V_{PG} = 5.25\text{ V}$ , $V_{OUT} > V_{IT}$		0.03	1	$\mu\text{A}$
TSD	Thermal shutdown temperature	Shutdown, temperature increasing Reset, temperature decreasing		+165 +140		$^\circ\text{C}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Adjustable devices tested at 0.8 V; external resistor tolerance is not taken into account.
- Dropout is defined as the voltage from the input to  $V_{OUT}$  when  $V_{OUT}$  is 2% below nominal.

TYPICAL CHARACTERISTICS

At  $T_J = +25^\circ\text{C}$ ,  $V_{OUT} = 1.5\text{ V}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.3\text{ V}$ ,  $V_{BIAS} = 3.3\text{ V}$ ,  $I_{OUT} = 50\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  
 $C_{IN} = 1\ \mu\text{F}$ ,  $C_{BIAS} = 1\ \mu\text{F}$ ,  $C_{SS} = 0.01\ \mu\text{F}$ , and  $C_{OUT} = 10\ \mu\text{F}$ , unless otherwise noted.

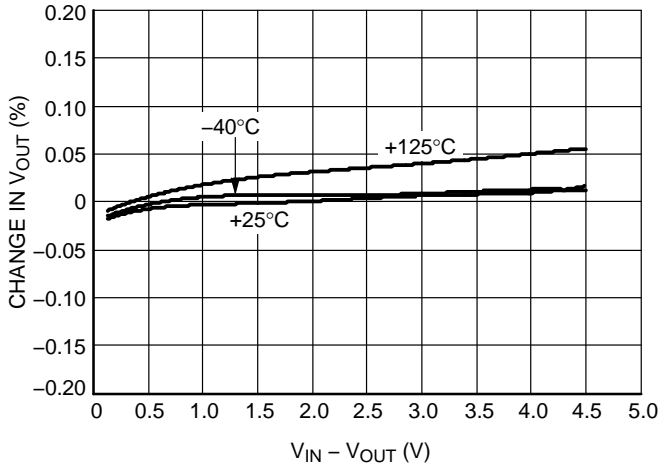


Figure 3.  $V_{IN}$  Line Regulation

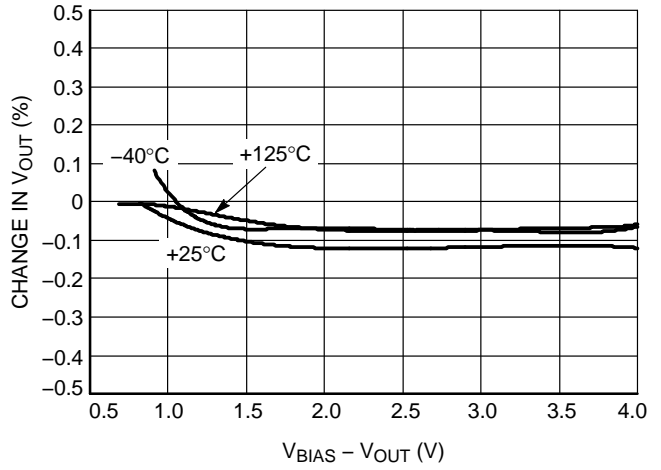


Figure 4.  $V_{BIAS}$  Line Regulation

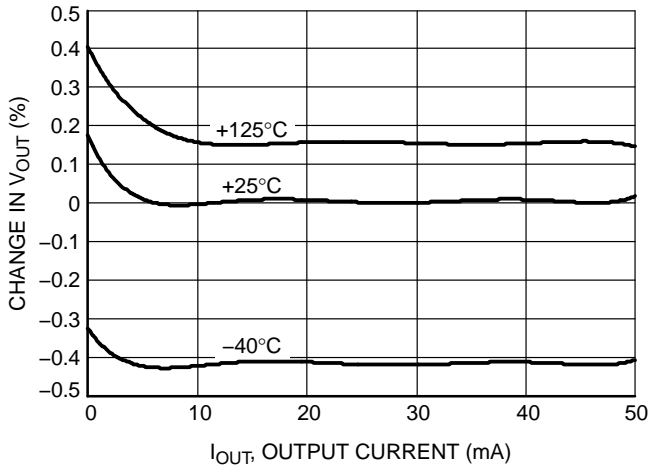


Figure 5. Load Regulation

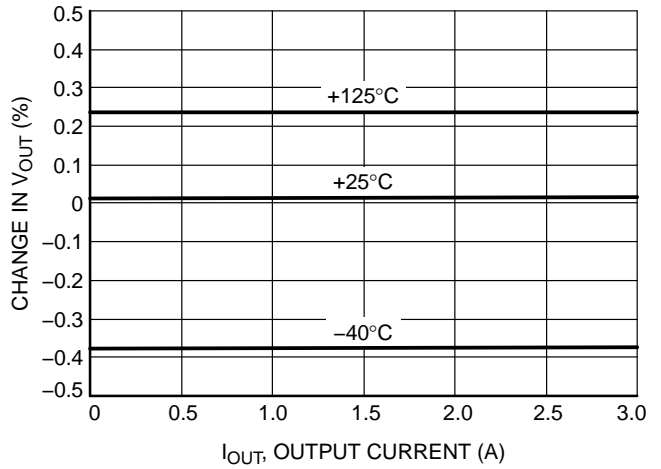


Figure 6. Load Regulation

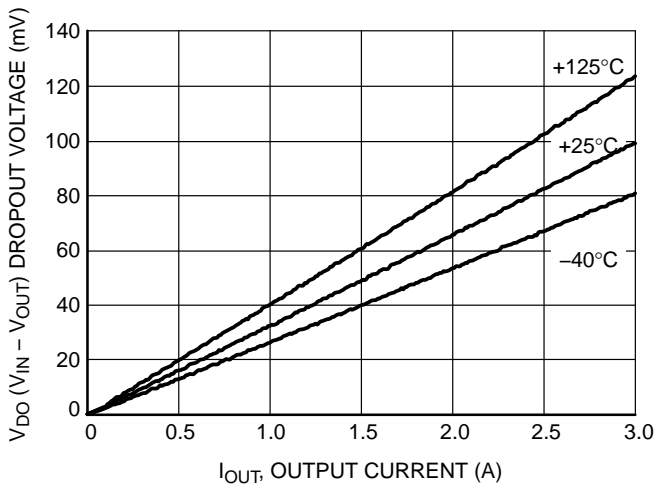


Figure 7.  $V_{IN}$  Dropout Voltage vs.  $I_{OUT}$  and Temperature  $T_J$

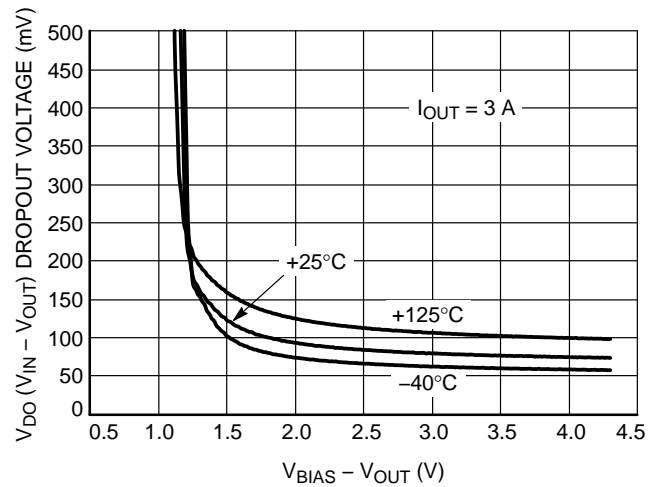


Figure 8.  $V_{IN}$  Dropout Voltage vs.  $(V_{BIAS} - V_{OUT})$  and Temperature  $T_J$

TYPICAL CHARACTERISTICS

At  $T_J = +25^\circ\text{C}$ ,  $V_{OUT} = 1.5\text{ V}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.3\text{ V}$ ,  $V_{BIAS} = 3.3\text{ V}$ ,  $I_{OUT} = 50\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{IN} = 1\ \mu\text{F}$ ,  $C_{BIAS} = 1\ \mu\text{F}$ ,  $C_{SS} = 0.01\ \mu\text{F}$ , and  $C_{OUT} = 10\ \mu\text{F}$ , unless otherwise noted.

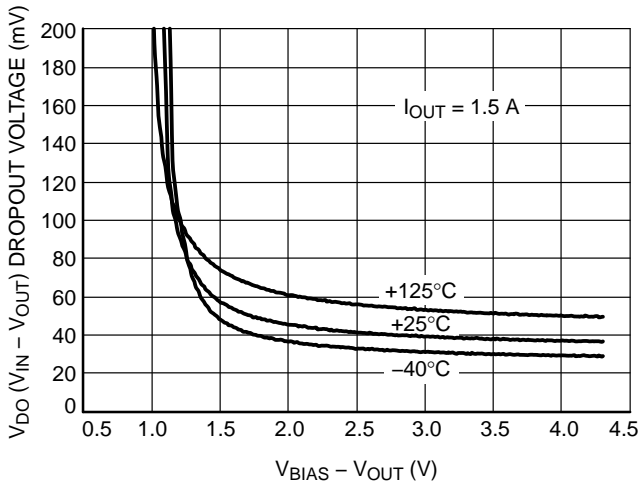


Figure 9.  $V_{IN}$  Dropout Voltage vs.  $(V_{BIAS} - V_{OUT})$  and Temperature  $T_J$

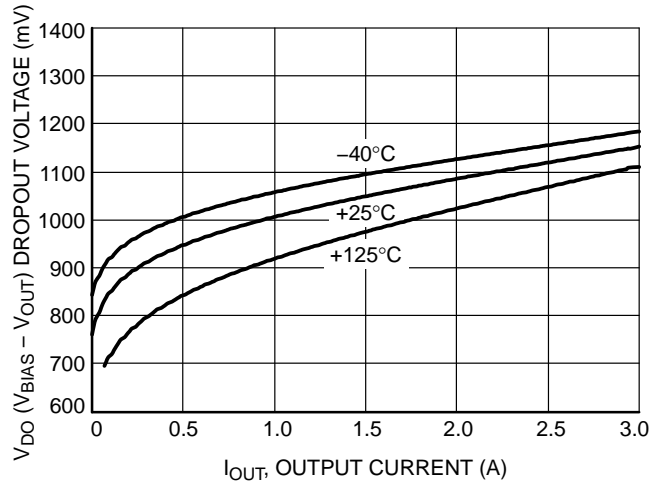


Figure 10.  $V_{BIAS}$  Dropout Voltage vs.  $I_{OUT}$  and Temperature  $T_J$

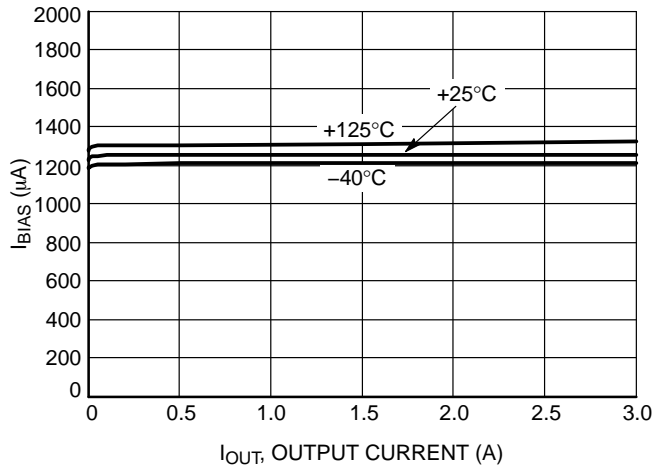


Figure 11. BIAS Pin Current vs.  $I_{OUT}$  and Temperature  $T_J$

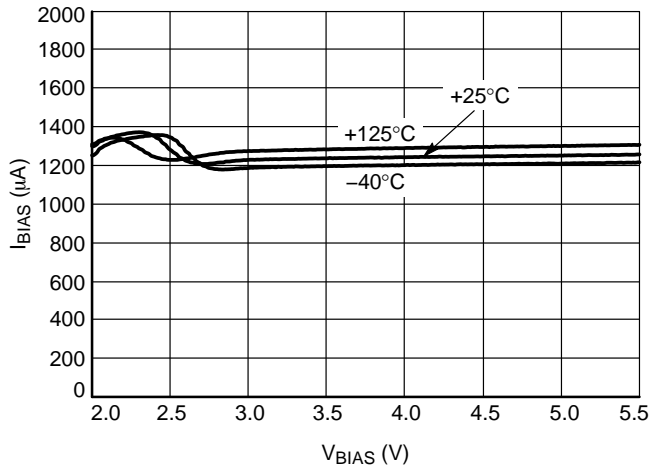


Figure 12. BIAS Pin Current vs.  $V_{BIAS}$  and Temperature  $T_J$

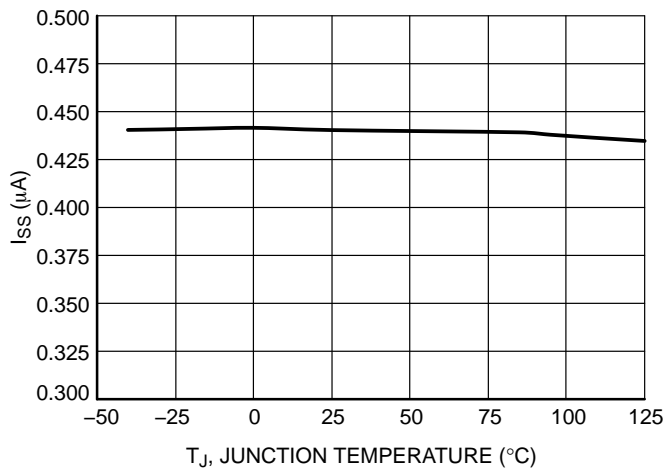


Figure 13. Soft Start Charging Current  $I_{SS}$  vs. Temperature  $T_J$

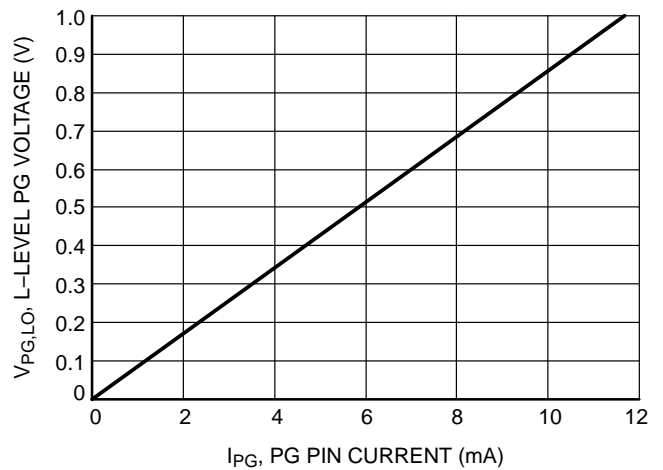


Figure 14. L-level PG Voltage vs. Current

TYPICAL CHARACTERISTICS

At  $T_J = +25^\circ\text{C}$ ,  $V_{OUT} = 1.5\text{ V}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.3\text{ V}$ ,  $V_{BIAS} = 3.3\text{ V}$ ,  $I_{OUT} = 50\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{IN} = 1\ \mu\text{F}$ ,  $C_{BIAS} = 1\ \mu\text{F}$ ,  $C_{SS} = 0.01\ \mu\text{F}$ , and  $C_{OUT} = 10\ \mu\text{F}$ , unless otherwise noted.

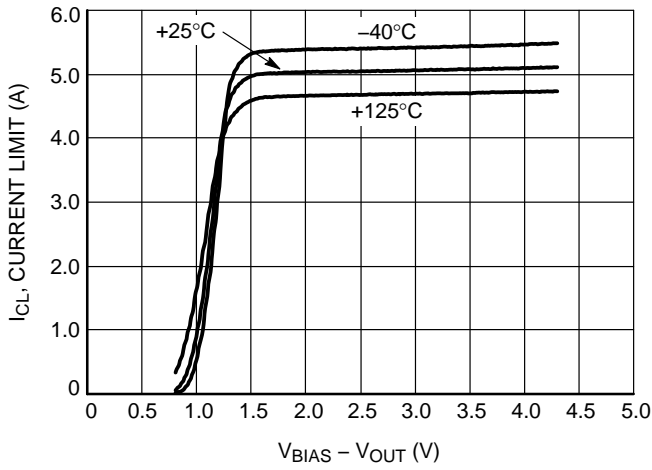


Figure 15. Current Limit vs. ( $V_{BIAS} - V_{OUT}$ )

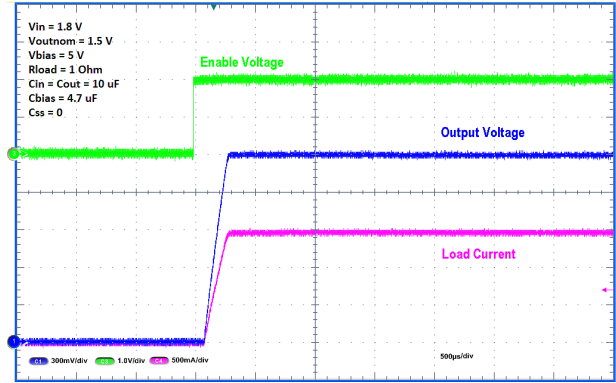


Figure 16. Start by Enable at  $C_{SS} = 0$

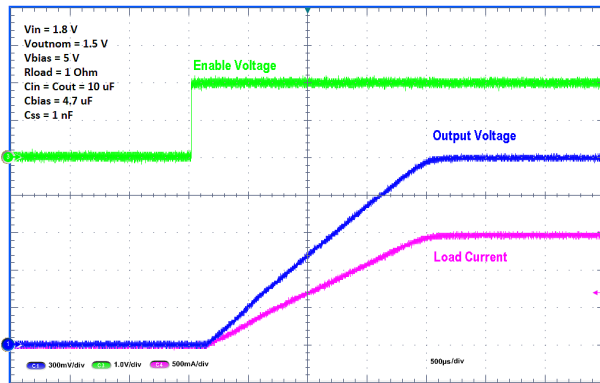


Figure 17. Start by Enable at  $C_{SS} = 1\text{ nF}$

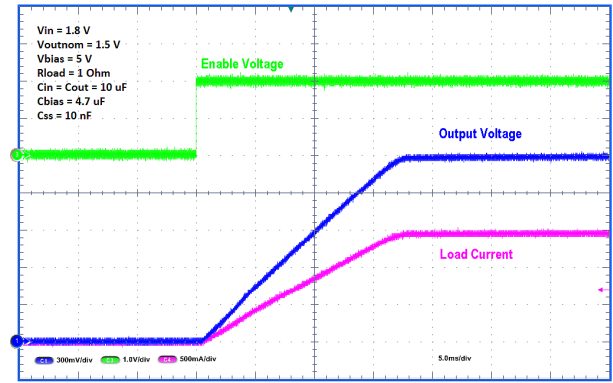


Figure 18. Start by Enable at  $C_{SS} = 10\text{ nF}$

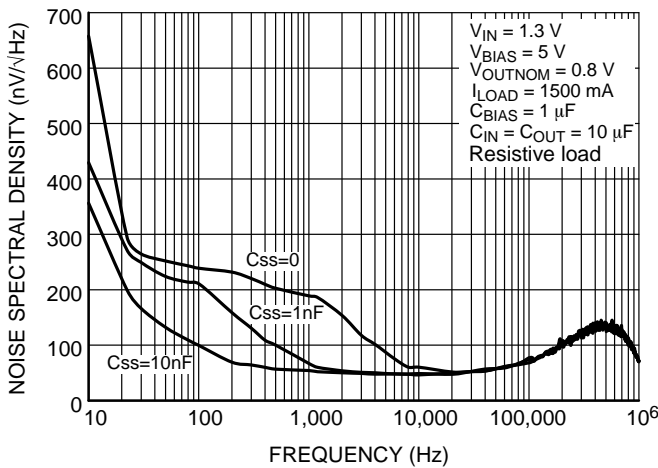


Figure 19. Output Voltage Noise Spectral Density at  $V_{OUT} = 0.8\text{ V}$

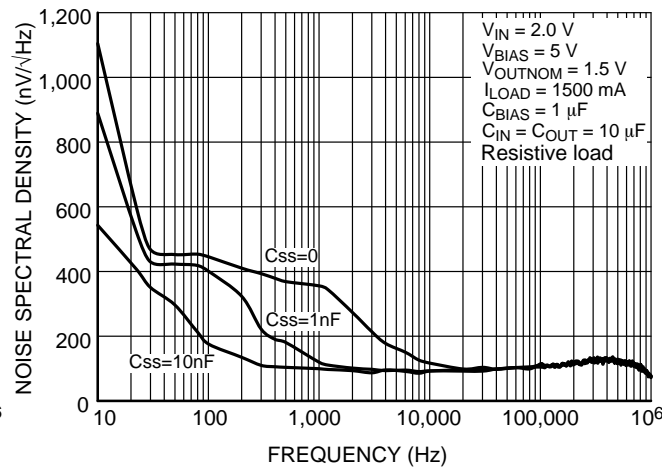


Figure 20. Output Voltage Noise Spectral Density at  $V_{OUT} = 1.5\text{ V}$

TYPICAL CHARACTERISTICS

At  $T_J = +25^\circ\text{C}$ ,  $V_{OUT} = 1.5\text{ V}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.3\text{ V}$ ,  $V_{BIAS} = 3.3\text{ V}$ ,  $I_{OUT} = 50\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  
 $C_{IN} = 1\ \mu\text{F}$ ,  $C_{BIAS} = 1\ \mu\text{F}$ ,  $C_{SS} = 0.01\ \mu\text{F}$ , and  $C_{OUT} = 10\ \mu\text{F}$ , unless otherwise noted.

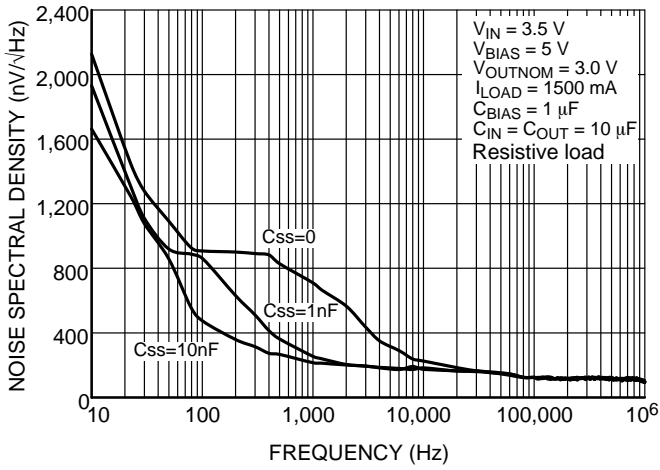


Figure 21. Output Voltage Noise Spectral Density at  $V_{OUT} = 3.0\text{ V}$

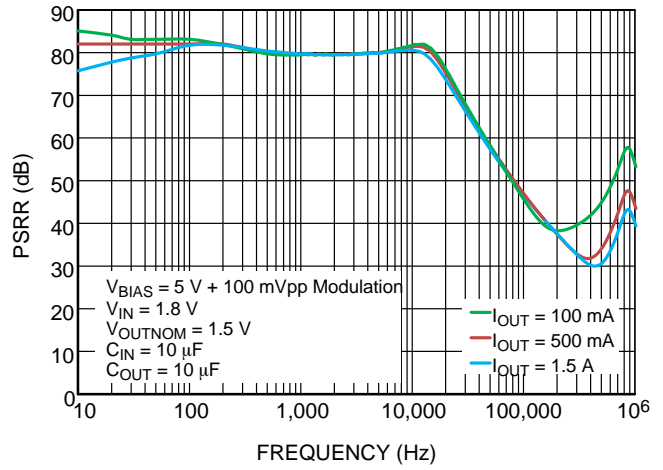


Figure 22.  $V_{BIAS}$  PSRR

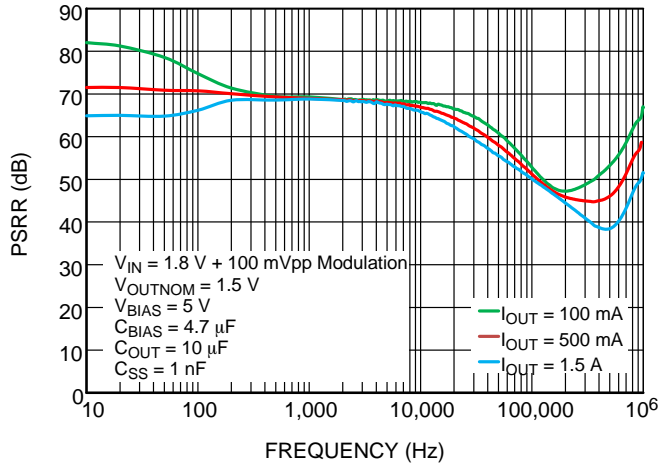


Figure 23.  $V_{IN}$  PSRR



APPLICATIONS INFORMATION

The NCV59744 dual-rail very low dropout voltage regulator is using NMOS pass transistor for output voltage regulation from  $V_{IN}$  voltage. All the low current internal control circuitry is powered from the  $V_{BIAS}$  voltage.

The use of an NMOS pass transistor offers several advantages in applications. Unlike a PMOS topology devices, the output capacitor has reduced impact on loop stability.  $V_{in}$  to  $V_{out}$  operating voltage difference can be very low compared with standard PMOS regulators in very low  $V_{in}$  applications.

The NCV59744 offers programmable smooth monotonic start-up. The controlled voltage rising limits the inrush current what is advantageous in applications with large capacitive loads. The Voltage Controlled Soft Start timing is programmable by external  $C_{SS}$  capacitor value.

The Enable (EN) input is equipped with internal hysteresis and deglitch filter.

Open Drain type Power Good (PG) output is available for  $V_{out}$  monitoring and sequencing of other devices.

NCV59744 is a Adjustable linear regulator. The required Output voltage can be adjusted by two external resistors. Typical application schematics is shown in Figure 24.

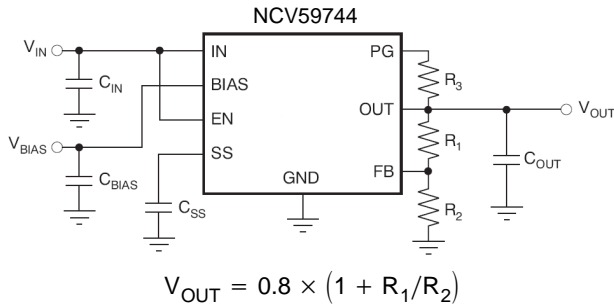


Figure 24. Typical Application Schematics

**Dropout Voltage**

Because of two power supply inputs  $V_{IN}$  and  $V_{BIAS}$  and one  $V_{OUT}$  regulator output, there are two Dropout voltages specified.

The first, the  $V_{IN}$  Dropout voltage is the voltage difference ( $V_{IN} - V_{OUT}$ ) when  $V_{OUT}$  starts to decrease by percents specified in the Electrical Characteristics table.  $V_{BIAS}$  is high enough, specific value is published in the Electrical Characteristics table.

The second,  $V_{BIAS}$  dropout voltage is the voltage difference ( $V_{BIAS} - V_{OUT}$ ) when  $V_{IN}$  and  $V_{BIAS}$  pins are joined together and  $V_{OUT}$  starts to decrease.

**Input and Output Capacitors**

The device is designed to be stable for all available types and values of output capacitors  $\geq 2.2 \mu F$ . The device is also stable with multiple capacitors in parallel, which can be of any type or value.

In applications where no low input supply impedance is available (PCB inductance in  $V_{in}$  and/or  $V_{bias}$  inputs as an

example) the recommended  $C_{in}$  and  $C_{bias}$  value is  $1 \mu F$  or greater. Ceramic or other low ESR capacitors are recommended. For the best performance all capacitors should be connected to the NCV59744 respective pins directly in the device PCB copper layer, not through vias having not negligible impedance.

**Enable Operation**

The enable pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this data sheet. If the enable function is not to be used then the pin should be connected to  $V_{IN}$  or  $V_{BIAS}$ .

**Output Noise**

When the NCV59744 device reaches the end of the Soft-Start cycle, the Soft Start capacitor is switched to serve as a Noise filtering capacitor.

**Output Voltage Adjust**

The output voltage can be adjusted from 0.8 V to 3.6 V using resistors divider between the output and the FB input. Recommended resistor values for frequently used voltages can be found in the Table 6.

**Programmable Soft-Start**

The Soft-Start ramp time depends on the Soft Start charging current  $I_{SS}$ , Soft-Start capacitor value  $C_{SS}$  and internal reference voltage  $V_{REF}$ .

The Soft -Start time can be calculated using following equations:

$$t_{ss} = C_{SS} \times (V_{REF} / I_{SS}) [s, F, V, A]$$

or in more practical units

$$t_{ss} = C_{SS} \times 0.8V / 0.45 = C_{SS} \times 1.78$$

where

$t_{ss}$  = Soft-Start time in milliseconds

$C_{SS}$  = Soft-Start capacitor value in nano Farads

Capacitor values for frequently used Soft-Start times can be found in the Table 7.

The maximal recommended value of  $C_{SS}$  capacitor is 15 nF. For higher  $C_{SS}$  values the capacitor full discharging before new Soft-Start cycle is not guaranteed.

**Current Limitation**

The internal Current Limitation circuitry allows the device to supply the full nominal current and surges but protects the device against Current Overload or Short.

**Thermal Protection**

Internal thermal shutdown (TSD) circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When TSD activated, the regulator output turns off. When cooling down under the low temperature threshold, device output is activated again. This TSD feature is provided to prevent failures from accidental overheating.

**Power Dissipation**

The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. For reliable operation junction temperature should be limited to +125°C.

**Table 6. RESISTOR VALUES FOR PROGRAMMING THE OUTPUT VOLTAGE**

V <sub>OUT</sub> (V)	R <sub>1</sub> (kΩ)	R <sub>2</sub> (kΩ)
0.8	Short	Open
0.9	0.619	4.99
1.0	1.13	4.53
1.05	1.37	4.33
1.1	1.87	4.99
1.2	2.49	4.99
1.5	4.12	4.75
1.8	3.57	2.87
2.5	3.57	1.69
3.3	3.57	1.15

NOTE:  $V_{OUT} = 0.8 \times (1 + R_1/R_2)$   
Resistors in the table are standard 1% types

**Table 7. CAPACITOR VALUES FOR PROGRAMMING THE SOFT-START TIME**

Soft-Start Time	C <sub>SS</sub>
0.2 ms	Open
0.5 ms	270 pF
1 ms	560 pF
5 ms	2.7 nF
10 ms	5.6 nF
18 ms	10 nF

**Table 8. ORDERING INFORMATION**

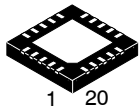
Device	Output Current	Output Voltage	Junction Temp. Range	Package	Shipping†
NCV59744MNADJTBG	3.0 A	ADJ	-40°C to +125°C	QFN20 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

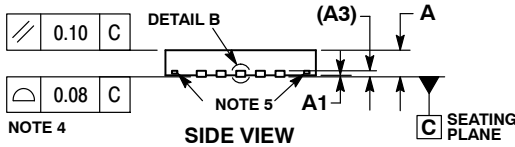
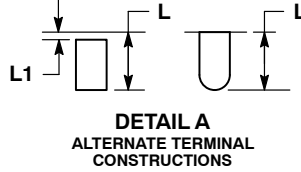
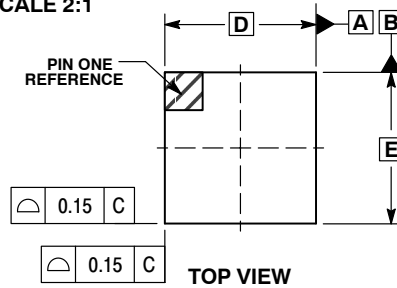
ON Semiconductor®



**QFN20 5x5, 0.65P**  
CASE 485DB  
ISSUE O

DATE 02 APR 2013

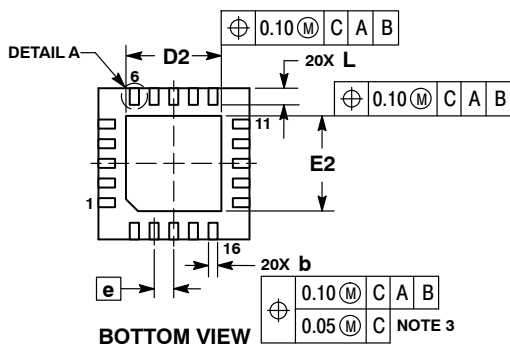
SCALE 2:1



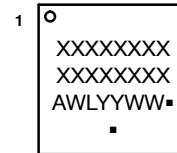
**NOTES:**

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. OPTIONAL FEATURES.

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	----	0.05
A3	0.20	REF
b	0.25	0.35
D	5.00	BSC
D2	3.05	3.25
E	5.00	BSC
E2	3.05	3.25
e	0.65	BSC
L	0.45	0.65
L1	----	0.15



**GENERIC MARKING DIAGRAM\***

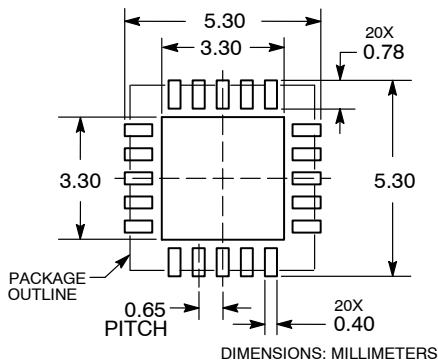


- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking.  
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

**RECOMMENDED SOLDERING FOOTPRINT\***



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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<b>DESCRIPTION:</b>	<b>QFN20 5x5, 0.65P</b>	<b>PAGE 1 OF 1</b>

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