NCP5351

4 A Synchronous Buck Power MOSFET Driver

The NCP5351 is a dual MOSFET gate driver optimized to drive the gates of both high−side and low−side Power MOSFETs in a Synchronous Buck converter. The NCP5351 is an excellent companion to multiphase controllers that do not have integrated gate drivers, such as ON Semiconductor's CS5323, CS5305 or CS5307. This architecture provides a power supply designer the flexibility to locate the gate drivers close to the MOSFETs.

The 4.0 A drive capability makes the NCP5351 ideal for minimizing switching losses in MOSFETs with large input capacitance. Optimized internal, adaptive nonoverlap circuitry further reduces switching losses by preventing simultaneous conduction of both MOSFETs.

The floating top driver design can accommodate MOSFET drain voltages as high as 25 V. Both gate outputs can be driven low, and supply current reduced to less than 25 μA, by applying a low logic level to the Enable (EN) pin. An undervoltage lockout function ensures that both driver outputs are low when the supply voltage is low, and a thermal shutdown function provides the IC with overtemperature protection.

The NCP5351 is pin−to−pin compatible with the SC1205 and is available in a standard SO−8 package and thermally enhanced DFN10.

Features

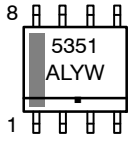
- 4.0 A Peak Drive Current
- Rise and Fall Times < 15 ns Typical into 6000 pF
- Propagation Delay from Inputs to Outputs < 20 ns
- Adaptive Nonoverlap Time Optimized for Large Power MOSFETs
- Floating Top Driver Accommodates Applications Up to 25 V
- Undervoltage Lockout to Prevent Switching when the Input Voltage is Low
- Thermal Shutdown Protection Against Overtemperature
- < 1.0 mA Quiescent Current − Enabled
- 25 μA Quiescent Current − Disabled
- Internal TG to DRN Pulldown Resistor Prevents HV Supply−Induced Turn On of High−Side MOSFET
- Pb−Free Package is Available

ON Semiconductor®

http://onsemi.com

MARKING DIAGRAMS

SO−8
D SUFFIX
CASE 751



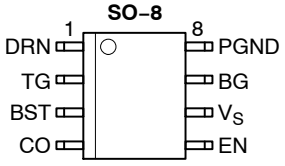
DFN10
MN SUFFIX
CASE 485C

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

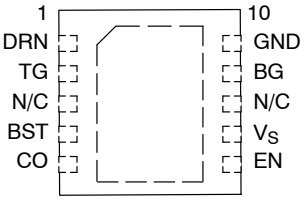
(Note: Microdot may be in either location)

PIN CONNECTIONS

SO−8



DFN10



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

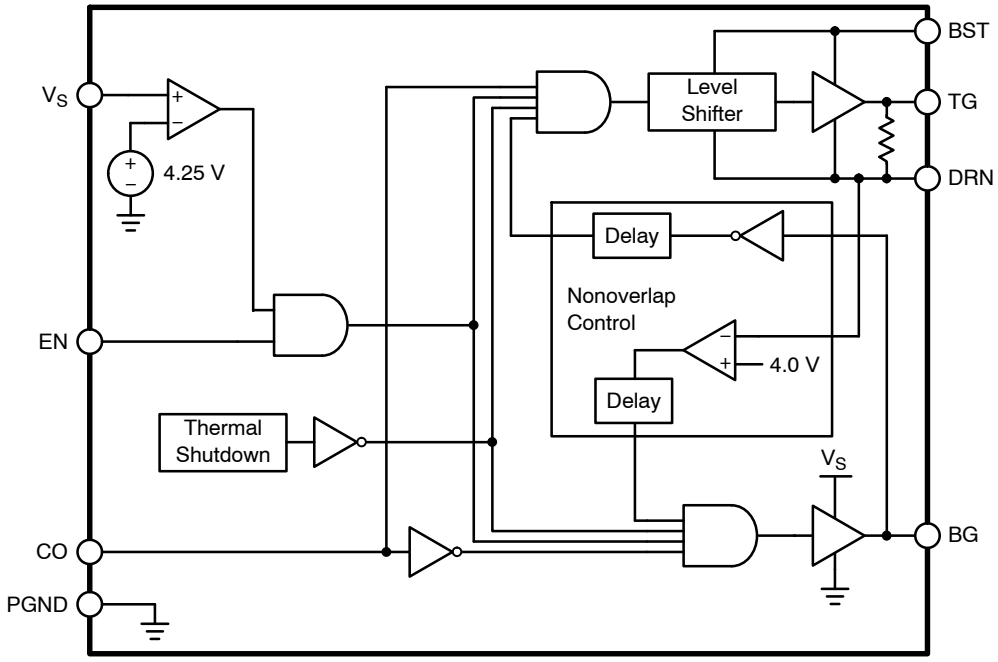


Figure 1. Block Diagram

Table 1. Input–Output Truth Table

EN	CO	DRN	TG	BG
L	X	X	L	L
H	L	< 3.0 V	L	H
H	H	< 3.0 V	H	L
H	L	> 5.0 V	L	L
H	H	> 5.0 V	H	L

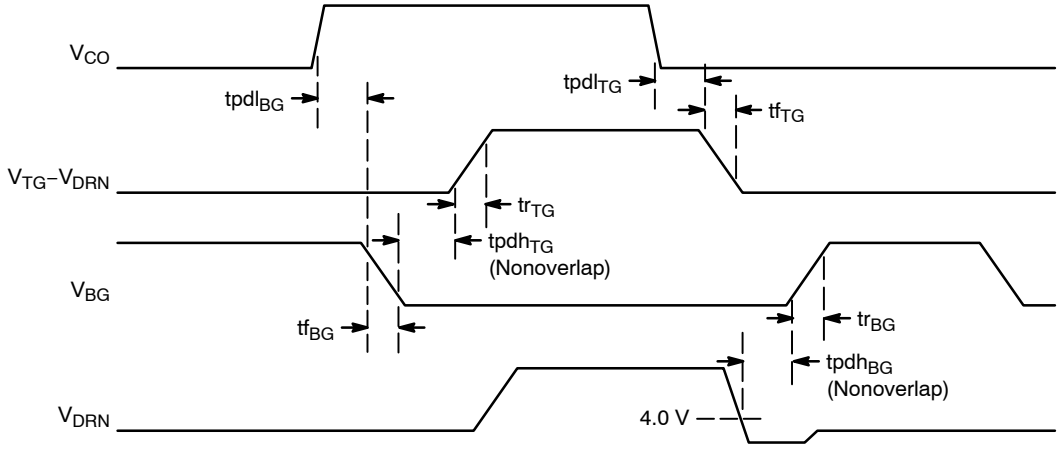


Figure 2. Timing Diagram

PACKAGE PIN DESCRIPTION

Pin Number		Pin Symbol	Description
SO−8	DFN−10		
1	1	DRN	The switching node common to the high and low−side FETs. The high−side (TG) driver and supply (BST) are referenced to this pin.
2	2	TG	Driver output to the high−side MOSFET gate.
3	4	BST	Bootstrap supply voltage input. In conjunction with a Schottky diode to V_S, a 0.1 μF to 1.0 μF ceramic capacitor connected between BST and DRN develops supply voltage for the high−side driver (TG).
4	5	CO	Logic level control input produces complementary output states − no inversion at TG; inversion at BG.
−	3, 8	N/C	Not Connected.
5	6	EN	Logic level enable input forces TG and BG low, and supply current to 10 μA when EN is low.
6	7	V_S	Power supply input. A 0.1 μF to 1.0 μF ceramic capacitor should be connected from this pin to PGND.
7	9	BG	Driver output to the low−side (synchronous rectifier) MOSFET gate.
8	−	PGND	Ground.
−	10	GND	Ground.

MAXIMUM RATINGS – SO–8

Rating	Value	Unit
Operating Junction Temperature, T_J	Internally Limited	°C
Package Thermal Resistance: SO–8 Junction–to–Case, $R_{\theta JC}$ Junction–to–Ambient, $R_{\theta JA}$	 45 165	 °C/W °C/W
Storage Temperature Range, T_S	–65 to 150	°C
Lead Temperature Soldering: Reflow: (SMD styles only) (Note 1) Pb–Free	230 peak 260 peak	°C
MSL Rating	1	–

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

1. 60 seconds maximum above 183°C.

MAXIMUM RATINGS – DFN–10

Rating	Symbol	Value	Unit
Thermal Resistance, Junction–to–Air	R_{JA}	68.5	°C/W
Operating Ambient Temperature Range	T_A	–30 to 85	°C
ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 2)	V_{ESD}	> 2500 > 150	V
Moisture Sensitivity	MSL	Level 1	
Storage Temperature Range	T_{stg}	–55 to 150	°C
Junction Operating Temperature	T_J	–30 to 125	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. This device series contains ESD protection and exceeds the following tests:
   Human Body Model, 100 pF discharge through a 1.5 kΩ following specification JESD22/A114.
   Machine Model, 200 pF discharged through all pins following specification JESD22/A115.
   Latchup as per JESD78 Class II: > 100 mA.

MAXIMUM RATINGS

Pin Symbol	Pin Name	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
V_S	Main Supply Voltage Input	6.3 V	–0.3 V	NA	4.0 A Peak (< 100 μs) 250 mA DC
BST	Bootstrap Supply Voltage Input	25 V wrt/PGND 6.3 V wrt/DRN	–0.3 V wrt/DRN	NA	4.0 A Peak (< 100 μs) 250 mA DC
DRN	Switching Node (Bootstrap Supply Return)	25 V	–1.0 V DC –5.0 V for 100 ns –6.0 V for 20 ns	4.0 A Peak (< 100 μs) 250 mA DC	NA
TG	High–Side Driver Output (Top Gate)	25 V wrt/PGND 6.3 V wrt/DRN	–0.3 V wrt/DRN	4.0 A Peak (< 100 μs) 250 mA DC	4.0 A Peak (< 100 μs) 250 mA DC
BG	Low–Side Driver Output (Bottom Gate)	6.3 V	–0.3 V	4.0 A Peak (< 100 μs) 250 mA DC	4.0 A Peak (< 100 μs) 250 mA DC
CO	TG & BG Control Input	6.3 V	–0.3 V	1.0 mA	1.0 mA
EN	Enable Input	6.3 V	–0.3 V	1.0 mA	1.0 mA
PGND	Ground	0 V	0 V	4.0 A Peak (< 100 μs) 250 mA DC	NA

NOTE: All voltages are with respect to PGND except where noted.

ELECTRICAL CHARACTERISTICS ($0°C < T_J < 125°C$; $V_S = 5.0$ V; 4.0 V $< V_{BST} < 25$ V; $V_{EN} = V_S$; unless otherwise noted)

Parameter	Test Conditions	Min	Typ	Max	Unit
DC OPERATING SPECIFICATIONS POWER SUPPLY					
V_S Quiescent Current, Operating	V_{CO} = 0 V, 4.5 V; No output switching	–	1.0	–	mA
V_{BST} Quiescent Current, Operating	V_{CO} = 0 V, 4.5 V; No output switching	–	50	–	μA
Quiescent Current, Non−Operating	V_{EN} = 0 V; V_{CO} = 0 V, 4.5 V	–	–	25	μA
Undervoltage Lockout					
Start Threshold	CO = 0 V	4.05	4.25	4.48	V
Hysteresis	CO = 0 V	–	275	–	mV
CO INPUT CHARACTERISTICS					
High Threshold	–	2.0	–	–	V
Low Threshold	–	–	–	0.8	V
Input Bias Current	$0 < V_{CO} < V_S$	–	0	1.0	μA
EN INPUT CHARACTERISTICS					
High Threshold	Both outputs respond to CO	2.0	–	–	V
Low Threshold	Both outputs are low, independent of CO	–	–	0.8	V
Input Bias Current	$0 < V_{EN} < V_S$	–	0	10	μA
THERMAL SHUTDOWN					
Overtemperature Trip Point	–	–	170	–	°C
Hysteresis	–	–	30	–	°C
HIGH−SIDE DRIVER					
Peak Output Current	–	–	4.0	–	A
Output Resistance (Sourcing)	Duty Cycle < 2.0%, Pulse Width < 100 μs, T_J = 125°C, $V_{BST} - V_{DRN}$ = 4.5 V, V_{TG} = 4.0 V + V_{DRN}	–	0.5	–	Ω
Output Resistance (Sinking)	Duty Cycle < 2.0%, Pulse Width < 100 μs, T_J = 125°C, $V_{BST} - V_{DRN}$ = 4.5 V, V_{TG} = 0.5 V + V_{DRN}	–	0.42	–	Ω
LOW−SIDE DRIVER					
Peak Output Current	–	–	4.0	–	A
Output Resistance (Sourcing)	Duty Cycle < 2.0%, Pulse Width < 100 μs, T_J = 125°C, V_S = 4.5 V, V_{BG} = 4.0 V	–	0.6	–	Ω
Output Resistance (Sinking)	Duty Cycle < 2.0%, Pulse Width < 100 μs, T_J = 125°C, V_S = 4.5 V, V_{BG} = 0.5 V	–	0.42	–	Ω

ELECTRICAL CHARACTERISTICS (continued) ($0°C < T_J < 125°C$; $V_S = 5.0$ V; 4.0 V $< V_{BST} < 25$ V; $V_{EN} = V_S$, $C_{LOAD} = 5.7$ nF; unless otherwise noted.)

Parameter	Test Conditions	Min	Typ	Max	Unit
AC OPERATING SPECIFICATIONS HIGH−SIDE DRIVER					
Rise Time	$V_{BST} - V_{DRN} = 5.0$ V, $T_J = 125°C$	–	8.0	16	ns
Fall Time	$V_{BST} - V_{DRN} = 5.0$ V, $T_J = 125°C$	–	14	21	ns
Propagation Delay Time, TG Going High (Nonoverlap Time)	$V_{BST} - V_{DRN} = 5.0$ V, $T_J = 125°C$	30	45	60	ns
Propagation Delay Time, TG Going Low	$V_{BST} - V_{DRN} = 5.0$ V, $T_J = 125°C$	–	18	37	ns
LOW−SIDE DRIVER					
Rise Time	$T_J = 125°C$	–	10	15	ns
Fall Time	$T_J = 125°C$	–	12	20	ns
Propagation Delay Time, BG Going High (Non−Overlap Time)	$T_J = 125°C$	25	55	80	ns
Propagation Delay Time, BG Going Low	$T_J = 125°C$	–	10	18	ns
UNDERVOLTAGE LOCKOUT					
V_S Rising	EN = V_S, CO = 0 V, $dV_S/dt > 1.0$ V/μs, from 4.0 V to 4.5 V, time to BG > 1.0 V, $T_J = 125°C$	–	30	–	μs
V_S Falling	EN = V_S, CO = 0 V, $dV_S/dt < -1.0$ V/μs, from 4.5 V to 4.0 V, time to BG < 1.0 V, $T_J = 125°C$	–	500	–	μs

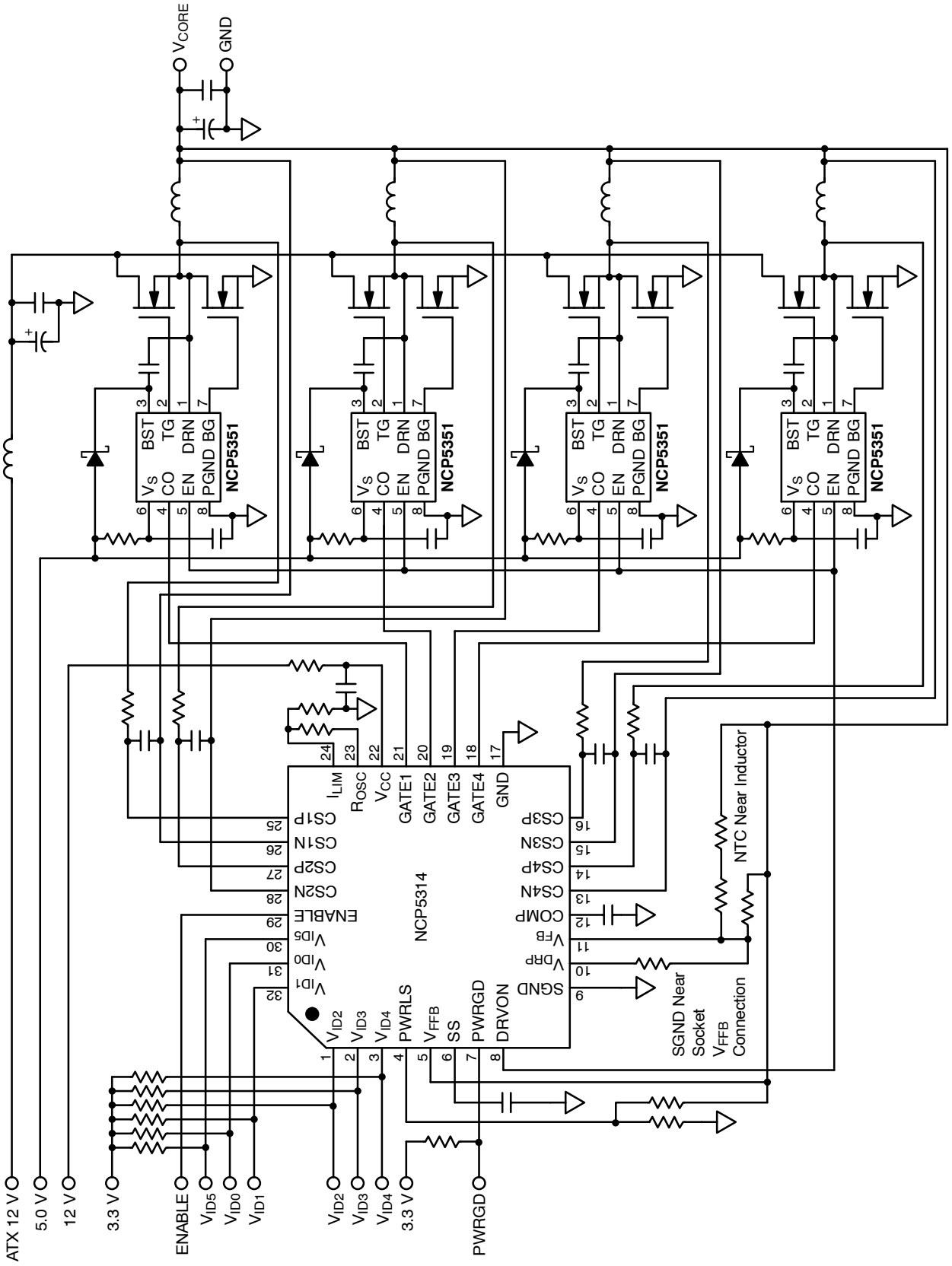


Figure 3. Application Diagram

APPLICATIONS INFORMATION

Theory Of Operation

Enable Pin

The Enable Pin (EN) is controlled by a logic level input. With a logic level high on the EN pin, the output states of the drivers are controlled by applying a logic level voltage to the CO pin. With a logic level low both gates are forced low. By bringing both gates low when disabling, the output voltage is prevented from ringing below ground, which could potentially cause damage to the microprocessor or the device being powered.

Undervoltage Lockout

The TG and BG are held low until V_S reaches 4.25 V during startup. The CO pin takes control of the gates' states when the V_S threshold is exceeded. If V_S decreases 300 mV below threshold, the output gate will be forced low and remain low until V_S rises above startup threshold.

Adaptive Nonoverlap

The Adaptive Nonoverlap prevents a condition where the top and bottom MOSFETs conduct at the same time and short the input supply. When the top MOSFET is turning off, the drain (switch node) is sampled and the BG is disabled for a fixed delay time ($tpdh_{BG}$) after the drain drops below 4 V, thus eliminating the possibility of shoot−through. When the bottom MOSFET is turning off, TG is disabled for a fixed delay ($tpdh_{TG}$) after BG drops below 2.0 V. (See Figure 2 for complete timing information).

Layout Guidelines

When designing any switching regulator, the layout is very important for proper operation. The designer should follow some simple layout guidelines when incorporating gate drivers in their designs. Gate drives experience high di/dt during switching and the inductance of gate drive traces should be minimized. Gate drive traces should be kept as short and wide as practical and should have a return path directly below the gate trace. The use of a ground plane is a desirable way to return ground signals. Also, component location will make a difference. The boost and the V_S capacitor are the most critical and should be placed as close as possible to the driver IC pins, as shown in Figure 4(a), C21 and C17.

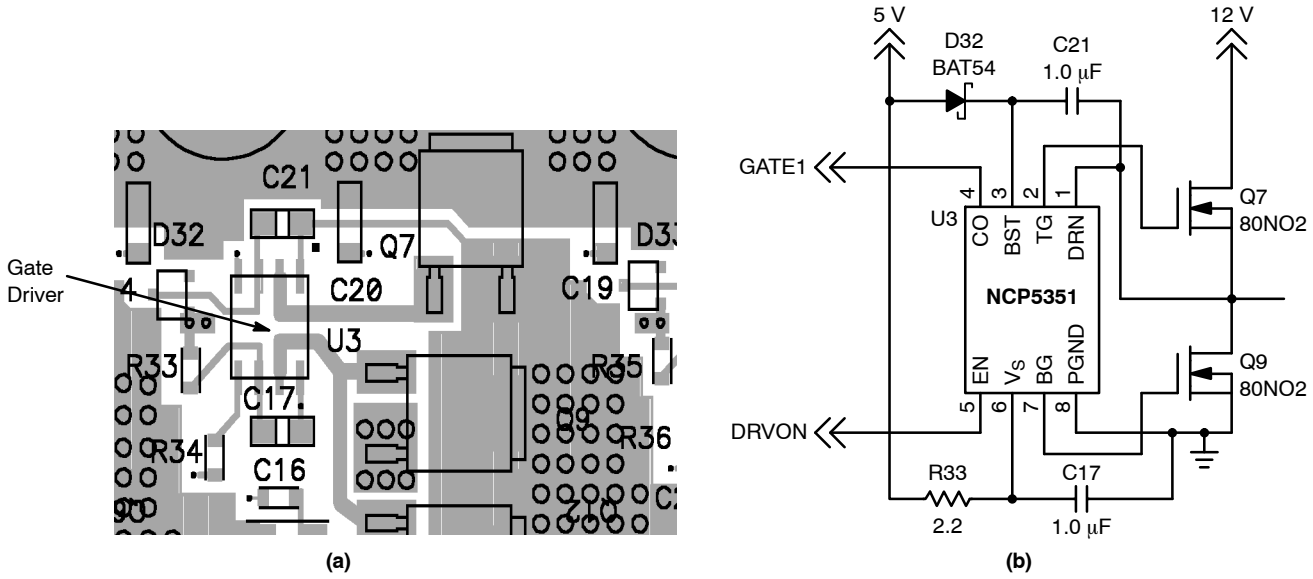
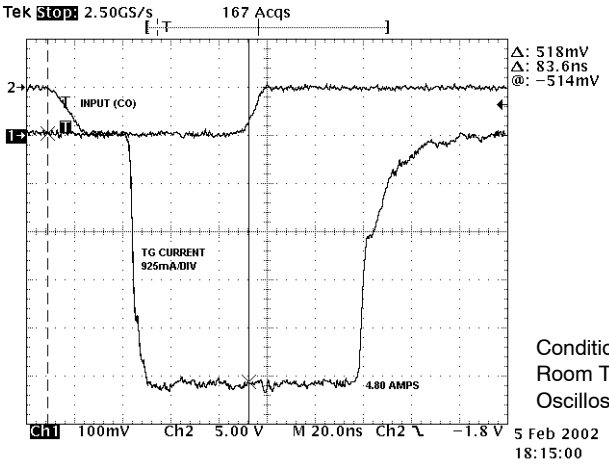
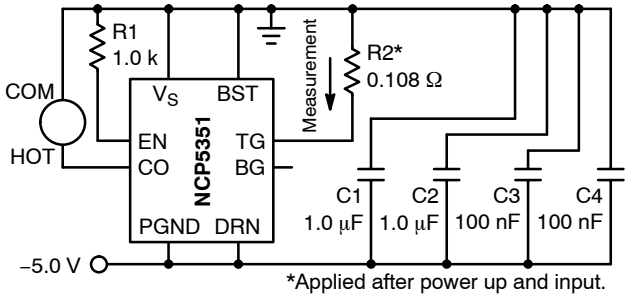


Figure 4. Proper Layout (a), Component Selection (b)

TYPICAL PERFORMANCE CHARACTERISTICS





Conditions: BST − DRN = 5.0 V;
Room Temperature;
Oscilloscope referenced to V_S (5.0 V).

Figure 5. Top Gate Sinking Current from 0.108 Ω

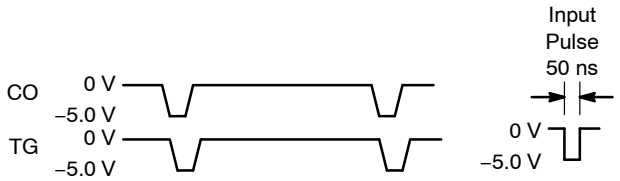
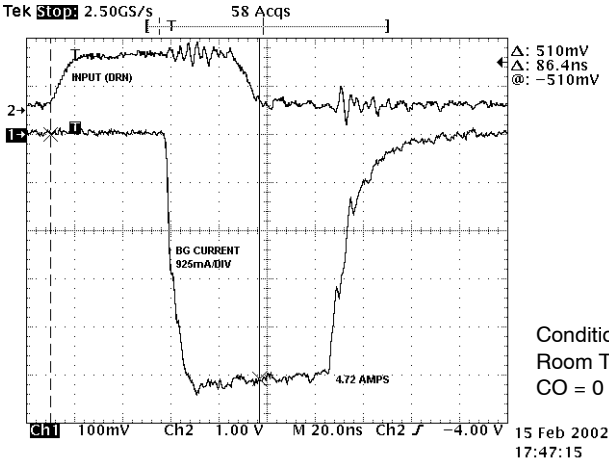
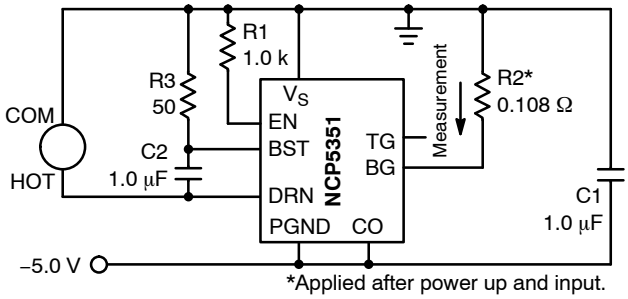


Figure 6. Top Gate Sinking





Conditions: V_S = 5.0 V;
Room Temperature;
CO = 0 V.

Figure 7. Bottom Gate Sinking Current from 0.108 Ω

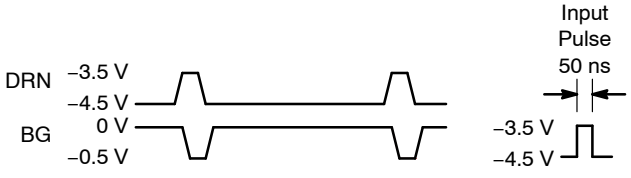
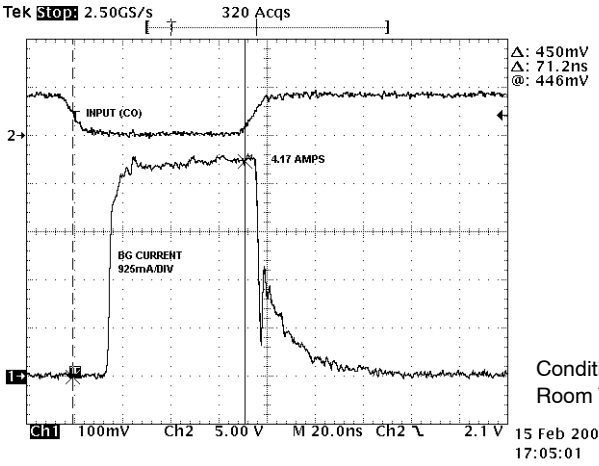
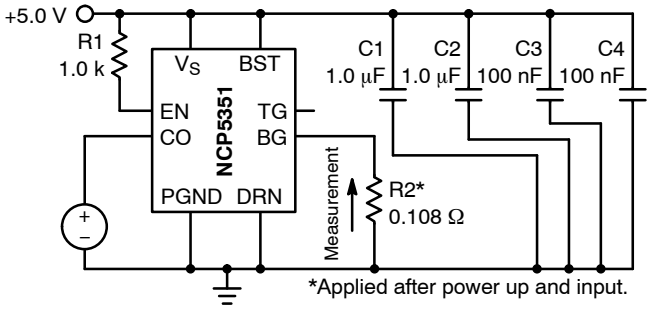


Figure 8. Bottom Gate Sinking

TYPICAL PERFORMANCE CHARACTERISTICS





Conditions: V_S = 5.0 V;
Room Temperature; DRN = 0 V.

Figure 9. Bottom Gate Sourcing Current into 0.108 Ω

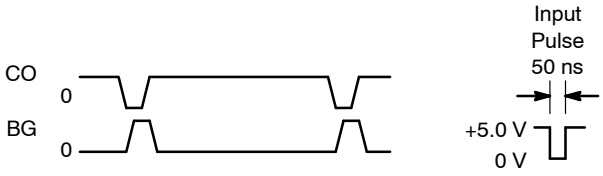
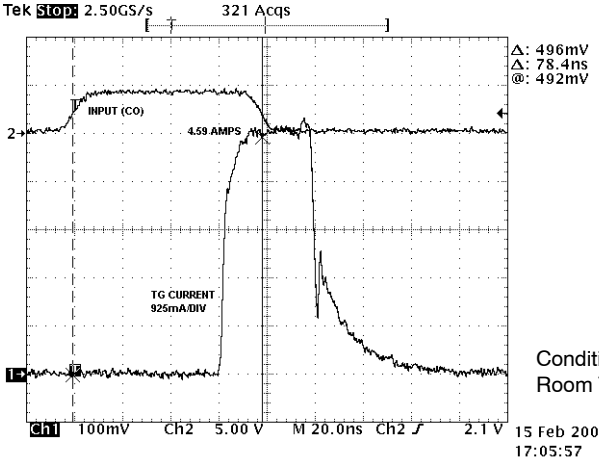
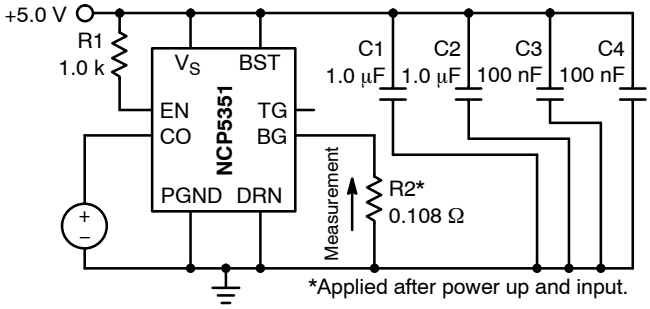


Figure 10. Bottom Gate Sourcing





Conditions: BST − DRN = 5.0 V;
Room Temperature; DRN = 0 V.

Figure 11. Top Gate Sourcing Current into 0.108 Ω

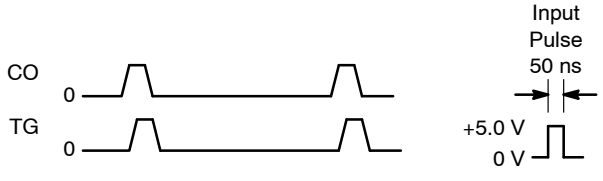


Figure 12. Top Gate Sourcing

TYPICAL PERFORMANCE CHARACTERISTICS

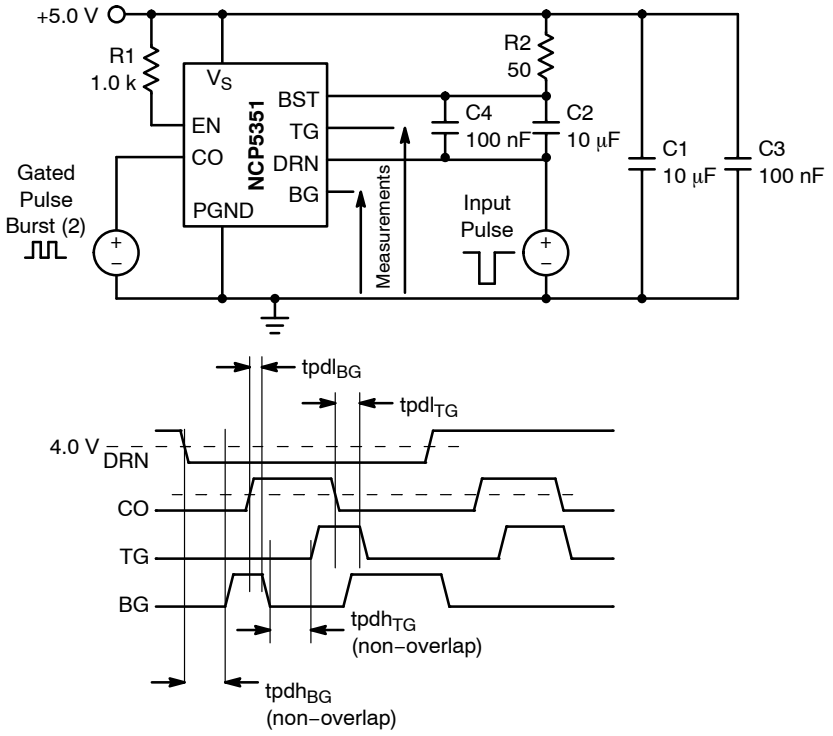
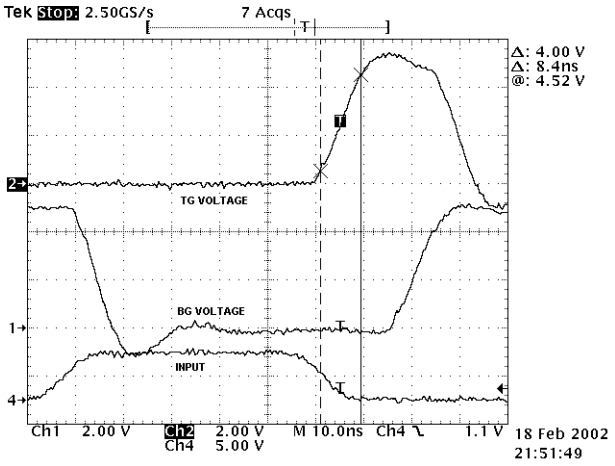
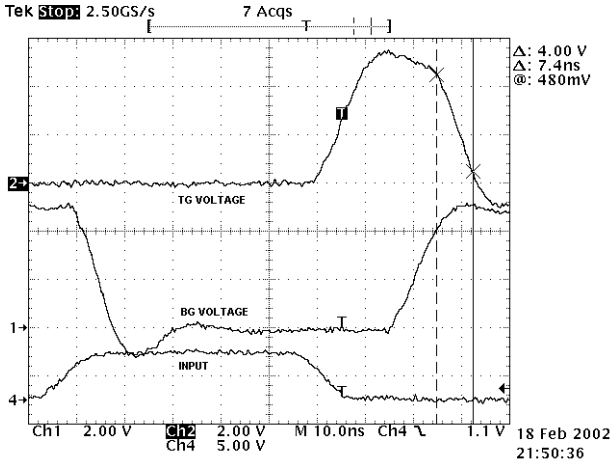


Figure 13. Nonoverlap Test Configuration



Conditions: V_S = 5.0 V; BST − DRN = 5.0 V; C_{LOAD} = 5.7 nF; Room Temperature.

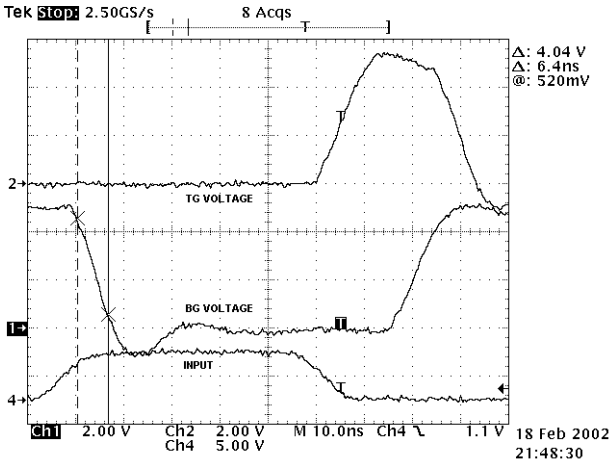
Figure 14. Top Gate Rise Time



Conditions: V_S = 5.0 V; BST − DRN = 5.0 V; C_{LOAD} = 5.7 nF; Room Temperature.

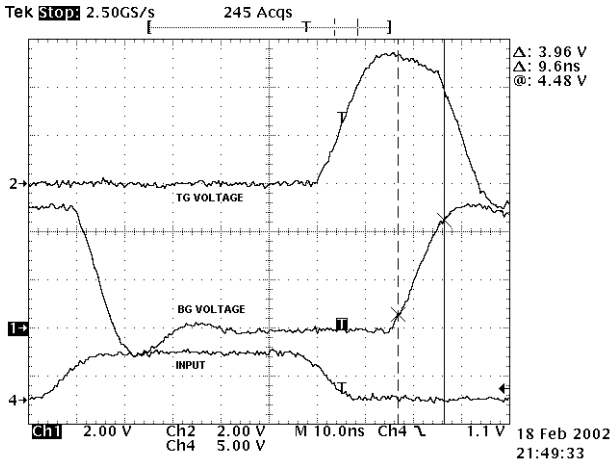
Figure 15. Top Gate Fall Time

TYPICAL PERFORMANCE CHARACTERISTICS



Conditions: V_S = 5.0 V; BST − DRN = 5.0 V; C_{LOAD} = 5.7 nF; Room Temperature.

Figure 16. Bottom Gate Fall Time



Conditions: V_S = 5.0 V; BST − DRN = 5.0 V; C_{LOAD} = 5.7 nF; Room Temperature.

Figure 17. Bottom Gate Rise Time

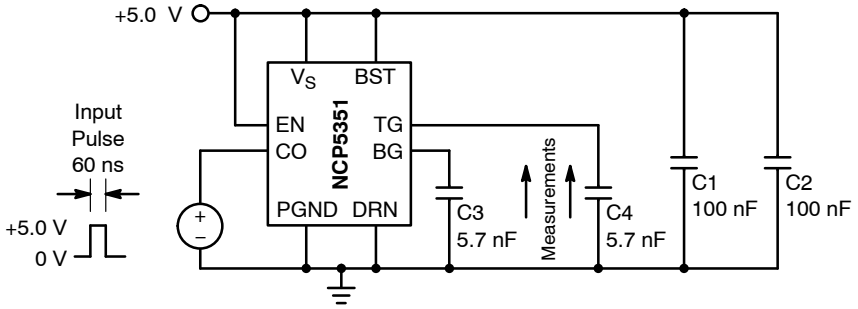


Figure 18. Bottom Gate and Top Gate Rise/Fall Time Test

ORDERING INFORMATION

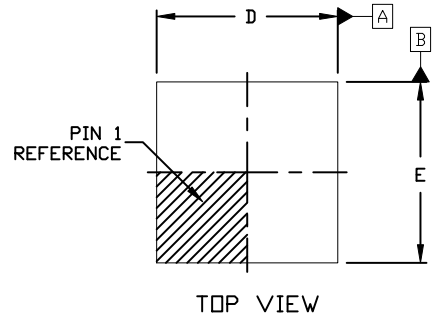
Device	Package	Shipping†
NCP5351D	SOIC−8	98 Units / Rail
NCP5351DG	SOIC−8 (Pb−Free)	98 Units / Rail
NCP5351DR2	SOIC−8	2500 / Tape & Reel
NCP5351DR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP5351MNR2	DFN10	2500 / Tape & Reel
NCP5351MNR2G	DFN10 (Pb−Free)	2500 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

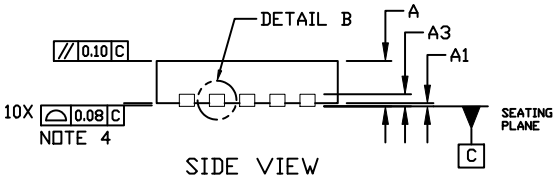
DFN10, 3x3, 0.5P
CASE 485C
ISSUE F

DATE 16 DEC 2021

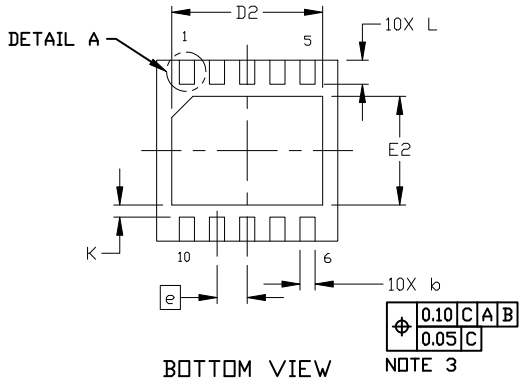
SCALE 2:1



TOP VIEW

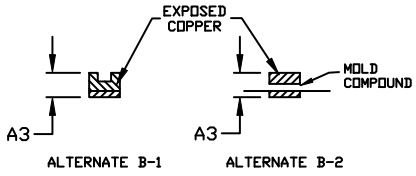


SIDE VIEW

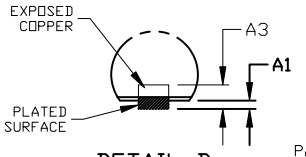


BOTTOM VIEW

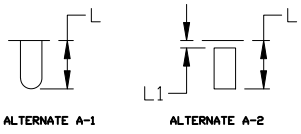
NOTES:
1. DIMENSION AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL b MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASH MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL.
6. FOR DEVICE OPN CONTAINING W OPTION, DETAIL A AND DETAIL B ALTERNATE CONSTRUCTIONS ARE NOT APPLICABLE. WETTABLE FLANK CONSTRUCTION IS DETAIL B AS SHOWN ON SIDE VIEW OF PACKAGE.



DETAIL B
ALTERNATE CONSTRUCTION

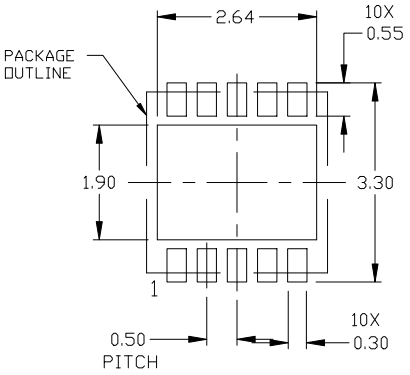


DETAIL B
WETTABLE FLANK
CONSTRUCTION



DETAIL A
ALTERNATE CONSTRUCTION

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	---	0.05
A3		0.20 REF	
b	0.18	0.23	0.30
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
E	2.90	3.00	3.10
E2	1.70	1.80	1.90
e		0.50 BSC	
K		0.20 REF	
L	0.30	0.40	0.50
L1	---	---	0.03



RECOMMENDED
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

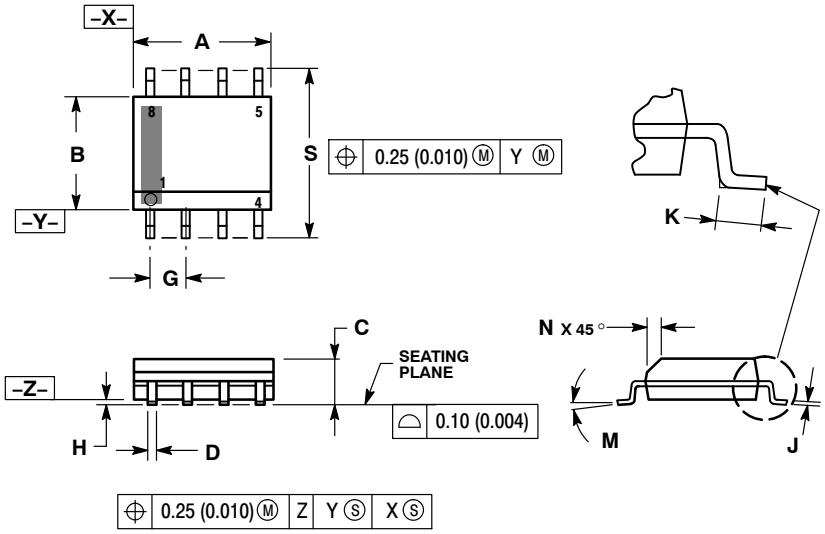
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON03161D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**DFN10, 3X3 MM, 0.5 MM PITCH**		**PAGE 1 OF 1**

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

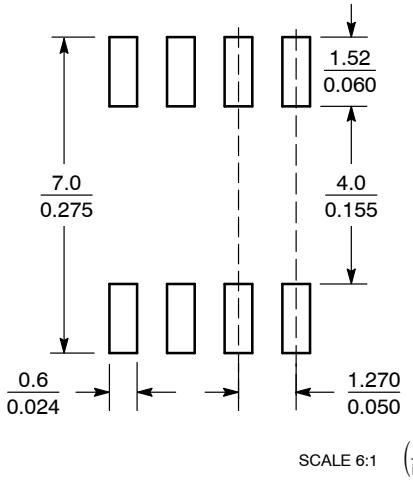
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

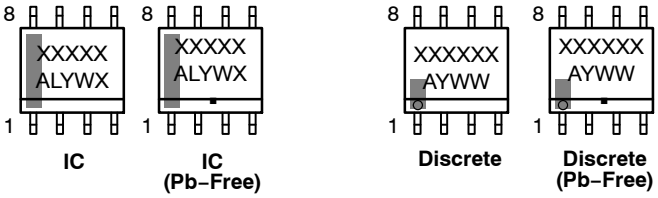
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

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