NCP4208

VR11.1 Digital Programmable 8-Phase Synchronous Buck Converter with I^2C Interface

The NCP4208 is an integrated power control IC with an I^2C interface. The NCP4208 is a highly efficient, multiphase, synchronous buck switching regulator controller, which aids design of High Efficiency and High Density solutions. The NCP4208 can be programmed for 1−, 2−, 3−, 4−, 5−, 6−, 7− or 8−phase operation, allowing for the construction of up to 8 complementary buck switching stages.

The NCP4208 supports $\overline{PSI}$, which is a power state indicator and can be used to reduce the number of operating phases at light loads. The I^2C interface enables digital programming of key system parameters to optimize system performance and provide feedback to the system.

The NCP4208 has a built in shunt regulator that allows the part to be powered from the +12 V system supply through a series resistor. The NCP4208 is specified over the extended commercial temperature range of 0°C to +85°C and is available in a 48 Lead QFN package.

Features

- Selectable 1−, 2−, 3−, 4−, 5−, 6−, 7− or 8−Phase Operation at Up to 1.5 MHz per Phase
- Temperature Measurement
- Logic−Level PWM Outputs for Interface to External High Power Drivers
- Fast−Enhanced PWM for Excellent Load Transient Performance
- Active Current Balancing Between All Output Phases
- Built−In Power−Good/Crowbar Blanking Supports On−The−Fly (OTF) VID Code Changes
- Digitally Programmable 0.375 V to 1.6 V Output Supports VR11.1 Specifications
- Short Circuit Protection with Latchoff Delay
- Supports $\overline{PSI}$ Power Saving Mode During Light Loads
- This is a Pb−Free Device

Applications

- Desktop PC
- Servers

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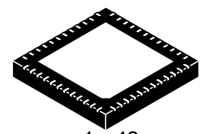
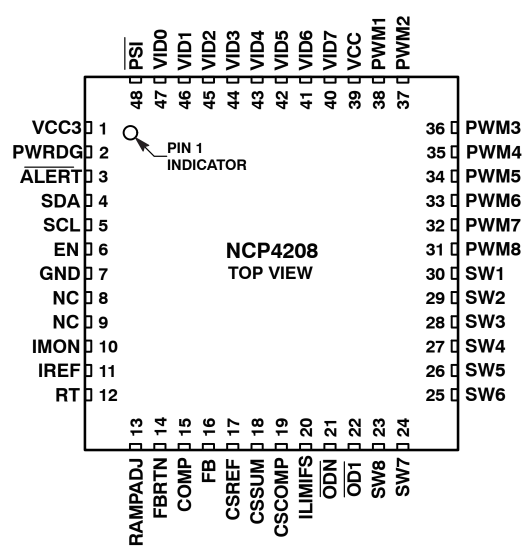


QFN 48
CASE 485AJ

MARKING DIAGRAM

A	= Assembly Lot
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
NCP4208MNR2G	QFN48 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

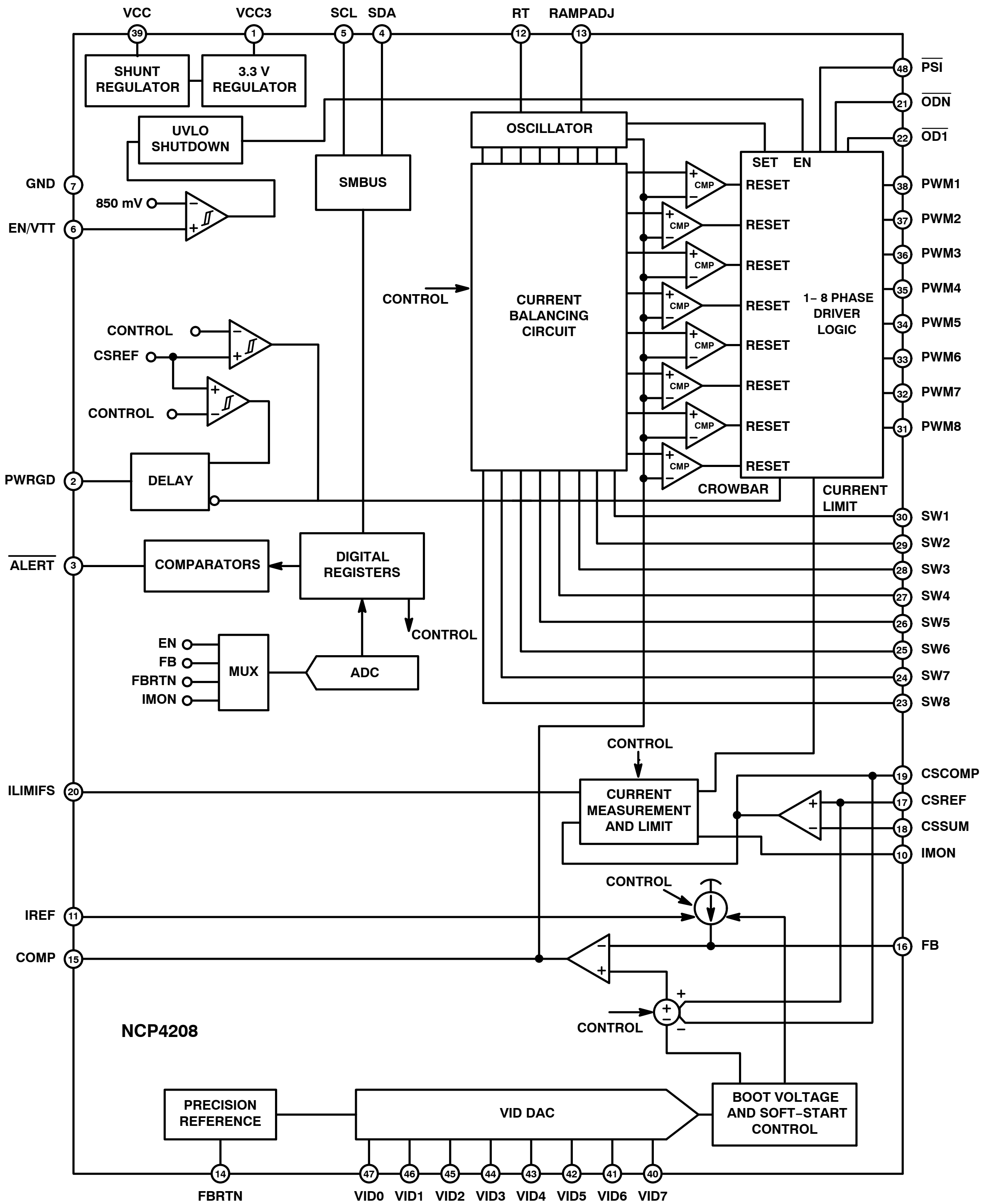


Figure 1. Simplified Block Diagram

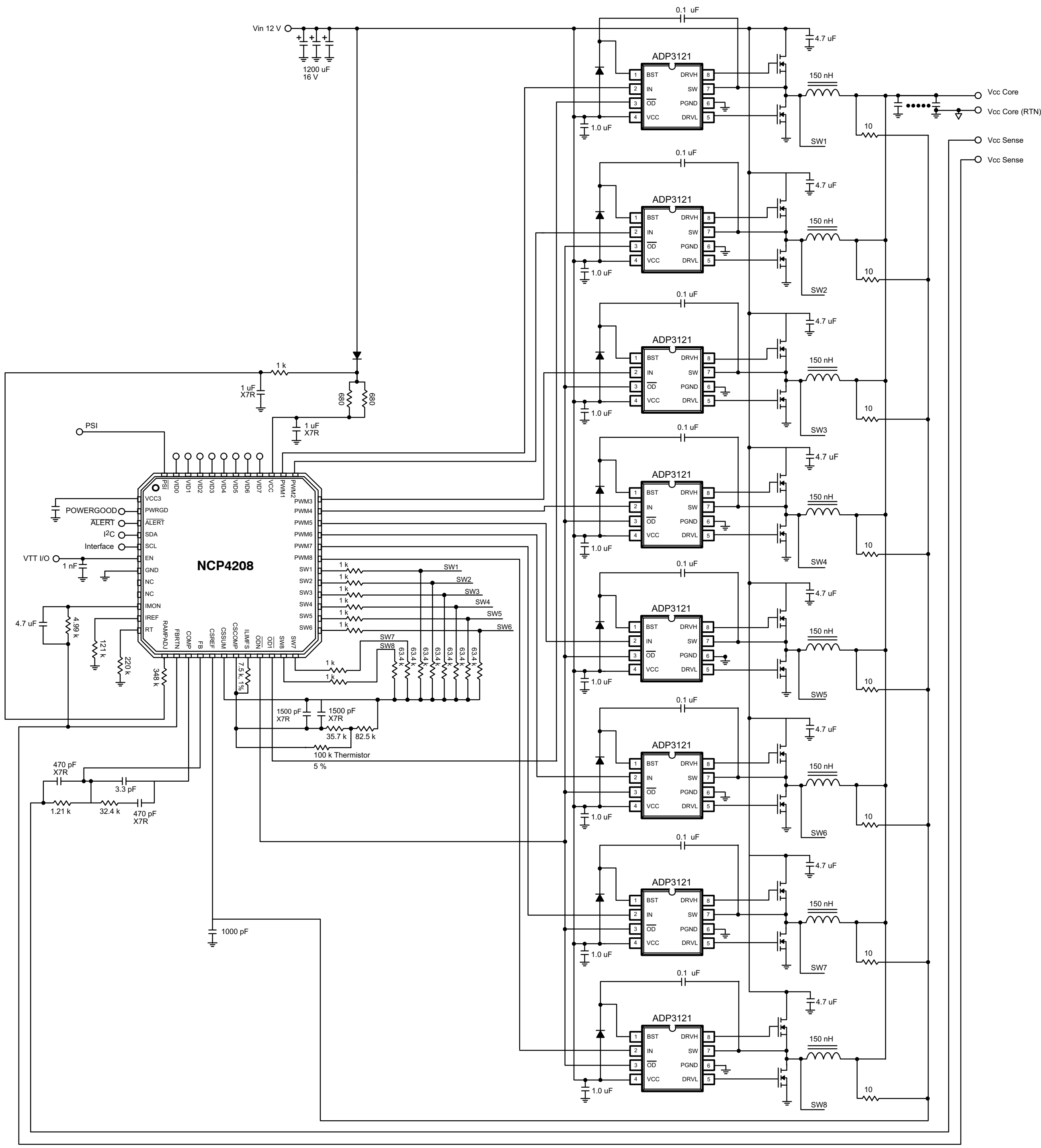


Figure 2. Application Schematic

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Range	V_{IN}	−0.3 to 6	V
FBRTN	V_{FBRTN}	−0.3 to +0.3	V
PWM2 to PWM8, Rampadj		−0.3 to V_{IN} + 0.3	V
SW1 to SW8		−5 to +25	V
SW1 to SW8 (<200 ns)		−10 to +25	V
All other Inputs and Outputs		−0.3 to V_{IN} + 0.3	V
Storage Temperature Range	TSTG	−65 to 150	°C
Operating Ambient Temperature Range		0 to 85	°C
ESD Capability, Human Body Model	ESDHBM	1.5	kV
ESD Capability, Machine Model	ESDMM	150	V
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 2)	T_{SLD}	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

1. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance, Junction−to−Air (Note 2) QFN, 7x7 mm	$R_{\theta JA}$	27	°C/W

2. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

TYPICAL CHARACTERISTICS

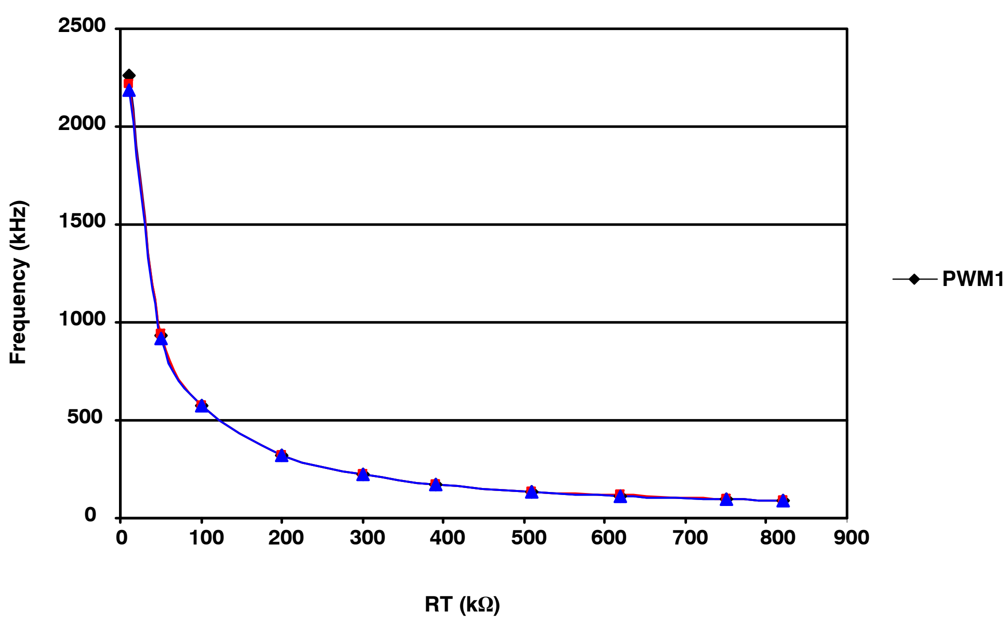


Figure 3. NCP4208 RT vs Frequency

PIN ASSIGNMENT

Pin No.	Mnemonic	Description
1	VCC3	3.3 V Power Supply Output. A capacitor from this pin to ground provided decoupling for the interval 3.3 V LDO.
2	PWRGD	Power−Good Output: Open−drain output that signals when the output voltage is outside of the proper operating range.
3	$\overline{ALERT}$	$\overline{ALERT}$ Output: Open drain output that asserts low when the VR exceeds a programmable limit. Can be configured for Comparator Mode or Interrupt Mode.
4	SDA	Digital Input / Output. I^2C serial data bidirectional pin. Requires pullup.
5	SCL	Digital Input. I^2C serial bus clock open drain input. Requires pullup.
6	EN	Power Supply Enable Input. Pulling this pin to GND disables the PWM outputs and pulls the PWRGD output low.
7	GND	Ground. All internal biasing and the logic output signals of the device are referenced to this ground.
8 to 9	NC	No Connect
10	IMON	Total Current Output Pin.
11	IREF	Current Reference Input. An external resistor from this pin to ground sets the reference current for IFB, and IILIMFS.
12	RT	Frequency Setting Resistor Input. An external resistor connected between this pin and GND sets the oscillator frequency of the device.
13	RAMPADJ	PWM Ramp Current Input. An external resistor from the converter input voltage to this pin sets the internal PWM ramp.
14	FBRTN	Feedback Return. VID DAC and error amplifier reference for remote sensing of the output voltage.
15	COMP	Error Amplifier Output and Compensation Point.
16	FB	Feedback Input. Error amplifier input for remote sensing of the output voltage. An external resistor between this pin and the output voltage sets the no load offset point.
17	CSREF	Current Sense Reference Voltage Input. The voltage on this pin is used as the reference for the current sense amplifier and the power−good and crowbar functions. This pin should be connected to the common point of the output inductors.
18	CSSUM	Current Sense Summing Node. External resistors from each switch node to this pin sum the average inductor currents together to measure the total output current.
19	CSCOMP	Current Sense Compensation Point. A resistor and capacitor from this pin to CSSUM determines the gain of the current sense amplifier and the positioning loop response time.
20	ILIMFS	Current Sense and Limit Scaling Pin. An external resistor from this pin to CSCOMP sets the internal current sensing signal for current limit and IMON. This value can be overwritten using the I^2C interface.
21	$\overline{ODN}$	Output Disable Logic Output for $\overline{PSI}$ operation. This pin is actively pulled low when $\overline{PSI}$ is low, otherwise it functions in the same way as $\overline{OD1}$.
22	$\overline{OD1}$	Output Disable Logic Output. This pin is actively pulled low when the EN input is low or when VCC is below its UVLO threshold to signal to the Driver IC that the driver high−side and low−side outputs should go low.
23 to 30	SW8 to SW1	Current Balance Inputs. Inputs for measuring the current level in each phase. The SW pins of unused phases should be left open.
31 to 38	PWM8 to PWM1	Logic−Level PWM Outputs. Each output is connected to the input of an external MOSFET driver such as the ADP3121. Connecting the PWM8, PWM7, PWM6, PWM5, PWM4, PWM3 and PWM2 outputs to VCC causes that phase to turn off, allowing the NCP4208 to operate as a 1−, 2−, 3−, 4−, 5−, 6−, 7−, or 8−phase controller.
39	VCC	Supply Voltage for the Device. A 340 Ω resistor should be placed between the 12 V system supply and the VCC pin. The internal shunt regulator maintains VCC = 5.0 V.
40 to 47	VID7 to VID0	Voltage Identification DAC Inputs. These eight pins are pulled down to GND, providing a logic zero if left open. When in normal operation mode, the DAC output programs the FB regulation voltage from 0.375 V to 1.6 V.
48	$\overline{PSI}$	Power State Indicator. Pulling this pin low places the controller in lower power state operation.

ELECTRICAL CHARACTERISTICS

V_{IN} = (5.0 V) FBRTN − GND, for typical values T_A = 25°C, for min/max values T_A = 0°C to 85°C; unless otherwise noted. (Notes 1 and 2)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Reference Current						
Reference Bias Voltage		V_{IREF}	1.75	1.8	1.85	V
Reference Bias Current	R_{IREF} = 121 kΩ	I_{IREF}		15		μA
Error Amplifier						
Output Voltage Range		V_{COMP}	0		4.4	V
Accuracy	Relative to nominal DAC output, referenced to FBRTN (refer to Figure 4) In startup	V_{FB} $V_{FB(BOOT)}$	−9.0 1.091	 1.1	+9.0 1.109	mV V
Load Line Positioning Accuracy			−77	−80	−83	mV
Load Line Range			−350		0	mV
Load Line Attenuation			0		100	%
Differential Non−linearity			−1.0		+1.0	LSB
Input Bias Current	$I_{FB} = I_{IREF}$	I_{FB}	13.3	15	18.5	μA
Offset Accuracy	VR Offset Register = 111111, VID = 1.0 V VR Offset Register = 011111, VID = 1.0 V			−193.75 193.75		mV
FBRTN Current		I_{FBRTN}		100	200	μA
Output Current	FB forced to V_{OUT} −3%	I_{COMP}		500		μA
Gain Bandwidth Product	COMP = FB	$GBW_{(ERR)}$		20		MHz
Slew Rate	COMP = FB			25		V/μs
BOOT Voltage Hold Time	Internal Timer	t_{BOOT}		2.0		ms
VID Inputs						
Input Low Voltage Input High Voltage	VID(X)	$V_{IL(VID)}$ $V_{IH(VID)}$	 0.8		0.3	V
Input Current		$I_{IN(VID)}$		−5.0		μA
VID Transition Delay Time	VID code change to FB change		400			ns
No CPU Detection Turn−Off Delay Time	VID code change to PWM going low		5.0			μs
Oscillator						
Frequency Range		f_{OSC}	0.25		9.0	MHz
Frequency Variation	T_A = 25°C, R_T = 500 kΩ, 4−phase T_A = 25°C, R_T = 250 kΩ, 4−phase T_A = 25°C, R_T = 121 kΩ, 4−phase	f_{PHASE}	170	195 375 750	225	kHz
Output Voltage	RT = 500 kΩ to GND	V_{RT}	1.9	2.01	2.1	V
RAMPADJ Output Voltage	RAMPADJ − FB, V_{FB} = 1.0 V, IRAMPADJ = −150 μA	$V_{RAMPADJ}$	−50		+50	mV
RAMPADJ Input Current Range		$I_{RAMPADJ}$	5.0		60	μA
Current Sense Amplifier						
Offset Voltage	CSSUM − CSREF (refer to Figure 5)	$V_{OS(CSA)}$	−1.0		+1.0	mV
Input Bias Current, CSREF	CSREF = 1.0 V	$I_{BIAS(CSREF)}$	−20		+20	μA
Input Bias Current, CSSUM	CSREF = 1.0 V	$I_{BIAS(CSSUM)}$	−10		+10	nA
Gain Bandwidth Product	CSSUM = CSCOMP	$GBW_{(CSA)}$		10		MHz
Slew Rate	C_{CSCOMP} = 10 pF			10		V/μs
Input Common−Mode Range	CSSUM and CSREF		0		3.0	V
Output Voltage Range			0.05		3.0	V
Output Current		I_{CSCOMP}		500		μA
Current Limit Latchoff Delay Time	Internal Timer			8.0		ms

1. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
2. Refer to Application Information section.
3. Values based on design and/or characterization.

ELECTRICAL CHARACTERISTICS

V_{IN} = (5.0 V) FBRTN − GND, for typical values T_A = 25°C, for min/max values T_A = 0°C to 85°C; unless otherwise noted. (Notes 1 and 2)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
$\overline{PSI}$						
Input Low Voltage Input High Voltage			 0.8		0.3	V
Input Current				−5.0		μA
Assertion Timing	Fsw = 300kHz			3.3		μs
De−assertion Timing	Fsw = 300kHz				825	ns
IMON						
Clamp Voltage			1.0		1.15	V
Accuracy	10 x (CSREF − CSCOMP) / R_{ILIM}		−3.0		3.0	%
Output Current					800	μA
Offset			−6.0		6.0	mV
Current Limit Comparator						
I_{LIM} Bias Current	CSREF − CSCOMP / R_{ILIM}, CSREF − CSCOMP = 150 mV, R_{ILIMC} = 7.5 kΩ	I_{LIM}		20		μA
Current Limit Threshold Current	4/3 x I_{IREF}	I_{CL}		20		μA
Current Balance Amplifier						
Common−Mode Range		$V_{SW(X)CM}$	−600		+200	mV
Input Resistance	SW(X) = 0 V	$R_{SW(X)}$	14	19	25	kΩ
Input Current	SW(X) = 0 V	$I_{SW(X)}$	7.0	12	20	μA
Input Current Matching	SW(X) = 0 V	$\Delta I_{SW(X)}$	−6.0		+6.0	%
Phase Balance Adj. Range Low	Phase Bal Registers = 00000			−25		%
Phase Balance Adj. Range High	Phase Bal Registers = 11111			+25		%
Delay Timer						
Internal Timer	Delay Time Register = 011			2.0		ms
Timer Range Low	Delay Time Register = 000			0.5		ms
Timer Range High	Delay Time Register = 111			4.0		ms
Soft−Start						
Internal Timer	Soft−Start Slope Register = 010			0.5		V/ms
Timer Range Low	Soft−Start Slope Register = 000			0.1		V/ms
Timer Range High	Soft−Start Slope Register = 111			1.5		V/ms
Enable Input						
Input Low Voltage Input High Voltage		$V_{IL(EN)}$ $V_{IH(EN)}$	 0.8		0.3	V
Input Current		$I_{IN(EN)}$		−1.0		μA
Delay Time	EN > 0.8 V, Internal Delay	$t_{DELAY(EN)}$		2.0		ms
$\overline{ODN}$ and $\overline{OD1}$ Outputs						
Output Low Voltage	$I_{OD(SINK)}$ = −400 μA	$V_{OL(\overline{ODN/1})}$		160	500	mV
Output High Voltage	$I_{OD(SOURCE)}$ = 400 μA	$V_{OL(\overline{ODN/1})}$	4.0	5.0		V
$\overline{ODN}$ / $\overline{OD1}$ Pulldown Resistor				60		kΩ
Power−Good Comparator						
Undervoltage Threshold	Relative to Nominal DAC Output	$V_{PWRGD(UV)}$	−600	−500	−400	mV
Undervoltage Adj. Range Low	PWRGD_LO Register = 000			−500		mV
Undervoltage Adj. Range High	PWRGD_LO Register = 111			−150		mV
Overvoltage Threshold	Relative to DAC Output, PWRGD_Hi = 00	$V_{PWRGD(OV)}$	200	300	400	mV

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2. Refer to Application Information section.
3. Values based on design and/or characterization.

ELECTRICAL CHARACTERISTICS

V_{IN} = (5.0 V) FBRTN − GND, for typical values T_A = 25°C, for min/max values T_A = 0°C to 85°C; unless otherwise noted. (Notes 1 and 2)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Power−Good Comparator						
Overvoltage Adjustment Range Low	PWRGD_Hi Register = 11			150		mV
Overvoltage Adjustment Range High	PWRGD_Hi Register = 00			300		mV
Output Low Voltage	$I_{PWRGD(SINK)}$ = −4 mA	$V_{OL(PWRGD)}$		150	300	mV
Power−Good Delay Time During Soft−Start VID Code Changing VID Code Static	 Internal Timer		 100	 2.0 250 200		 ms μs ns
Crowbar Trip Point Crowbar Adjustment Range Crowbar Reset Point	Relative to DAC Output, PWRGD_Hi = 00 PWRGD_Hi Limit Relative to FBRTN	$V_{CROWBAR}$	200 150 250	300 300	400 300 350	mV
Crowbar Delay Time VID Code Changing VID Code Static	Overvoltage to PWM going low	$t_{CROWBAR}$	 100	 250 400		 μs ns
PWM Outputs						
Output Low Voltage	$I_{PWM(SINK)}$ = −400 μA	$V_{OL(PWM)}$		160	500	mV
Output High Voltage	$I_{PWM(SOURCE)}$ = 400 μA	$V_{OH(PWM)}$	4.0	5.0		V
Duty Cycle Matching				±3		%
I²C Interface						
Logic High Input Voltage		$V_{IH(SDA,SCL)}$	2.1			V
Logic Low Input Voltage		$V_{IH(SDA,SCL)}$			0.8	V
Hysteresis				500		mV
SDA Output Low Voltage	I_{SDA} = −6 mA	V_{OL}			0.4	V
Input Current		V_{IH}; I_{IL}	−1.0		1.0	μA
Input Capacitance		$C_{SCL, SDA}$		5.0		pF
Clock Frequency		f_{SCL}			400	kHz
SCL Falling Edge to SDA Valid Time					1.0	μs
$\overline{ALERT}$, $\overline{FAULT}$ Outputs						
Output Low Voltage	I_{OUT} = −6 mA	V_{OL}			0.4	V
Output High Leakage Current	V_{OH} = 5.0 V	V_{OH}			1.0	μA
Analog / Digital Converter						
Total Unadjusted Error (TUE)				±1.0		%
Differential Non−linearity (DNL)	8 Bits			1.0		LSB
Conversion Time	Averaging Enabled (32 averages)			80		ms
Supply						
V_{CC}	V_{CC}		4.70	5.25	5.75	V
DC Supply Current	V_{SYSTEM} = 13.2 V, R_{SHUNT} = 340 Ω	I_{VCC}		21	26	mA
UVLO Turn−On Current				6.5	11	mA
UVLO Threshold Voltage	V_{CC} Rising	V_{UVLO}	9.0			V
UVLO Turn−Off Voltage	V_{CC} Falling			4.1		V
VCC3 Output Voltage	I_{VCC3} = 1 mA	V_{CC3}	3.0	3.3	3.6	V

1. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
2. Refer to Application Information section.
3. Values based on design and/or characterization.

TEST CIRCUITS

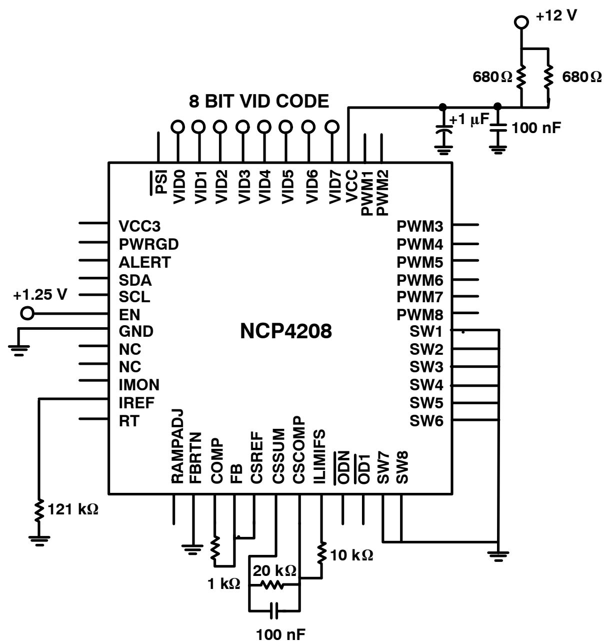


Figure 4. Closed−Loop Output Voltage Accuracy

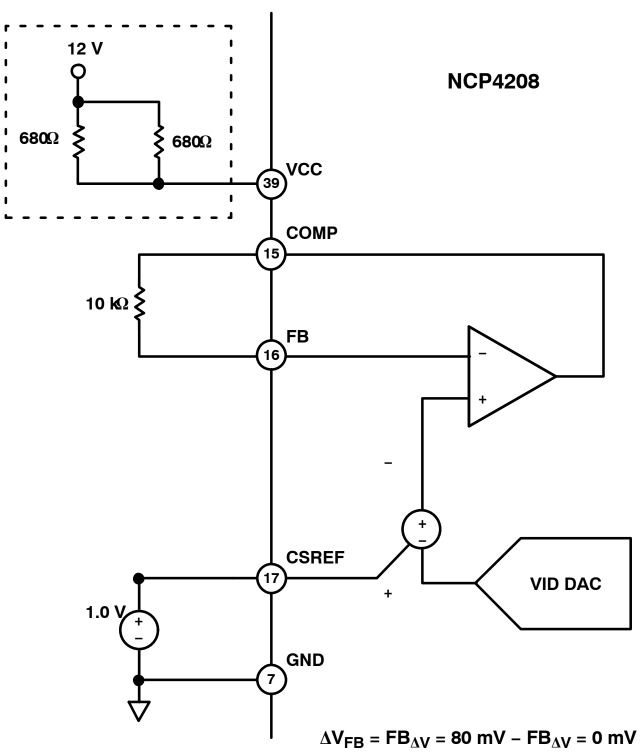


Figure 5. Current Sense Amplifier VOS

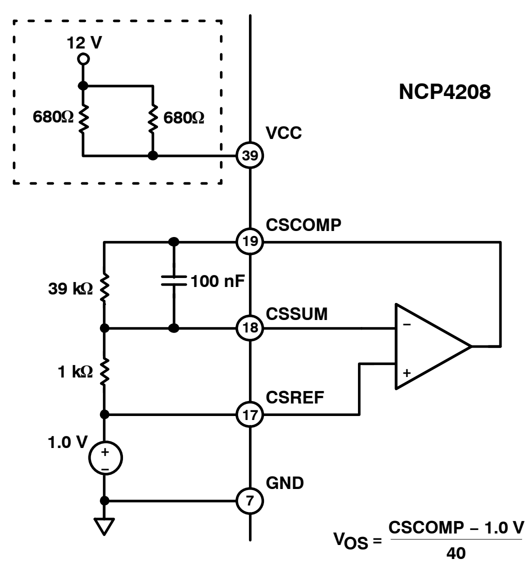


Figure 6. Positioning Voltage

Theory of Operation

The NCP4208 is an 8−phase VR11 controller; it combines a multi−mode, fixed frequency PWM control with multi−phase logic outputs for use in multi−phase synchronous buck CPU core supply power converters. In addition, the NCP4208 incorporates a serial interface to allow the programming of key system performance specifications and read back CPU data such as voltage, current and power. Multiphase operation is important for producing the high currents and low voltages demanded by today's microprocessors. Handling the high currents in a single−phase converter would place high thermal demands on the components in the system such as the inductors and MOSFETs.

Startup Sequence

The NCP4208 follows the VR11 startup sequence shown in Figure 7. After both the EN and UVLO conditions are met, a programmable internal timer goes through one cycle TD1. This delay cycle is programmed using Delay Command, default delay = 2 ms). The first eight clock cycles of TD2 are blanked from the PWM outputs and used for phase detection as explained in the following section. Then the programmable internal soft−start ramp is enabled (TD2) and the output comes up to the boot voltage of 1.1 V. The boot hold time is also set by the Delay Command. This second delay cycle is called TD3. During TD3 the processor VID pins settle to the required VID code. When TD3 is over, the NCP4208 reads the VID inputs and soft starts either up or down to the final VID voltage (TD4). After TD4 has been completed and the PWRGD masking time (equal to VID OTF masking) is finished, a third cycle of the internal timer sets the PWRGD blanking (TD5).

The internal delay and soft−start times are programmable using the serial interface and the Delay Command and Soft−Start Command.

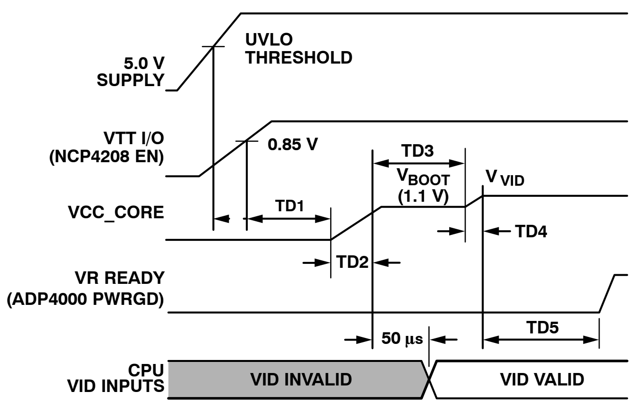


Figure 7. System Startup Sequence for VR11

Soft−Start

The Soft−Start slope for the output voltage is set by an internal timer. The default value is 0.5 V/msec, which can be programmed through the I[2]C interface. After TD1 and the phase detection cycle have been completed, the SS time (TD2 in Figure 7) starts. The SS circuit uses the internal VID DAC to increase the output voltage in 6.25 mV steps up to the 1.1 V boot voltage.

Once the SS circuit has reached the boot voltage, the boot voltage delay time (TD3) is started. The end of the boot voltage delay time signals the beginning of the second soft−start time (TD4). The SS voltage changes from the boot voltage to the programmed VID DAC voltage (either higher or lower) using 6.25 mV steps.

The soft− start slew rate is programmed using Bits <2:0> of the Ton_Rise (0xD5) command code. Table 1. Soft−Start Codes provides the soft−start values. Figure 8 shows typical startup waveforms for the NCP4208.

Table 1. Soft−Start Codes

Code	Soft−Start (V/msec)
000	0.3
001	0.3
010	0.5 = default
011	0.7
100	0.9
101	1.1
110	1.3
111	1.5

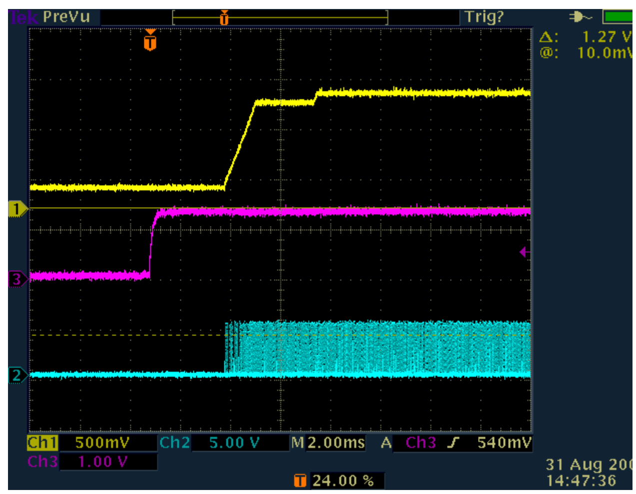


Figure 8. Typical Startup Waveforms
Channel 1: CSREF, Channel 2: EN, Channel 3: PWM1

Phase Detection

During startup, the number of operational phases and their phase relationship is determined by the internal circuitry that monitors the PWM outputs. Normally, the NCP4208 operates as an 8−phase PWM controller.

To operate as a 7−phase controller connect PWM8 to V_{CC}.

To operate as a 6−phase controller, connect PWM7 and PWM8 to V_{CC}. To operate as a 5−phase controller connect PWM6, PWM7 and PWM8 to V_{CC}. To operate as a 4−phase controller, connect PWM5, PWM6, PWM7 and PWM8 to V_{CC}. To operate as a 3−phase controller, connect PWM4, PWM5, PWM6, PWM7 and PWM8 to V_{CC}. To operate as a 2−phase controller connect PWM3, PWM4, PWM5, PWM6, PWM7 and PWM8 to V_{CC}. To operate as a 1−phase controller connect PWM2, PWM3, PWM4, PWM5, PWM6, PWM7 and PWM8 to V_{CC}.

Prior to soft−start, while EN is low, the PWM8, PWM7, PWM6, PWM5, PWM4, PWM3 and PWM2 pins sink approximately 100 μA each. An internal comparator checks each pin's voltage vs. a threshold of 3.0 V. If the pin is tied to V_{CC}, it is above the threshold. Otherwise, an internal current sink pulls the pin to GND, which is below the threshold. PWM1 is low during the phase detection interval that occurs during the first eight clock cycles of TD2. After this time, if the remaining PWM outputs are not pulled to V_{CC}, the 100 μA current sink is removed, and they function as normal PWM outputs. If they are pulled to V_{CC}, the 100 μA current source is removed, and the outputs are put into a high impedance state.

The PWM outputs are logic−level devices intended for driving fast response external gate drivers such as the ADP3121. Because each phase is monitored independently, operation approaching 100% duty cycle is possible. In addition, more than one output can be on at the same time to allow overlapping phases.

Master Clock Frequency

The clock frequency of the NCP4208 is set with an external resistor connected from the RT pin to ground. The frequency follows the graph in Figure 3. To determine the frequency per phase, the clock is divided by the number of phases in use. If all phases are in use, divide by 8. If 4 phases are in use divide by 4.

Output Voltage Differential Sensing

The NCP4208 combines differential sensing with a high accuracy VID DAC and reference, and a low offset error amplifier. This maintains a worst−case specification of ±9 mV differential sensing error over its full operating output voltage and temperature range. The output voltage is sensed between the FB pin and FBRTN pin. FB is connected through a resistor, R_B, to the regulation point, usually the remote sense pin of the microprocessor. FBRTN is connected directly to the remote sense ground point. The internal VID DAC and precision reference are referenced to FBRTN, which has a minimal current of 70 μA to allow accurate remote sensing. The internal error amplifier compares the output of the DAC to the FB pin to regulate the output voltage.

Output Current Sensing

The NCP4208 provides a dedicated current sense amplifier (CSA) to monitor the total output current for proper voltage positioning vs. load current, for the I_{MON} output and for current limit detection. Sensing the load current at the output gives the total real time current being delivered to the load, which is an inherently more accurate method than peak current detection or sampling the current across a sense element such as the low−side MOSFET. This amplifier can be configured several ways, depending on the objectives of the system, as follows:

- Output inductor DCR sensing without a thermistor for lowest cost.
- Output inductor DCR sensing with a thermistor for improved accuracy with tracking of inductor temperature.
- Sense resistors for highest accuracy measurements.

The positive input of the CSA is connected to the CSREF pin, which is connected to the average output voltage. The inputs to the amplifier are summed together through resistors from the sensing element, such as the switch node side of the output inductors, to the inverting input CSSUM. The feedback resistor between CSCOMP and CSSUM sets the gain of the amplifier and a filter capacitor is placed in parallel with this resistor. The gain of the amplifier is programmable by adjusting the feedback resistor. This difference signal is used internally to offset the VID DAC for voltage positioning. This different signal can be adjusted between 50%−150% of the external value using the I^2C Loadline Calibration (0xDE) and Loadline Set (0xDF) commands.

The difference between CSREF and CSCOMP is then used as a differential input for the current limit comparator.

To provide the best accuracy for sensing current, the CSA is designed to have a low offset input voltage. Also, the sensing gain is determined by external resistors to make it extremely accurate.

The CPU current can also be monitored over the I^2C interface. The current limit and the loadline can be programmed over I^2C interface.

Loadline Setting

The Loadline is programmable over the I^2C on the NCP4208. It is programmed using the Loadline Calibration (0xDE) and Loadline Set (0xDF) commands. The Loadline can be adjusted between 0% and 100% of the external R_{CSA}. In this example R_{CSA} = 1 mΩ. R_O needs to be 0.8 mΩ, therefore programming the Loadline Calibration + Loadline Set register to give a combined percentage of 80% will set the R_O to 0.8 mΩ.

Table 2. Loadline Commands

Code	Loadline (as a percentage of R_{CSA})
0 0000	0%
0 0001	3.226%
1 0000	51.6% = default
1 0001	53.3%
1 1110	96.7%
1 1111	100%

Current Limit Setpoint

The current limit threshold on the NCP4208 is programmed by a resistor between the I_{ILIMFS} pin and the CSCOMP pin. The I_{ILIMFS} current, I_{ILIMFS}, is compared with an internal current reference of 20 μA. If I_{ILIMFS} exceeds 20 μA then the output current has exceeded the limit and the current limit protection is tripped.

$$I_{ILIMFS} = \frac{V_{ILIMFS} - V_{CSCOMP}}{R_{ILIMFS}} \quad \text{(eq. 1)}$$

Where $V_{ILIMFS} = V_{CSREF}$

$$I_{ILIMFS} = \frac{V_{CSREF} - V_{CSCOMP}}{R_{ILIMFS}} \quad \text{(eq. 2)}$$

$$V_{CSREF} - V_{CSCOMP} = \frac{R_{CS}}{R_{PH}} \times R_L \times I_{LOAD}$$

Where R_L = DCR of the Inductor.

Assuming that:

$$\frac{R_{CS}}{R_{PH}} \times R_L = 1\ \text{m}\Omega \quad \text{(eq. 3)}$$

i.e. the external circuit is set up for a 1 mΩ Loadline then the R_{ILIMFS} is calculated as follows:

$$I_{ILIMFS} = \frac{1\ \text{m}\Omega \times I_{LOAD}}{R_{ILIMIFS}} \quad \text{(eq. 4)}$$

Assuming we want a current limit of 150 A that means that I_{LIMFS} must equal 20 μA at that load.

$$20\ \mu A = \frac{1\ \text{m}\Omega \times 150\ \text{AD}}{R_{ILIMIFS}} = 7.5\ \text{k}\Omega \quad \text{(eq. 5)}$$

Solving this equation for $R_{LIMITFS}$ we get 7.5 kΩ.

The current limit threshold can be modified from the resistor programmed value by using the I²C interface using Bits <4:0> of the Current Limit Threshold command (0xE2). The limit is programmable between 50% of the external limit and 146.7% of the external limit. The resolution is 3.3%. Table 3 gives some examples codes.

Table 3. Current Limit

Code	Current Limit (% of External Limit)
0 0000	50%
0 0001	53.3%
1 0000	100% = default
1 0001	103.3%
1 1110	143.3%
1 1111	146.7%

Active Impedance Control Mode

For controlling the dynamic output voltage droop as a function of output current, the CSA gain and loadline programming can be scaled to be equal to the droop impedance of the regulator times the output current. This droop voltage is then used to set the input control voltage to the system. The droop voltage is subtracted from the DAC reference input voltage directly to tell the error amplifier where the output voltage should be. This allows enhanced feed−forward response.

Output Current Monitor

I_{MON} is an analog output from the NCP4208 representing the total current being delivered to the load. It outputs an accurate current that is directly proportional to the current set by the I_{LIMFS} resistor. The current is then run through a parallel RC connected from the I_{MON} pin to the FBRTN pin to generate an accurately scaled and filtered voltage as per the VR11.1 specification. The size of the resistor is used to set the I_{MON} scaling.

$$I_{IMON} = 10 \times \frac{R_{CSA} \times I_{LOAD}}{R_{ILIMFS}} \quad \text{(eq. 6)}$$

and

$$R_{CSA} = \frac{\text{DCR(inductor)} \times \text{RCS}}{R_{PH}} \quad \text{(eq. 7)}$$

If the I_{MON} and the OCP need to be changed based on the TDC of the CPU, then the I_{LIMFS} resistor is the only component that needs to be changed. If the I_{MON} scaling is the only change needed then changing the I_{MON} resistor accomplishes this.

The I_{MON} pin also includes an active clamp to limit the I_{MON} voltage to 1.15 V MAX while maintaining 900 mV MIN full scale accurate reporting.

Current Control Mode and Thermal Balance

The NCP4208 has individual inputs (SW1 to SW8) for each phase that are used for monitoring the current of each phase. This information is combined with an internal ramp to create a current balancing feedback system that has been optimized for initial current balance accuracy and dynamic thermal balancing during operation. This current balance information is independent of the average output current information used for positioning as described in the Output Current Sensing section.

The magnitude of the internal ramp can be set to optimize the transient response of the system. It also monitors the supply voltage for feed−forward control for changes in the supply. A resistor connected from the power input voltage to the RAMPADJ pin determines the slope of the internal PWM ramp.

The balance between the phases can be programmed using the I²C Phase Bal SW(x) commands (0xE3 to 0xEA).

This allows each phase to be adjusted if there is a difference in temperature due to layout and airflow considerations. The phase balance can be adjusted from a default gain of 5 (Bits 4:0 = 10000). The minimum gain programmable is 3.75 (Bits 4:0 = 00000) and the maximum gain is 6.25 (Bits 4:0 = 11111).

Voltage Control Mode

A high gain, high bandwidth, voltage mode error amplifier is used for the voltage mode control loop. The control input voltage to the positive input is set via the VID logic according to the voltages listed in Table 8. The VID code is set using the VID Input pins or it can be programmed over the I^2C using the VOUT_Command. By default, the NCP4208 outputs a voltage corresponding to the VID Inputs. To output a voltage following the VOUT_Command the user first needs to program the required VID Code. Then the VID_EN Bits need to be enabled. The following is the sequence:

1. Program the required VID Code to the VOUT_Command code (0x21).
2. Set the VID_EN bit (Bit 3) in the VR Config 1A (0xD2) and on the VR Config 1B (0xD3).

This voltage is also offset by the droop voltage for active positioning of the output voltage as a function of current, commonly known as active voltage positioning. The output of the amplifier is the COMP pin, which sets the termination voltage for the internal PWM ramps.

The negative input (FB) is tied to the output sense location with Resistor R_B and is used for sensing and controlling the output voltage at this point. A current source (equal to I_{REF}) from the FB pin flowing through R_B is used for setting the no load offset voltage from the VID voltage. The no load voltage is negative with respect to the VID DAC for Intel CPU's. The main loop compensation is incorporated into the feedback network between FB and COMP.

An offset voltage can be added to the control voltage over the serial interface. This is done using Bits <5:0> of the VOUT_CAL (0xDD) Command. The max offset that can be applied is ±200 mV. The LSB size id 6.25 mV. A positive offset is applied when Bit 5 = 0. A negative offset is applied when Bit 5 = 1.

Table 4. Offset Codes

VOUT_Cal CODE	OFFSET VOLTAGE
0 0001	+6.25 mV
0 0010	+12.5 mV
0 0011	+18.75 mV

Dynamic VID

The NCP4208 has the ability to dynamically change the VID inputs while the controller is running. This allows the output voltage to change while the supply is running and supplying current to the load. This is commonly referred to as Dynamic VID (DVID). A DVID can occur under either light or heavy load conditions. The processor signals the controller by changing the VID inputs (or by programming a new VOUT_Command) in a single or multiple steps from the start code to the finish code. This change can be positive or negative.

When a VID bit changes state, the NCP4208 detects the change and ignores the DAC inputs for a minimum of 200 ns. This time prevents a false code due to logic skew while the VID inputs are changing. Additionally, the first VID change initiates the PWRGD and CROWBAR blanking functions for a minimum of 100 μs to prevent a false PWRGD or CROWBAR event. Each VID change resets the internal timer.

If a VID off code is detected the NCP4208 will wait for 5 μsec to ensure that the code is correct before initiating a shutdown of the controller.

The NCP4208 also uses the TON_Transition (0xD6) to limit the DVID slew rates. These can be encountered when the system does a large single VID step for power state changes, thus the DVID slew rate needs to be limited to prevent large inrush currents.

The transition slew rate is programmed using Bits <2:0> of the Ton_Transition (0xD6) command code. Table 5 provides the transition rate values.

Table 5. Transition Rate Codes

Code	Transition Rate (V/msec)
000	1
001	3
010	5 = default
011	7
100	9
101	11
110	13
111	15

Enhanced transient Mode

The NCP4208 incorporates enhanced transient response for both load step up and load release. For load step up it senses the output of the error amp to determine if a load step up has occurred and then sequences on the appropriate number of phases to ramp up the output current.

For load release, it also senses the output of the error amp and uses the load release information to trigger the TRDET pin, which is then used to adjust the error amp feedback for optimal positioning. This is especially important during high frequency load steps.

Additional information is used during load transients to ensure proper sequencing and balancing of phases during high frequency load steps as well as minimizing the stress on components such as the input filter and MOSFET's.

Current Reference

The I_{REF} pin is used to set an internal current reference. This reference current sets I_{FB}. A resistor to ground programs the current based on the 1.8 V output.

$$I_{REF} = \frac{1.8\ V}{R_{IREF}} \qquad \text{(eq. 8)}$$

Typically, R_{IREF} is set to 121 kΩ to program I_{REF} = 15 μA.

Internal Delay Timer

The delay times for the startup timing sequence are set by an internal timer. The default time is 2 msec which can be changed through the I^2C interface. This timer is used for multiple delay timings (TD1, TD3, and TD5) during the startup sequence. Also, it is used for timing the current limit latchoff as explained in the Current Limit section. The current limit timer is set to 4 times the delay timer.

The delay timer is programmed using Bits <2:0> of the Ton Delay command (0xD4). The delay can be programmed between 0.5 msec and 4 msec. Table 6 provides the programmable delay values.

Table 6. Delay Codes

Code	Delay (msec)
000	0.5
001	1
010	1.5
011	2 = default
100	2.5
101	3
110	3.5
111	4

Current Limit, Short−Circuit and Latchoff Protection

The NCP4208 compares a programmable current limit set point to the voltage from the output of the current sense amplifier. The level of current limit is set with the resistor from the ILIMFS pin to CSCOMP, and can be adjusted using the I^2C interface.

The current limit threshold can be modified from the resistor programmed value by using the I^2C interface using Bits <4:0> of the Current Limit Threshold command (0xE2). The limit is programmable between 50% of the external limit and 146.7% of the external limit. The resolution is 3.3%. The current limit threshold can be modified from the resistor programmed value by using the serial interface.

If the limit is reached and TD5 has completed, an internal latchoff delay time will start, and the controller will shut down if the fault is not removed. This delay is four times longer than the delay time during the startup sequence. The current limit delay time only starts after the TD5 has completed. If there is a current limit during startup, the NCP4208 will go through TD1 to TD5, and then start the latchoff time. As the controller continues to cycle the phases during the latchoff delay time, if the short is removed before the timer is complete, the controller can return to normal operation.

The latchoff function can be reset by either removing and reapplying the supply voltage to the NCP4208, or by toggling the EN pin low for a short time.

The OCP latchoff function can be disabled by using the I^2C interface. Setting the CLIM_EN bit (bit 1) of the VR Config 1A (0xD2) and VR Config 1B (0xD3) registers to 0 disables the current limit latchoff function. The NCP4208 can continue to operate in current limit indefinitely.

During startup when the output voltage is below 200 mV, a secondary current limit is active. This is necessary because the voltage swing of CSCOMP cannot go below ground. This secondary current limit limits controls of the internal COMP voltage to the PWM comparators to 1.5 V. This limits the voltage drop across the low−side MOSFETs through the current balance circuitry. Typical overcurrent latchoff waveforms are shown in Figure 9.

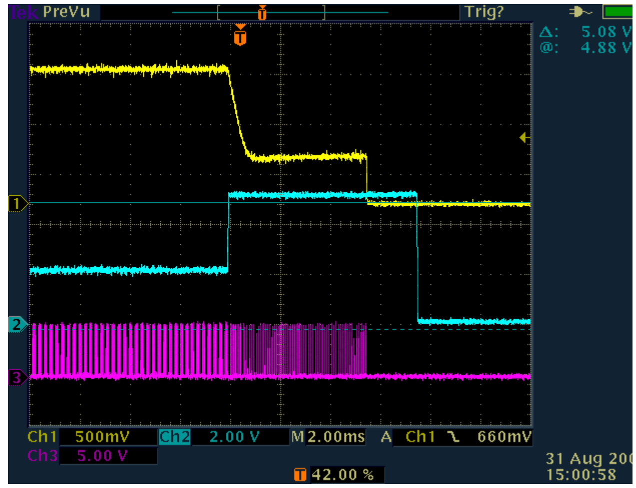


Figure 9. Overcurrent Latchoff Waveforms Channel 1: CSREF, Channel 2: COMP, Channel 3: PWM1

An inherent per phase current limit protects individual phases if one or more phases stops functioning because of a faulty component. This limit is based on the maximum normal mode COMP voltage.

Power Good Monitoring

The power good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open−drain output whose high level (when connected to a pullup resistor) indicates that the output voltage is within the nominal limits specified in the specifications above based on the VID voltage setting. PWRGD goes low if the output voltage is outside of this specified range, if the VID DAC inputs are in no CPU mode, or whenever the EN pin is pulled low. PWRGD is blanked during a DVID event for a period of 100 μs to prevent false signals during the time the output is changing.

The PWRGD circuitry also incorporates an initial turn−on delay time (TD5). Prior to the SS voltage reaching the programmed VID DAC voltage and the PWRGD masking time finishing, the PWRGD pin is held low. Once the SS circuit reaches the programmed DAC voltage, the internal timer operates.

The value for the PWRGD high limit and low limit can be programmed using the serial interface.

Power State Indicator

The $\overline{PSI}$ pin is an input used to determine the operating state of the load. If this input is pulled low, the load is in a low power state and the controller asserts the $\overline{ODN}$ pin low, which can be used to disable phases and maintain better efficiency at lighter loads.

The sequencing into and out of low power operation is maintained to minimize output deviations as well as providing full power load transients immediately after exiting a low power state. The number of phases switched on when $\overline{PSI}$ is asserted is set using Bits 7:6 of the Manufacturer Config Register 0x03. Table 7 shows which phases are enabled for each configuration.

Table 7. Configuration and Enabled Phases

# Phases Running Normally	Code	# Phases Running During $\overline{PSI}$	Current Limit Divided by:	Phases Running
8	00	1	4	1
	01	2	4	1 and 5
	10	4	2	1, 3, 5, 7
	11	4	2	1, 3, 5, 7
7	00	1	4	1
	01	1	4	1
	10	1	2	1
	11	1	2	1
6	00	1	4	1
	01	2	3	1 and 4
	10	3	2	1, 3, 5
	11	1	2	1, 3, 5
5	00	1	4	1
	01	1	2	1
	10	1	2	1
	11	1	2	1
4	00	1	4	1
	01	1	2	1
	10	1	2	1
	11	1	2	1
3	00	1	3	1
	01	1	2	1
	10	1	2	1
	11	1	2	1
2	00	1	2	1
	01	1	2	1
	10	1	2	1
	11	1	2	1
1	00	1	1	1
	01	1	1	1
	10	1	1	1
	11	1	1	1

Output Crowbar

As part of the protection for the load and output components of the supply, the PWM outputs are driven low (turning on the low−side MOSFETs) when the output voltage exceeds the upper crowbar threshold. This crowbar action stops once the output voltage falls below the release threshold of approximately 300 mV.

The value for the crowbar limit follows the programmable PWRGD high limit.

Turning on the low−side MOSFETs pulls down the output as the reverse current builds up in the inductors. If the output overvoltage is due to a short in the high−side MOSFET, this action current limits the input supply or blows its fuse, protecting the microprocessor from being destroyed.

Output Enable and UVLO

For the NCP4208 to begin switching, the input supply current to the controller must be higher than the UVLO threshold and the EN pin must be higher than its 0.8 V threshold. This initiates a system startup sequence. If either UVLO or EN is less than their respective thresholds, the NCP4208 is disabled. This holds the PWM outputs at ground and forces PWRGD, $\overline{ODN}$ and $\overline{OD1}$ signals low.

In the application circuit (see Figure 2), the $\overline{OD1}$ pin should be connected to the $\overline{OD}$ inputs of the external drivers for the phases that are always on. The $\overline{ODN}$ pin should be connected to the $\overline{OD}$ inputs of the external drivers on the phases that are shut down during low power operation. Grounding the driver $\overline{OD}$ inputs disables the drivers such that both DRVH and DRVL are grounded. This feature is important in preventing the discharge of the output capacitors when the controller is shut off. If the driver outputs are not disabled, a negative voltage can be generated during output due to the high current discharge of the output capacitors through the inductors.

The NCP4208 uses a shunt to generate 5.0 V from the 12 V supply range. A trade-off can be made between the power dissipated in the shunt resistor and the UVLO threshold. Figure 10 shows the typical resistor value needed to realize certain UVLO voltages. It also gives the maximum power dissipated in the shunt resistor for these UVLO voltages.

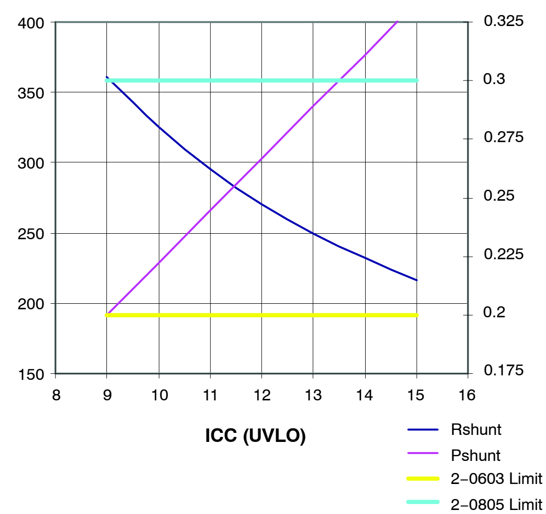


Figure 10. Typical Shunt Resistor Value and Power Dissipation for Different UVLO Voltage

I^{2}C Interface

Control of the NCP4208 is carried out using the I^{2}C Interface. The NCP4208 SMBus address is 0x20 (010 0000). With the $R/\overline{W}$ bit set to 0 this gives an 8 bit address of 0x40.

Data is sent over the serial bus in sequences of nine clock pulses: 8 bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low−to−high transition when the clock is high might be interpreted as a stop signal. The number of data bytes that can be transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.

1. When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the tenth clock pulse to assert a stop condition. In read mode, the master device overrides the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse; this is known as No Acknowledge. The master takes the data line low during the low period before the tenth clock pulse, and then high during the tenth clock pulse to assert a stop condition.

   Any number of bytes of data can be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

   In the NCP4208, write operations contain one, two or three bytes, and read operations contain one or two bytes. The command code or register address determines the number of bytes to be read or written, See the register map for more information.

   To write data to one of the device data registers or read data from it, the address pointer register must be set so that the correct data register is addressed (i.e. command code), and then data can be written to that register or read from it. The first byte of a read or write operation always contains an address that is stored in the address pointer register. If data is to be written to the device, the write operation contains a second data byte that is written to the register selected by the address pointer register.

   This write byte operation is shown in Figure 12. The device address is sent over the bus, and then $R/\overline{W}$ is set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the address pointer register. The second data byte is the data to be written to the internal data register.

2. The read byte operation is shown in Figure 13. First the command code needs to be written to the NCP4208 so that the required data is sent back. This is done by performing a write to the NCP4208 as before, but only the data byte containing the register address is sent, because no data is written to the register. A repeated start is then issued and a read operation is then performed consisting of the serial bus address; $R/\overline{W}$ bit set to 1, followed by the data byte read from the data register.

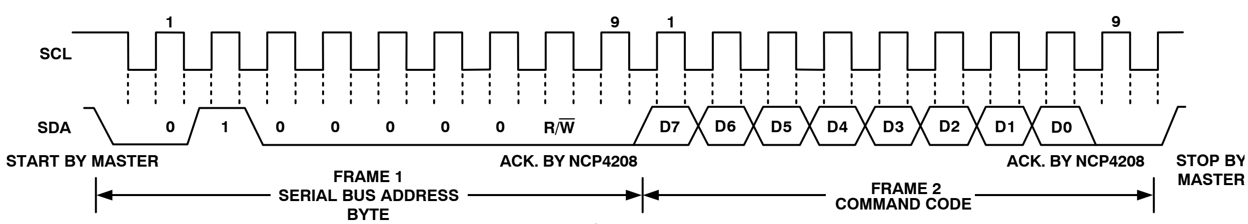


Figure 11. Send Byte

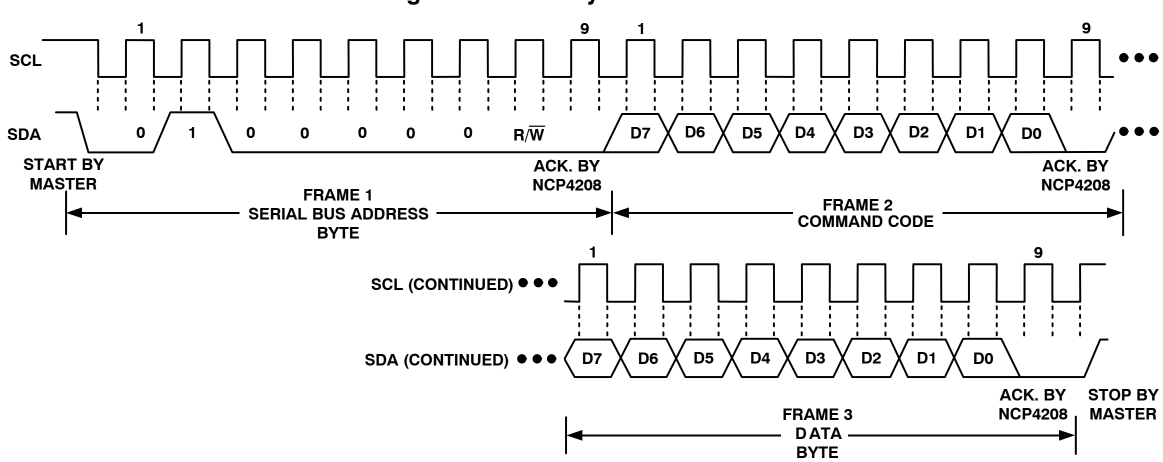


Figure 12. Write Byte

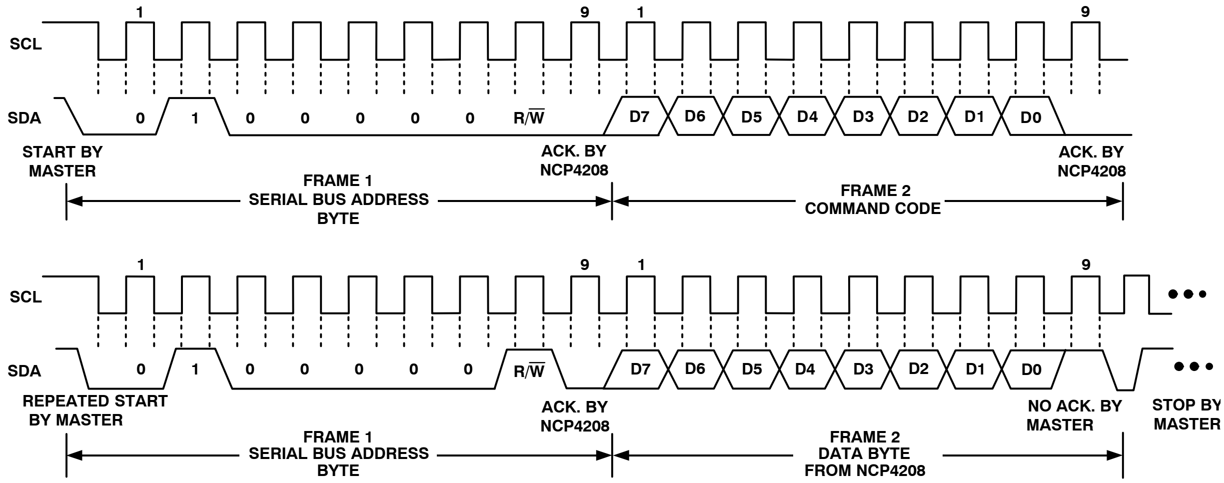


Figure 13. Read Byte

3. It is not possible to read or write a data byte from a data register without first writing to the address pointer register, even if the address pointer register is already at the correct value.
4. In addition to supporting the send byte, the NCP4208 also supports the read byte, write byte, read word and write word protocols.

Write Operations

The following abbreviations are used in the diagrams:

S—START
P—STOP
R—READ
W—WRITE
A—ACKNOWLEDGE
$\overline{A}$—NO ACKNOWLEDGE

The NCP4208 uses the following I^2C write protocols.

Send Byte

In this operation, the master device sends a single command byte to a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7−bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master asserts a stop condition on SDA and the transaction ends.

For the NCP4208, the send byte protocol is used to clear Faults. This operation is shown in Figure 14.

1	2	3		4	5	6
S	SLAVE ADDRESS	W	A	COMMAND CODE	A	P

Figure 14. Send Byte Command

If the master is required to read data from the register immediately after setting up the address, it can assert a repeat start condition immediately after the final ACK and carry out a single byte read without asserting an intermediate stop condition.

Write Byte

In this operation, the master device sends a command byte and one data byte to the slave device as follows: The master device asserts a start condition on SDA.

1. The master sends the 7−bit slave address followed by the write bit (low).
2. The addressed slave device asserts ACK on SDA.
3. The master sends a command code.
4. The slave asserts ACK on SDA.
5. The master sends a data byte.
6. The slave asserts ACK on SDA.
7. The master asserts a stop condition on SDA and the transaction ends.

The byte write operation is shown Figure 15.

1	2	3		4	5	6	7	8
S	SLAVE ADDRESS	W	A	COMMAND CODE	A	DATA	A	P

Figure 15. Single Byte Write to a Register

Write Word

In this operation, the master device sends a command byte and two data bytes to the slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7−bit slave address followed by the write bit (low).

3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master sends the first data byte.
7. The slave asserts ACK on SDA.
8. The master sends the second data byte.
9. The slave asserts ACK on SDA.
10. The master asserts a stop condition on SDA and the transaction ends.

The word write operation is shown in Figure 16.

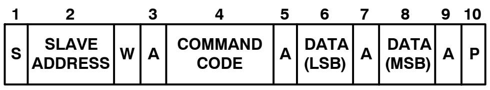


Figure 16. Single Word Write to a Register

Block Write

In this operation, the master device sends a command byte and a byte count followed by the stated number of data bytes to the slave device as follows:

1. The master device asserts a START condition on SDA.
2. The master sends the 7−bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master sends the byte count N
7. The slave asserts ACK on SDA.
8. The master sends the first data byte
9. The slave asserts ACK on SDA.
10. The master sends the second data byte.
11. The slave asserts ACK on SDA.
12. The master sends the remainder of the data byes.
13. The slave asserts an ACK on SDA after each data byte.
14. After the last data byte the master asserts a STOP condition on SDA.

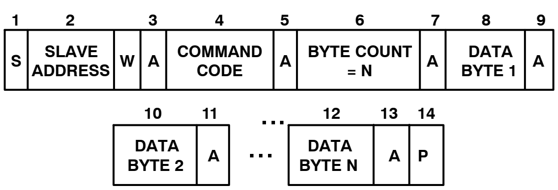


Figure 17. Block Write to a Register

Read Operations

The NCP4208 uses the following I^{2}C read protocols.

Read Byte

In this operation, the master device receives a single byte from a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7−bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserted ACK on SDA.
6. The master sends a repeated start condition on SDA.
7. The master sends the 7 bit slave address followed by the read bit (high).
8. The slave asserts ACK on SDA.
9. The slave sends the Data Byte.
10. The master asserts NO ACK on SDA.
11. The master asserts a stop condition on SDA and the transaction ends.

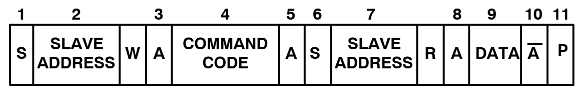


Figure 18. Single Byte Read from a Register

Read Word

In this operation, the master device receives two data bytes from a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7−bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserted ACK on SDA.
6. The master sends a repeated start condition on SDA.
7. The master sends the 7 bit slave address followed by the read bit (high).
8. The slave asserts ACK on SDA.
9. The slave sends the first Data Byte (low Data Byte).
10. The master asserts ACK on SDA.
11. The slave sends the second Data Byte (high Data Byte).
12. The masters asserts a No ACK on SDA
13. The master asserts a stop condition on SDA and the transaction ends.

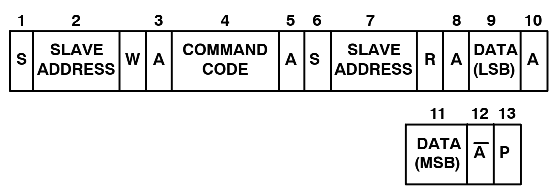


Figure 19. Word Read from a Command Coder

In this operation, the master device sends a command byte, the slave sends a byte count followed by the stated number of data bytes to the master device as follows:

1. The master device asserts a START condition on SDA.
2. The master sends the 7−bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a REPEATED START condition on SDA.

5. The master sends the 7−bit slave address followed by the read bit (high).
6. The slave asserts ACK on SDA.
7. The slave sends the byte count N.
8. The master asserts ACK on SDA.
9. The slave sends the first data byte.
10. The master asserts ACK on SDA.
11. The slave sends the remainder of the data byes, the master asserts an ACK on SDA after each data byte.
12. After the last data byte the master asserts a No ACK on SDA.
13. The master asserts a STOP condition on SDA.

Configuration Register 1 (0xD1)

Bit 3 BUS_TO_EN = 1; Bus timeout enabled.

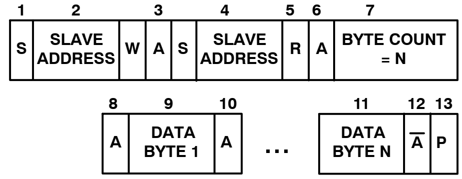


Figure 20. Block Write to a Command Coder

I^2C Timeout

The NCP4208 includes a I^2C timeout feature. If there is no I^2C activity for 35 ms, the NCP4208 assumes that the bus is locked and releases the bus. This prevents the device from locking or holding the I^2C expecting data. The timeout feature can be disabled.

Table 8. VR11 and VR10.x VID CODES for the NCP4208

OUTPUT	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
OFF	0	0	0	0	0	0	0	0
OFF	0	0	0	0	0	0	0	1
1.60000	0	0	0	0	0	0	1	0
1.59375	0	0	0	0	0	0	1	1
1.58750	0	0	0	0	0	1	0	0
1.58125	0	0	0	0	0	1	0	1
1.57500	0	0	0	0	0	1	1	0
1.56875	0	0	0	0	0	1	1	1
1.56250	0	0	0	0	1	0	0	0
1.55625	0	0	0	0	1	0	0	1
1.55000	0	0	0	0	1	0	1	0
1.54375	0	0	0	0	1	0	1	1
1.53750	0	0	0	0	1	1	0	0
1.53125	0	0	0	0	1	1	0	1
1.52500	0	0	0	0	1	1	1	0
1.51875	0	0	0	0	1	1	1	1
1.51250	0	0	0	1	0	0	0	0
1.50625	0	0	0	1	0	0	0	1
1.50000	0	0	0	1	0	0	1	0
1.49375	0	0	0	1	0	0	1	1
1.48750	0	0	0	1	0	1	0	0
1.48125	0	0	0	1	0	1	0	1
1.47500	0	0	0	1	0	1	1	0
1.46875	0	0	0	1	0	1	1	1
1.46250	0	0	0	1	1	0	0	0
1.45625	0	0	0	1	1	0	0	1
1.45000	0	0	0	1	1	0	1	0
1.44375	0	0	0	1	1	0	1	1
1.43750	0	0	0	1	1	1	0	0
1.43125	0	0	0	1	1	1	0	1
1.42500	0	0	0	1	1	1	1	0
1.41875	0	0	0	1	1	1	1	1
1.41250	0	0	1	0	0	0	0	0
1.40625	0	0	1	0	0	0	0	1
1.40000	0	0	1	0	0	0	1	0

Table 8. VR11 and VR10.x VID CODES for the NCP4208

OUTPUT	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
1.39375	0	0	1	0	0	0	1	1
1.38750	0	0	1	0	0	1	0	0
1.38125	0	0	1	0	0	1	0	1
1.37500	0	0	1	0	0	1	1	0
1.36875	0	0	1	0	0	1	1	1
1.36250	0	0	1	0	1	0	0	0
1.35625	0	0	1	0	1	0	0	1
1.35000	0	0	1	0	1	0	1	0
1.34375	0	0	1	0	1	0	1	1
1.33750	0	0	1	0	1	1	0	0
1.33125	0	0	1	0	1	1	0	1
1.32500	0	0	1	0	1	1	1	0
1.31875	0	0	1	0	1	1	1	1
1.31250	0	0	1	1	0	0	0	0
1.30625	0	0	1	1	0	0	0	1
1.30000	0	0	1	1	0	0	1	0
1.29375	0	0	1	1	0	0	1	1
1.28750	0	0	1	1	0	1	0	0
1.28125	0	0	1	1	0	1	0	1
1.27500	0	0	1	1	0	1	1	0
1.26875	0	0	1	1	0	1	1	1
1.26250	0	0	1	1	1	0	0	0
1.25625	0	0	1	1	1	0	0	1
1.25000	0	0	1	1	1	0	1	0
1.24375	0	0	1	1	1	0	1	1
1.23750	0	0	1	1	1	1	0	0
1.23125	0	0	1	1	1	1	0	1
1.22500	0	0	1	1	1	1	1	0
1.21875	0	0	1	1	1	1	1	1
1.21250	0	1	0	0	0	0	0	0
1.20625	0	1	0	0	0	0	0	1
1.20000	0	1	0	0	0	0	1	0
1.19375	0	1	0	0	0	0	1	1
1.18750	0	1	0	0	0	1	0	0
1.18125	0	1	0	0	0	1	0	1
1.17500	0	1	0	0	0	1	1	0
1.16875	0	1	0	0	0	1	1	1
1.16250	0	1	0	0	1	0	0	0
1.15625	0	1	0	0	1	0	0	1
1.15000	0	1	0	0	1	0	1	0
1.14375	0	1	0	0	1	0	1	1
1.13750	0	1	0	0	1	1	0	0
1.13125	0	1	0	0	1	1	0	1
1.12500	0	1	0	0	1	1	1	0
1.11875	0	1	0	0	1	1	1	1
1.11250	0	1	0	1	0	0	0	0
1.10625	0	1	0	1	0	0	0	1
1.10000	0	1	0	1	0	0	1	0
1.09375	0	1	0	1	0	0	1	1

Table 8. VR11 and VR10.x VID CODES for the NCP4208

OUTPUT	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
1.08750	0	1	0	1	0	1	0	0
1.08125	0	1	0	1	0	1	0	1
1.07500	0	1	0	1	0	1	1	0
1.06875	0	1	0	1	0	1	1	1
1.06250	0	1	0	1	1	0	0	0
1.05625	0	1	0	1	1	0	0	1
1.05000	0	1	0	1	1	0	1	0
1.04375	0	1	0	1	1	0	1	1
1.03750	0	1	0	1	1	1	0	0
1.03125	0	1	0	1	1	1	0	1
1.02500	0	1	0	1	1	1	1	0
1.01875	0	1	0	1	1	1	1	1
1.01250	0	1	1	0	0	0	0	0
1.00625	0	1	1	0	0	0	0	1
1.00000	0	1	1	0	0	0	1	0
0.99375	0	1	1	0	0	0	1	1
0.98750	0	1	1	0	0	1	0	0
0.98125	0	1	1	0	0	1	0	1
0.97500	0	1	1	0	0	1	1	0
0.96875	0	1	1	0	0	1	1	1
0.96250	0	1	1	0	1	0	0	0
0.95625	0	1	1	0	1	0	0	1
0.95000	0	1	1	0	1	0	1	0
0.94375	0	1	1	0	1	0	1	1
0.93750	0	1	1	0	1	1	0	0
0.93125	0	1	1	0	1	1	0	1
0.92500	0	1	1	0	1	1	1	0
0.91875	0	1	1	0	1	1	1	1
0.91250	0	1	1	1	0	0	0	0
0.90625	0	1	1	1	0	0	0	1
0.90000	0	1	1	1	0	0	1	0
0.89375	0	1	1	1	0	0	1	1
0.88750	0	1	1	1	0	1	0	0
0.88125	0	1	1	1	0	1	0	1
0.87500	0	1	1	1	0	1	1	0
0.86875	0	1	1	1	0	1	1	1
0.86250	0	1	1	1	1	0	0	0
0.85625	0	1	1	1	1	0	0	1
0.85000	0	1	1	1	1	0	1	0
0.84375	0	1	1	1	1	0	1	1
0.83750	0	1	1	1	1	1	0	0
0.83125	0	1	1	1	1	1	0	1
0.82500	0	1	1	1	1	1	1	0
0.81875	0	1	1	1	1	1	1	1
0.81250	1	0	0	0	0	0	0	0
0.80625	1	0	0	0	0	0	0	1
0.80000	1	0	0	0	0	0	1	0
0.79375	1	0	0	0	0	0	1	1
0.78750	1	0	0	0	0	1	0	0

Table 8. VR11 and VR10.x VID CODES for the NCP4208

OUTPUT	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
0.78125	1	0	0	0	0	1	0	1
0.77500	1	0	0	0	0	1	1	0
0.76875	1	0	0	0	0	1	1	1
0.76250	1	0	0	0	1	0	0	0
0.75625	1	0	0	0	1	0	0	1
0.75000	1	0	0	0	1	0	1	0
0.74375	1	0	0	0	1	0	1	1
0.73750	1	0	0	0	1	1	0	0
0.73125	1	0	0	0	1	1	0	1
0.72500	1	0	0	0	1	1	1	0
0.71875	1	0	0	0	1	1	1	1
0.71250	1	0	0	1	0	0	0	0
0.70625	1	0	0	1	0	0	0	1
0.70000	1	0	0	1	0	0	1	0
0.69375	1	0	0	1	0	0	1	1
0.68750	1	0	0	1	0	1	0	0
0.68125	1	0	0	1	0	1	0	1
0.67500	1	0	0	1	0	1	1	0
0.66875	1	0	0	1	0	1	1	1
0.66250	1	0	0	1	1	0	0	0
0.65625	1	0	0	1	1	0	0	1
0.65000	1	0	0	1	1	0	1	0
0.64375	1	0	0	1	1	0	1	1
0.63750	1	0	0	1	1	1	0	0
0.63125	1	0	0	1	1	1	0	1
0.62500	1	0	0	1	1	1	1	0
0.61875	1	0	0	1	1	1	1	1
0.61250	1	0	1	0	0	0	0	0
0.60625	1	0	1	0	0	0	0	1
0.60000	1	0	1	0	0	0	1	0
0.59375	1	0	1	0	0	0	1	1
0.58750	1	0	1	0	0	1	0	0
0.58125	1	0	1	0	0	1	0	1
0.57500	1	0	1	0	0	1	1	0
0.56875	1	0	1	0	0	1	1	1
0.56250	1	0	1	0	1	0	0	0
0.55625	1	0	1	0	1	0	0	1
0.55000	1	0	1	0	1	0	1	0
0.54375	1	0	1	0	1	0	1	1
0.53750	1	0	1	0	1	1	0	0
0.53125	1	0	1	0	1	1	0	1
0.52500	1	0	1	0	1	1	1	0
0.51875	1	0	1	0	1	1	1	1
0.51250	1	0	1	1	0	0	0	0
0.50625	1	0	1	1	0	0	0	1
0.50000	1	0	1	1	0	0	1	0
OFF	1	1	1	1	1	1	1	0
OFF	1	1	1	1	1	1	1	1

Table 9. I^{2}C Commands for the NCP4208

<table>
<tr><th>Cmd Code</th><th>R/W</th><th>Default</th><th>Description</th><th># Bytes</th><th>Comment</th></tr>
<tr><td>0x01</td><td>R/W</td><td>0x80</td><td>Operation</td><td>1</td><td>00xx xxxx – Immediate Off
01xx xxxx – Soft Off
1000 xxxx – On (slew rate set by soft−start) − Default
1001 01xx – Margin Low (Ignore Fault)
1001 10xx – Margin Low (Act on Fault)
1010 01xx – Margin High (Ignore Fault)
1010 10xx – Margin High (Act on Fault)</td></tr>
<tr><td>0x02</td><td>R/W</td><td>0x17</td><td>ON_OFF_Config</td><td>1</td><td>Configures how the controller is turned on and off.
<table>
<tr><th>Bit</th><th>Default</th><th>Comment</th></tr>
<tr><td>7:5</td><td>000</td><td>Reserved for Future Use</td></tr>
<tr><td>4</td><td>1</td><td>This bit is read only. Switching starts when commanded by the Control Pin and the Operation Command, as set in Bits 3:0.</td></tr>
<tr><td>3</td><td>0</td><td>0: Unit ignores OPERATION commands over the I^{2}C interface
1: Unit responds to OPERATION command, powerup may also depend upon Control input, as described in Bit 2</td></tr>
<tr><td>2</td><td>1</td><td>0: Unit ignores EN pin
1: Unit responds EN pin, powerup may also depend upon the Operation Register, as described for Bit 3</td></tr>
<tr><td>1</td><td>1</td><td>Control Pin polarity
0 = Active Low
1 = Active High</td></tr>
<tr><td>0</td><td>1</td><td>This bit is read only.
1: means that when the controller is disabled it will either immediately turn off or soft off (as set in the Operation Command)</td></tr>
</table></td></tr>
<tr><td>0x03</td><td>W</td><td>NA</td><td>Clear_Faults</td><td>0</td><td>Writing any value to this command code will clear all Status Bits immediately. The SMBus $\overline{\text{ALERT}}$ is deasserted on this command. If the fault is still present the fault bit shall immediately be asserted again.</td></tr>
<tr><td>0x10</td><td>R/W</td><td>0x00</td><td>Write Protect</td><td>1</td><td>The Write_Protect command is used to control writing to the I^{2}C device. There is also a lock bit in the Manufacture Specific Registers that once set will disable writes to all commands until the power to the NCP4208 is cycled.
<table>
<tr><th>Data Byte</th><th>Comment</th></tr>
<tr><td>1000 0000</td><td>Disables all writes except to the Write_Protect Command</td></tr>
<tr><td>0100 0000</td><td>Disables all writes except to the Write_Protect and Operation Commands</td></tr>
<tr><td>0010 0000</td><td>Disables all writes except to the Write_Protect, Operation, ON_OFF_Config and VOUT_COMMAND Commands</td></tr>
<tr><td>0000 0000</td><td>Enables writes to all commands</td></tr>
<tr><td>0001 0000</td><td>Disables all writes except to WRITE_PROTECT, PAGE and all MFR−SPECIFIC Commands</td></tr>
</table></td></tr>
<tr><td>0x19</td><td>R</td><td>0xB0</td><td>Capability</td><td>1</td><td>This command allows the host to get some information on the I^{2}C device.
<table>
<tr><th>Bit</th><th>Default</th><th>Comment</th></tr>
<tr><td>7</td><td>1</td><td>PEC (Packet Error Checking is supported)</td></tr>
<tr><td>6:5</td><td>01</td><td>Max supported bus speed is 400 kHz</td></tr>
<tr><td>4</td><td>1</td><td>NCP4208 has an SMBus $\overline{\text{ALERT}}$ pin and ARA is supported</td></tr>
<tr><td>3:0</td><td>000</td><td>Reserved for future use</td></tr>
</table></td></tr>
<tr><td>0x20</td><td>R</td><td>0x20</td><td>VOUT_MODE</td><td>1</td><td>The NCP4208 supports VID mode for programming the output voltage.</td></tr>
<tr><td>0x21</td><td>R/W</td><td>0x00</td><td>VOUT_COMMAND</td><td>2</td><td>Sets the output voltage using VID.</td></tr>
</table>

<table>
<tr><th>Cmd Code</th><th>R/W</th><th>Default</th><th>Description</th><th># Bytes</th><th colspan="4">Comment</th></tr>
<tr><td>0x25</td><td>R/W</td><td>0x0020</td><td>VOUT_MARGIN_HIGH</td><td>2</td><td colspan="4">Sets the output voltage when operation command is set to Margin High. Programmed in VID Mode.</td></tr>
<tr><td>0x26</td><td>R/W</td><td>0x00B2</td><td>VOUT_MARGIN_LOW</td><td>2</td><td colspan="4">Sets the output voltage when operation command is set to Margin Low. Programmed in VID Mode.</td></tr>
<tr><td>0x38</td><td>R/W</td><td>0x0001</td><td>IOUT_CAL_GAIN</td><td>2</td><td colspan="4">Sets the ratio of voltage sensed to current output. Scale is Linear and is expressed in 1/Ω</td></tr>
<tr><td>0x39</td><td>R/W</td><td>0x0000</td><td>IOUT_CAL_OFFSET</td><td>2</td><td colspan="4">This offset is used to null out any offsets in the output current sensing circuitry. Units are Amps</td></tr>
<tr><td>0x4A</td><td>R/W</td><td>0x0064</td><td>IOUT_OC_WARN_LIMIT</td><td>2</td><td colspan="4">This sets the high current limit. Once this limit is exceeded IOUT_OC_WARN_LIMIT bit is set in the Status_IOUT register and an $\overline{ALERT}$ is generated. This limit is set in Amps.</td></tr>
<tr><td>0x6A</td><td>R/W</td><td>0x012C</td><td>POUT_OP_WARN LIMIT</td><td>2</td><td colspan="4">This sets the output power over power warn limit. Once exceeded Bit 0 of the Status I_{OUT} Command gets set and the $\overline{ALERT}$ output gets asserted (if not masked)</td></tr>
<tr><td rowspan="9">0x78</td><td rowspan="9">R</td><td rowspan="9">0x00</td><td rowspan="9">STATUS BYTE</td><td rowspan="9">1</td><th>Bit</th><th>Name</th><th colspan="2">Description</th></tr>
<tr><td>7</td><td>BUSY</td><td colspan="2">A fault was declared because the NCP4208 was busy and unable to respond.</td></tr>
<tr><td>6</td><td>OFF</td><td colspan="2">This bit is set whenever the NCP4208 is not switching.</td></tr>
<tr><td>5</td><td>VOUT_OV</td><td colspan="2">This bit gets set whenever the NCP4208 goes into OVP mode.</td></tr>
<tr><td>4</td><td>IOUT_OC</td><td colspan="2">This bit gets set whenever the NCP4208 latches off due to an overcurrent event.</td></tr>
<tr><td>3</td><td>VIN_UV</td><td colspan="2">Not supported.</td></tr>
<tr><td>2</td><td>TEMP</td><td colspan="2">Not supported.</td></tr>
<tr><td>1</td><td>CML</td><td colspan="2">A Communications, memory or logic fault has occurred.</td></tr>
<tr><td>0</td><td>None of the Above</td><td colspan="2">A fault has occurred which is not one of the above.</td></tr>
<tr><td rowspan="10">0x79</td><td rowspan="10">R</td><td rowspan="10">0x0000</td><td rowspan="10">STATUS WORD</td><td rowspan="10">2</td><th>Byte</th><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>Low</td><td>7</td><td>Res</td><td>Reserved for future use.</td></tr>
<tr><td>Low</td><td>6</td><td>OFF</td><td>This bit is set whenever the NCP4208 is not switching.</td></tr>
<tr><td>Low</td><td>5</td><td>VOUT_OV</td><td>This bit gets set whenever the NCP4208 goes into OVP mode.</td></tr>
<tr><td>Low</td><td>4</td><td>IOUT_OC</td><td>This bit gets set whenever the NCP4208 latches off due to an overcurrent event.</td></tr>
<tr><td>Low</td><td>3</td><td>Res</td><td>Reserved for future use.</td></tr>
<tr><td>Low</td><td>2</td><td>TEMP</td><td>Not supported.</td></tr>
<tr><td>Low</td><td>1</td><td>CML</td><td>A Communications, memory or logic fault has occurred.</td></tr>
<tr><td>High</td><td>0</td><td>None of the Above</td><td>A fault has occurred which is not one of the above.</td></tr>
<tr><td>High</td><td>7</td><td>V_{OUT}</td><td>This bit gets set whenever the measured output voltage goes outside its power good limits or an OVP event has taken place, i.e. any bit in Status V_{OUT} is set.</td></tr>
<tr><td rowspan="3">0x79</td><td rowspan="3">R</td><td rowspan="3">0x0000</td><td rowspan="3">STATUS WORD</td><td rowspan="3">2</td><th>Byte</th><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>High</td><td>6</td><td>I_{OUT}/P_{OUT}</td><td>This bit gets set whenever the measured output current or power exceeds its warning limit or goes into OCP. i.e. any bit in Status I_{OUT} is set.</td></tr>
<tr><td>High</td><td>5</td><td>INPUT</td><td>Not supported.</td></tr>
</table>

Cmd Code	R/W	Default	Description	# Bytes	Comment			
					High	4	MFR	A manufacturer specific warning or fault has occurred.
					High	3	$\overline{\text{POWER\_GOOD}}$	The Power Good signal is deasserted. Same as PowerGood in General Status.
					High	2	Res	Reserved for future use.
					High	1	OTHER	A Status bit in Status Other is asserted.
					High	0	Res	Reserved for future use.
0x7A	R	0x00	STATUS VOUT	1	**Bit**	**Name**	**Description**	
					7	Res	Not supported.	
					6	VOUT_ OVER VOLTAGE WARNING	This bit gets set whenever the measured output voltage goes above its powergood limit.	
					5	VOUT_ UNDER VOLTAGE WARNING	This bit gets set whenever the measured output voltage goes below its powergood limit.	
					4	Res	Reserved for future use.	
					3	VOUT_MAX Warning	Not supported, Can't program an output greater than MAX VID as there are no bits to program it.	
					2	Res	Not supported.	
					1	Res	Not supported.	
					0	Res	Not supported.	
0x7B	R	0x00	STATUS IOUT	1	**Bit**	**Name**	**Description**	
					7	I_{OUT} Overcurrent	This bit gets set if the NCP4208 latches off due to an OCP Event.	
					6	Res	Reserved for future use.	
					5	I_{OUT} Overcurrent Warning	This bit gets set if I_{OUT} exceeds its programmed high warning limit.	
					4	Res	Reserved for future use.	
					3	Res	Reserved for future use.	
					2	Res	Reserved for future use.	
					1	Res	Not supported.	
					0	P_{OUT} Over Power Warning Fault	This bit gets set if the measured P_{OUT} exceeds the Warn Limit.	
0x7E	R	0x00	STATUS CML	1	**Bit**	**Desc.**	**Name**	
					7	Supported	Invalid or Unsupported Command Received	
					6	Supported	Invalid or Unsupported Data Received	
					5	Supported	PEC Failed	
					4	Not supported	Memory Fault Detected	
					3	Not supported	Processor Fault Detected	
					2	Supported	Reserved	
					1	Supported	A communication fault other than the ones listed has occurred	
					0	Not supported	Other memory or Logic Fault has occurred	

Cmd Code	R/W	Default	Description	# Bytes	Comment: Bit	Comment: Name	Comment: Description
0x80	R	0x00	STATUS_ALERT	1	**Bit**	**Name**	**Description**
					7	Res	Reserved for future use.
					6	Res	Reserved for future use.
					5	Res	Reserved for future use.
					4	Res	Reserved for future use.
					3	Res	Reserved for future use.
					2	V_{MON} WARN	Gets asserted when V_{MON} exceeds it programmed WARN limits.
					1	Res	Reserved for future use.
					0	Res	Reserved for future use.
0x8B	R	0x00	READ_VOUT	2	Readback output voltage. Voltage is read back in VID Mode		
0x8C	R	0x00	READ_IOUT	2	Readback output current. Current is read back in Linear Mode (Amps).		
0x96	R	0x00	READ_POUT	2	Readback Output Power, read back in Linear Mode in W's.		
0x99	R	0x41	MFR_ID	1			
0x9A	R	0x0208	MFR_MODEL	2			
0x9B	R	0x03	MFR_REVISION	1			

Table 10. Manufacturer Specific Command Codes for the NCP4208

Cmd Code	R/W	Default	Description	# Bytes	Comment: Bit	Comment: Name	Comment: Description
0xDO	R/W	0x00	Lock/Reset	1	**Bit**	**Name**	**Description**
					1	Reset	Resets all registers to their POR Value. Has no effect if Lock bit is set.
					0	Lock	Logic 1 locks all limit values to their current settings. Once this bit is set, all lockable registers become read−only and cannot be modified until the NCP4208 is powered down and powered up again. This prevents rogue programs such as viruses from modifying critical system limit settings. (Lockable).
0xD1	R/W	0x03	Mfr Config	1	**Bit**	**Name**	**Description**
					7:6	$\overline{\text{PSI}}$	These bits sets the number of phases turned on during PSI. 00 = CL set for 1 Phase (default) 01 = CL set for 2 Phases 10 = CL set for 3 Phases 11 = CL set for 1 Phase
					5	Res	Reserved for future use.
					4	$\overline{\text{ALERT}}$ Mode	1 = Comparator Mode. 0 = $\overline{\text{ALERT}}$ Mode.
					3	BUS_TO_EN	Bus Timeout Enable. When the BUS_TO_EN bit is set to 1, the I^2C Timeout feature is enabled. In this state if, at any point during an I^2C transaction involving the NCP4208, activity ceases for more than 35 ms, the NCP4208 assumes the bus is locked and releases the bus. This allows the NCP4208 to be used with I^2C controllers that cannot handle I^2C timeouts. (Lockable).
					2	Res	Reserved for future use.
					1	$\overline{\text{ALERT}}$_EN	Enable the $\overline{\text{ALERT}}$ pin.
					0	ENABLE_ MONITOR	When the ENABLE_MONITOR bit is set to 1, the NCP4208 starts conversions with the ADC and monitors the voltages and temperatures.

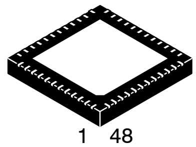
<table>
<tr><th>Cmd Code</th><th>R/W</th><th>Default</th><th>Description</th><th># Bytes</th><th colspan="3">Comment</th></tr>
<tr><td rowspan="6">0xD2</td><td rowspan="6">R/W</td><td rowspan="6">0x72</td><td rowspan="6">VR Config. 1A</td><td rowspan="6">1</td><td>Bit</td><td>Name</td><td>Description</td></tr>
<tr><td>6:4</td><td>Phase Enable Bits</td><td>000 = Phase 1
001 = Phase 2
010 = Phase 3
011 = Phase 4
100 = Phase 5
101 = Phase 6
110 = Phase 7
111 = Phase 8</td></tr>
<tr><td>3</td><td>VID_EN</td><td>When the VID_EN bit is set to 1, the VID code in the VOUT_COMMAND register sets the output voltage. When VID_EN is set to 0, the output voltage follows the VID input pins.</td></tr>
<tr><td>2</td><td>LOOP_EN</td><td>When the LOOP_EN bit is set to 1 in both registers, the control loop test function is enabled. This allows measurement of the control loop AC gain and phase response with appropriate instrumentation. The control loop signal insertion pin is I_{MON}. The control loop output pin is COMP.</td></tr>
<tr><td>1</td><td>CLIM_EN</td><td>When CLIM_EN is set to 1, the current limit time out latchoff functions normally. When this bit is set to 0 in both registers, the current limit latchoff is disabled. In this state, the part can be in current limit indefinitely.</td></tr>
<tr><td>0</td><td>Res</td><td>Reserved for future use.</td></tr>
<tr><td>0xD3</td><td>R/W</td><td>0x72</td><td>VR Config. 1B</td><td>1</td><td colspan="3">This register is for security reasons. It has the same format as register 0xD2. Bits need to be set in both registers for the function to take effect.</td></tr>
<tr><td>0xD4</td><td>R/W</td><td>0x03</td><td>Ton Delay</td><td>1</td><td colspan="3"></td></tr>
<tr><td>0xD5</td><td>R/W</td><td>0x02</td><td>Ton Rise</td><td>1</td><td colspan="3"></td></tr>
<tr><td>0xD6</td><td>R/W</td><td>0x01</td><td>Ton Transition</td><td>1</td><td colspan="3"></td></tr>
<tr><td>0xD7</td><td>R</td><td>0x00</td><td>V_{MON} Voltage</td><td>2</td><td colspan="3">This is a 16 bit value that reports back the voltage measured between FB and FBRTN</td></tr>
<tr><td>0xD8</td><td>R</td><td>0x00</td><td>EN/VTT Voltage</td><td>2</td><td colspan="3">This is a 16 bit value that reports back the voltage on the VTT Pin.</td></tr>
<tr><td>0xDD</td><td>R/W</td><td>0x00</td><td>VOUT_CAL</td><td>1</td><td colspan="3">Offset Command Code for V_{OUT}, max ±200 mV</td></tr>
<tr><td>0xDE</td><td>R/W</td><td>0x10</td><td>Loadline Calibration</td><td>1</td><td colspan="3">This value sets the internal loadline attenuation DAC calibration value. The maximum loadline is controlled externally by setting the gain of the current sense amplifier as explained in the applications section. This maximum loadline can then be adjusted from 100% to 0% in 30 steps. Each LSB represents a 3.226% change in the load line.
00000 = No Load Line
10000 = 51.6% of external load line
11111 = 100% of external Loadline</td></tr>
<tr><td>0xDF</td><td>R/W</td><td>0x00</td><td>Loadline Set</td><td>1</td><td colspan="3">This value sets the internal loadline attenuation DAC value. The maximum loadline is controlled externally by setting the gain of the current sense amplifier as explained in the applications section. This maximum loadline can then be adjusted from 100% to 0% in 30 steps. Each LSB represents a 3.226% change in the load line.
00000 = No Load Line
10000 = 51.6% of external load line
11111 = 100% of external load Line</td></tr>
<tr><td>0xE0</td><td>R/W</td><td>0x00</td><td>PWRGD Hi Threshold</td><td>1</td><td colspan="3">This value sets the PWRGD Hi Threshold and the CROWBAR Threshold:
Code = 00, PWRGD HI = 300 mV (default)
Code = 01, PWRGD HI = 250 mV
Code = 10, PWRGD HI = 200 mV
Code = 11, PWRGD HI = 150 mV</td></tr>
</table>

Cmd Code	R/W	Default	Description	# Bytes	Comment
0xE1	R/W	0x00	PWRGD Lo Threshold	1	This value sets the PWRGD Lo Threshold: Code = 000, PWRGD Lo = −500 mV (default) Code = 001, PWRGD Lo = −450 mV Code = 010, PWRGD Lo = −400 mV Code = 011, PWRGD Lo = −350 mV Code = 100, PWRGD Lo = −300 mV Code = 101, PWRGD Lo = −250 mV Code = 110, PWRGD Lo = −200 mV Code = 111, PWRGD Lo = −150 mV
0xE2	R/W	0x10	Current Limit Threshold	1	This value sets the internal current limit adjustment value. The default current limit is programmed using a resistor to ground on the LIMIT pin. The value of this register adjusts this value by a percentage between 50% and 146.7%. Each LSB represents a 3.33% change in the current limit threshold. 11111 = 146.7% of external current limit 10000 = 100% of external current limit (default) 00000 = 50% of external current limit
0xE3	R/W	0x10	Phase Bal SW1	1	These values adjust the gain of the internal phase balance amplifiers. The nominal gain is set to 5. These registers can adjust the gain by ±25% from 3.75 to 6.25. Code = 00000, Gain of 3.75 Code = 10000, Gain of 5 (default) Code = 11111, Gain of 6.25
0xE4	R/W	0x10	Phase Bal SW2	1	These values adjust the gain of the internal phase balance amplifiers. The nominal gain is set to 5. These registers can adjust the gain by ±25% from 3.75 to 6.25. Code = 00000, Gain of 3.75 Code = 10000, Gain of 5 (default) Code = 11111, Gain of 6.25
0xE5	R/W	0x10	Phase Bal SW3	1	These values adjust the gain of the internal phase balance amplifiers. The nominal gain is set to 5. These registers can adjust the gain by ±25% from 3.75 to 6.25. Code = 00000, Gain of 3.75 Code = 10000, Gain of 5 (default) Code = 11111, Gain of 6.25
0xE6	R/W	0x10	Phase Bal SW4	1	These values adjust the gain of the internal phase balance amplifiers. The nominal gain is set to 5. These registers can adjust the gain by ±25% from 3.75 to 6.25. Code = 00000, Gain of 3.75 Code = 10000, Gain of 5 (default) Code = 11111, Gain of 6.25
0xE7	R/W	0x10	Phase Bal SW5	1	These values adjust the gain of the internal phase balance amplifiers. The nominal gain is set to 5. These registers can adjust the gain by ±25% from 3.75 to 6.25. Code = 00000, Gain of 3.75 Code = 10000, Gain of 5 (default) Code = 11111, Gain of 6.25
0xE8	R/W	0x10	Phase Bal SW6	1	These values adjust the gain of the internal phase balance amplifiers. The nominal gain is set to 5. These registers can adjust the gain by ±25% from 3.75 to 6.25. Code = 00000, Gain of 3.75 Code = 10000, Gain of 5 (default) Code = 11111, Gain of 6.25
0xE9	R/W	0x10	Phase Bal SW7	1	These values adjust the gain of the internal phase balance amplifiers. The nominal gain is set to 5. These registers can adjust the gain by ±25% from 3.75 to 6.25. Code = 00000, Gain of 3.75 Code = 10000, Gain of 5 (default) Code = 11111, Gain of 6.25
0xEA	R/W	0x10	Phase Bal SW8	1	These values adjust the gain of the internal phase balance amplifiers. The nominal gain is set to 5. These registers can adjust the gain by ±25% from 3.75 to 6.25. Code = 00000, Gain of 3.75 Code = 10000, Gain of 5 (default) Code = 11111, Gain of 6.25

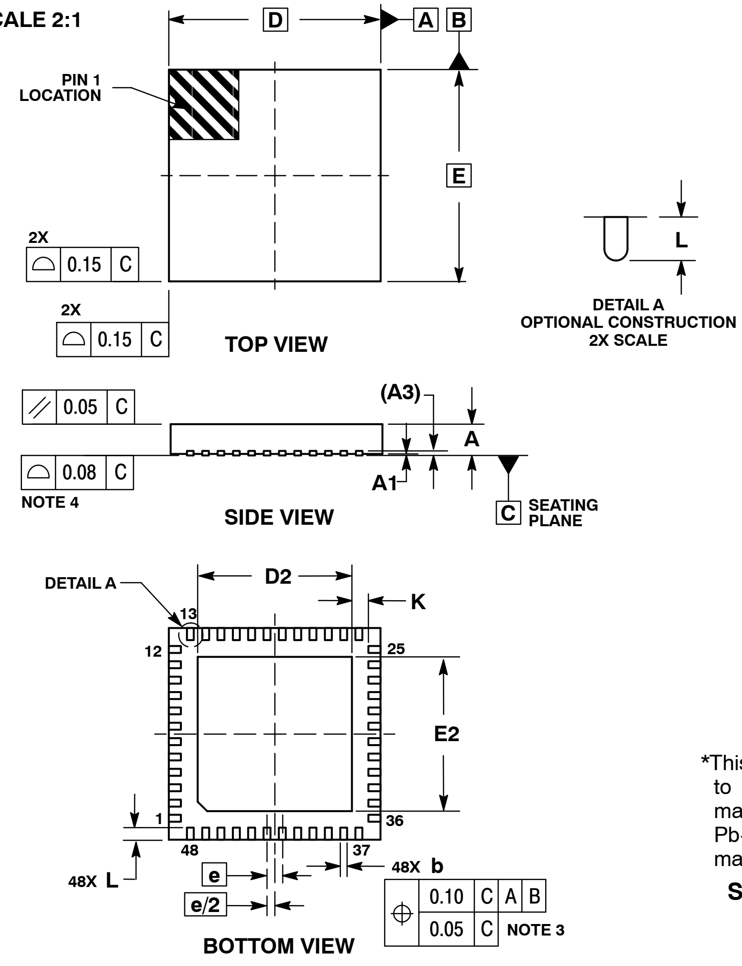
Cmd Code	R/W	Default	Description	# Bytes	Comment		
0xF1	R	0x00	ICPU MSB	1			
0xF6	R/W	0x0002	V_{MON} Warn Limit	2	V_{MON} Warn Limit		
0xF9	R/W	0x00	Mask $\overline{ALERT}$	1	**Bit**	**Name**	**Description**
					7	Mask V_{OUT}	Masks any $\overline{ALERT}$ caused by bits in Status V_{OUT} Register.
					6	Mask I_{OUT}	Masks any $\overline{ALERT}$ caused by bits in Status I_{OUT} Register.
					5	Res	Reserved
					4	Mask Temperature	Not Supported
					3	Mask CML	Masks any $\overline{ALERT}$ caused by bits in Status CML Register.
					2	V_{MON}	Masks any $\overline{ALERT}$ caused by V_{MON} exceeding its high or low limit.
					1	Res	Reserved
					0	Mask P_{OUT}	Masks any $\overline{ALERT}$ caused by P_{OUT} exceeding its programmed limit.
0xFA	R/W	0x00	Mask $\overline{FAULT}$	1	**Bit**	**Name**	**Description**
					7	Mask V_{OUT} $\overline{FAULT}$	Masks any $\overline{ALERT}$ caused by OVP.
					6	Mask I_{OUT} $\overline{FAULT}$	Masks any $\overline{ALERT}$ caused by OCP.
0xFB	R	0x10	General Status	1	**Bit**	**Name**	**Description**
					6	$\overline{ALERT}$	
					5	POWER GOOD	Replaced by Bit 3 of the Status Word Command
					4	RDY	
0xFC	R	0x00	Phase Status	1	**Bit**	**Name**	**Description**
					7	Phase 8	This bit is set to 1 when Phase 8 is enabled.
					6	Phase 7	This bit is set to 1 when Phase 7 is enabled.
					5	Phase 6	This bit is set to 1 when Phase 6 is enabled.
					4	Phase 5	This bit is set to 1 when Phase 5 is enabled.
					3	Phase 4	This bit is set to 1 when Phase 4 is enabled.
					2	Phase 3	This bit is set to 1 when Phase 3 is enabled.
					1	Phase 2	This bit is set to 1 when Phase 2 is enabled.
					0	Phase 1	This bit is set to 1 when Phase 1 is enabled

QFN48 7x7, 0.5P
CASE 485AJ−01
ISSUE O

DATE 27 APR 2007



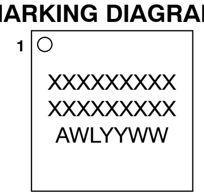
SCALE 2:1



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED ABETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	7.00 BSC	
D2	5.00	5.20
E	7.00 BSC	
E2	5.00	5.20
e	0.50 BSC	
K	0.20	---
L	0.30	0.50

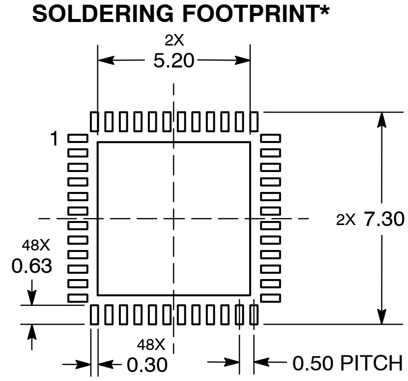
GENERIC MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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