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DC-DC Active Clamp Flyback PWM IC

Product Preview

NCP1568D

The NCP1568D is a highly integrated PWM controller designed to implement an active clamp flyback topology. NCP1568D employs a proprietary variable frequency algorithm to enable zero voltage switching (ZVS) of Super−Junction or GaN FETs across line, load, and output conditions. The ZVS feature increases power density of a power converter by increasing the operating frequency while achieving high efficiency. The Active Clamp Flyback (ACF) operation simplifies EMI filter design to avoid interference with other sensitive circuits in the system. The NCP1568D features a HV startup circuit, a strong low side driver, and a 5 V logic level driver for the active clamp FET. The NCP1568D is suitable for a variety of applications including power brick, industrial, telecom, lighting, and other applications where power density and efficiency are important requirements.

The NCP1568D also features multimode operation and transitions from ACF mode to Discontinuous Conduction Mode (DCM) to have outstanding light load operation. The NCP1568D further implements skip in standby mode, resulting in excellent standby power. The combination of flexible control scheme and user programmable features allow the use of NCP1568D with Super−Junction MOSFETs (Si) and Gallium Nitride (GaN) FETs.

Features

- Active Clamp Flyback Topology Aids in ZVS
- Proprietary Multi−Mode Operation to Enhance Efficiency at all Loads
- Proprietary Adaptive ZVS Algorithm Allows High Frequency Operation while Reducing EMI
- Adaptive Dead−Time Control Both Main and Active Clamp FETs
- Peak Current−Mode Control with built in Slope Compensation Options
- Flexible Control Scheme and Programmability Allow for Configuration with Either External Silicon or GaN FETs
- Programmable Optional Transition to DCM
- DCM Mode Frequency Foldback with Minimum Frequency Clamp
- Quiet Skip Eliminates Audible Noise
- 700 V Startup Circuit
- 0.85 A/1.5 A Source/Sink for Low Side
- 65 mA/150 mA Active Clamp Driver Output
- Programmable Frequency from 100 kHz to 1 MHz

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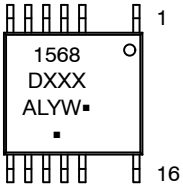
MARKING DIAGRAM

TSSOP−16
DT SUFFIX
CASE 948BW



1568D	=	Specific Device Code
XXX	=	Specific Variant (D00)
A	=	Assembly Location
L	=	Wafer Lot
Y	=	Year
W	=	Work Week
▪	=	Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

Features (Continued)

- Soft−Start Timer with 4 Options
- Dedicated FLT Pin Compatible with a Thermistor
- Adjustable Over Power Protection (OPP)
- Option for Auto−Recovery or Latched Faults
- Internal Thermal Shutdown

Applications

- USB Power Delivery
- Power Over Ethernet
- 1/32nd Brick
- Industrial Power Supplies

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

ORDERING INFORMATION

Device	LEB/DTMAX/ T_ZVSA (ns)	T_ZVSB (ns)	ACF FET Soft Start Time (ms)	ACF FET Soft Stop Time (ms)	Fixed Dead−Time from LDRV OFF to HDRV or ADRV ON (ns)	ATH Pin Mapping	Package	Shipping†
NCP1568DD00DBR2G	99/240/120	40	4	0.5	0	I = 1.92 E = 1	TSSOP−16 (Pb−Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

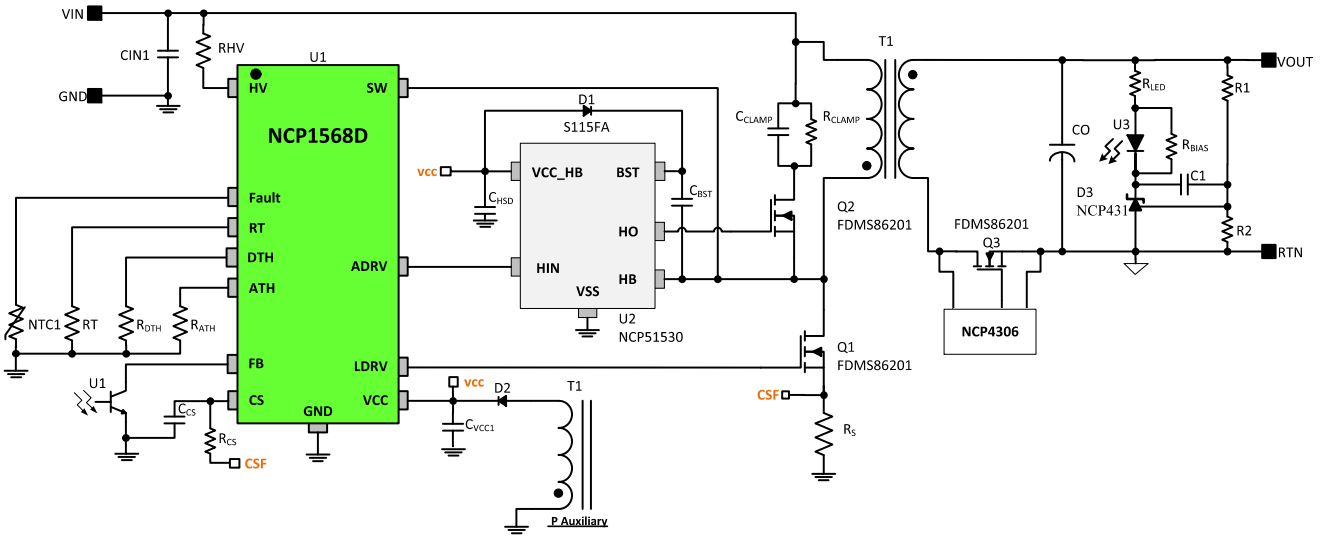


Figure 1. Typical Application for the NCP1568D Active Clamp Flyback

PIN DESCRIPTION

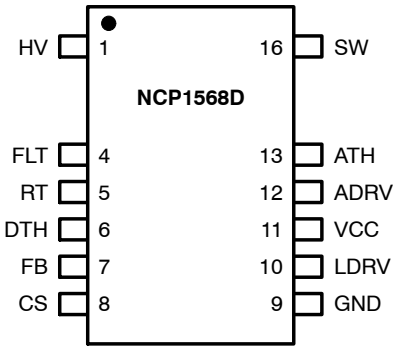


Figure 2. Pinout

Table 1. PIN FUNCTIONAL DESCRIPTION

Pin Out Controller Option	Name	Function
1	HV	Input to the HV startup circuit. A resistor can be placed in series with the HV pin to limit current in case of a short on the board. The recommended value for the resistor is 10 Ω.
2,3,14,15	–	Removed for creepage and clearance compliance.
4	FLT	The controller enters fault mode if the voltage of this pin is pulled above or below the fault thresholds.
5	RT	A resistor from the RT pin to ground sets the minimum frequency of the internal oscillator. A typical resistor of 100 kΩ sets 100 kHz and 20 kΩ sets 50 kHz.
6	DTH	A resistor to ground sets the ACF to DCM transition threshold with a precise 16 μA current source. Placing a 10 nF capacitor in parallel with the DTH setting resistor from this pin to ground reduces noise in the system. A typical value of resistor is 34.8 kΩ.
7	FB	Feedback input allows direct connection to an opto−coupler and is pulled up with an internal resistor and current source. Typical compensation will place a 120 pF capacitor as close to the pin as possible and a 34.8 kΩ in parallel.
8	CS	Current sense input. Placing a 47 pF capacitor to ground along with a resistor from the CS pin the low side FET source sense resistor connection typically 249 Ω will increases noise immunity? The value of the resistor can be adjusted for OPP Line compensation.
9	GND	Ground reference.
10	LDRV	Low−side drive output. Clamped to 12 V output.
11	V_{CC}	Supply input. At startup, an internal HV current charges the V_{CC} capacitor. Once the power stage is enabled, an auxiliary winding supplies current to the V_{CC} capacitor and the internal HV current source is turned−off. Placing a 10 nF capacitor in parallel with the ATH setting resistor from this pin to ground reduces noise in the system. A typical value of resistor is 47.5 kΩ.
12	ADRV	ADRV is the 5 V alternate ground based high side driver signal.
13	ATH	A resistor to ground sets the DCM to ACF transition threshold with a precise 10 μA current source.
16	SW	Connect to SW node used for adaptive dead−time control and ZVS based frequency modulation. Place a 2 kΩ resistor from the pin to the switch node to protect the device.

BLOCK DIAGRAM

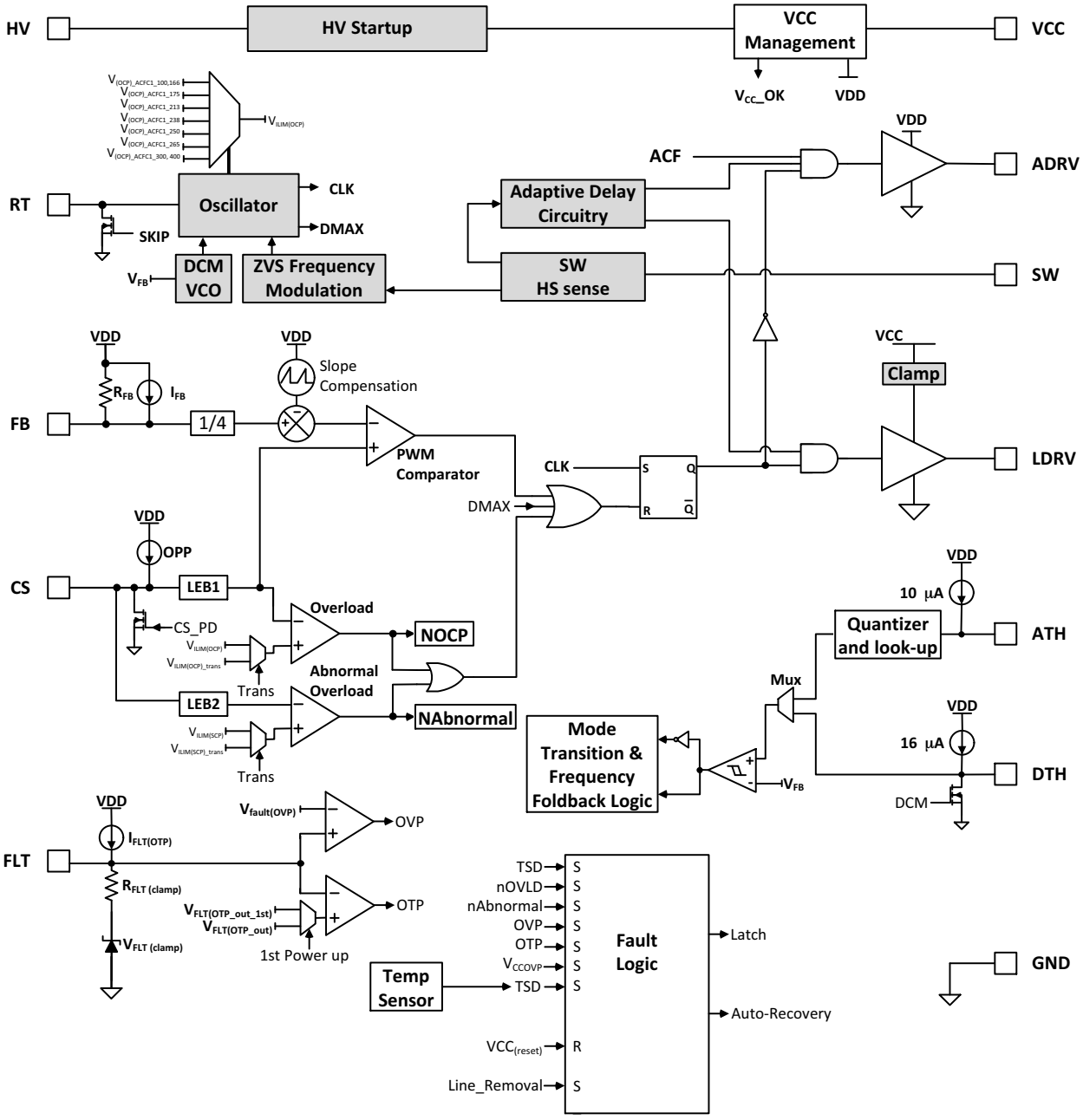


Figure 3. Block Diagram

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
High Voltage Startup Circuit Input Voltage	$V_{HV(MAX)}$	−0.3 to 700	V
High Voltage Startup Circuit Input Current	$I_{HV(MAX)}$	20	mA
Supply Input Voltage	$V_{CC(MAX)}$	−0.3 to 30	V
Supply Input Current	$I_{CC(MAX)}$	30	mA
Supply Input Voltage Slew Rate	dV_{CC}/dt	25	mV/μs
SW Pin to GND	$V_{SW(MAX)}$	−1 to 700	V
SW Pin Circuit Input Current	$I_{SW(MAX)}$	1	mA
ADRV Pin to GND	V_{ADRV}	−0.3 V to 5.5	V
ADRV Driver Maximum Current	$I_{ADRV(SRC)}$ $I_{ADRV(SNK)}$	130 190	mA
Low Side Driver Voltage (Note 1)	V_{DRV}	−0.3 V to $V_{DRV(high)}$	V
Maximum Input Voltage ATH, DTH, CS	$V_{ATH(MAX)}$	0.3 V to 5.5	V
Maximum Input Current ATH, DTH, CS	$I_{ATH(MAX)}$	10	mA
Maximum Input Voltage (Other Pins: FB, RT, FLT)	V_{MAX}	−0.3 to 30	V
Maximum Input Current (Other Pins: FB, RT, FLT)	I_{MAX}	27	mA
Operating Junction Temperature	T_J	−40 to 125	°C
Storage Temperature Range	T_{STG}	−60 to 150	°C
Power Dissipation (T_A = 25°C, 1 Oz Cu, 0.231 Sq Inch Printed Circuit Copper Clad) Plastic Package TSSOP16	$P_{D(MAX)}$	833	mW
Thermal Resistance, Junction to Ambient 1 Oz Cu Printed Circuit Copper Clad) Plastic Package TSSOP16	$R_{\theta JA}$	150	°C/W
ESD Capability Human Body Model per JEDEC Standard JESD22−A114F Except SW Pin Human Body Model per JEDEC Standard JESD22−A114F SW Pin Charge Device Model per JEDEC Standard JESD22−C101F. Latch−Up Protection per JEDEC Standard JESD78E		 2000 1500 1000 ±100	 V V V mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Maximum driver voltage is limited by the driver clamp voltage, $V_{DRV(high)}$, when V_{CC} exceeds the driver clamp voltage. Otherwise, the maximum driver voltage is V_{CC}.

Table 3. RECOMMENDED OPERATING CONDITIONS

Description	Symbol	Min	Typ	Max	Units
V_{CC} operating voltage	V_{CC}	10	16	27	V
Operating Junction temperature	Jc	−40		125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ELECTRICAL CHARACTERISTICS
(V_{CC} = 12 V, V_{HV} = 120 V, V_{FLT} = open, V_{FB} = 2 V, RT1= 33 kΩ, V_{CS} = 0 V, C_{VCC} = 100 nF, A_{DRV} = 100 pF, L_{DRV} = 1.5 nF for typical values T_J = 25°C, for min/max values, T_J is −40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
START−UP AND SUPPLY CIRCUITS						
Supply Voltage						V
Startup Threshold	V_{CC} increasing	$V_{CC(on)}$	14.5	15.2	15.9	
Minimum Operating Voltage After Turn−On	V_{CC} decreasing	$V_{CC(off)}$	8.5	9.0	9.9	
Operating Hysteresis	$V_{CC(on)}$ − $V_{CC(off)}$	$V_{CC(HYS)}$	5.5	–	–	
Internal Latch/Logic Reset Level	V_{CC} decreasing	$V_{CC(reset)}$	5.6	6.1	6.6	
V_{CC} Level at Which I_{start1} Transitions to I_{start2}	V_{CC} increasing, I_{HV} = I_{start1}	$V_{CC(inhibit)}$	0.27	0.57	1.03	
$V_{CC(off)}$ to Drive Turn−Off Timeout Delay	V_{CC} decreasing	$t_{delay(Vcc\_off)}$	–	42	100	μs
Startup Delay	Delay from $V_{CC(on)}$ to first LDRV pulse	$t_{delay(start)}$	8	34	60	μs
Start−Up Time	C_{VCC} = 0.47 μF, V_{CC} = 0 V to $V_{CC(on)}$	$t_{start-up}$	–	2.53	6.5	ms
Minimum HV Pin Voltage for Rated Start−Up Current Source	V_{CC} = $V_{CC(on)}$ − 0.5 V	$V_{HV(MIN)}$	–	–	25	V
Inhibit Current Sourced from V_{CC} Pin	V_{CC} = 0 V	I_{start1}	0.342	0.540	0.794	mA
Start−Up Current Sourced from V_{CC} Pin	V_{CC} = $V_{CC(on)}$ − 0.5 V	I_{start2}	2.5	3.67	4.4	mA
Start−Up Circuit Off−State Leakage Current	V_{hv} = 162.5 V	$I_{HV(off1)}$	–	–	23	μA
	V_{hv} = 325 V	$I_{HV(off2)}$	–	–	24	
	V_{hv} = 700 V	$I_{HV(off3)}$	–	–	25	
Switch Pin Off−State Leakage Current	FLT = 0 V					μA
	V_{hv} = 162 V	$I_{SW(off1)}$	–	–	1.5	
	V_{hv} = 325 V	$I_{SW(off2)}$	–	–	2	
	V_{hv} = 700 V	$I_{SW(off3)}$	–	–	4	
Switch Pin Active Current Draw	V_{ATH} = V_{DTH} = 0 V					μA
	V_{HV} = 162 V	$I_{SW(on1)}$	92	117	152	
	V_{HV} = 325 V	$I_{SW(on2)}$	92	118	153	
	V_{HV} = 700 V	$I_{SW(on3)}$	92	119	154	
Supply Current						mA
FLT PIN OTP	V_{CC} = $V_{CC(on)}$ − 0.5 V	I_{CC1A}	0.14	0.24	0.32	
FLT PIN OVP	V_{CC} = $V_{CC(on)}$ − 0.5 V	I_{CC1B}	0.14	0.25	0.32	
Latch Fault	V_{CC} = $V_{CC(on)}$ − 0.5 V	I_{CC1C}	0.14	0.22	0.32	
Skip Mode (Excluding FB & FLT Current)	V_{FB} = 0 V	I_{CC2}	0.18	0.26	0.35	
Operating Current 500 kHz	F_{sw} = 500 kHz, A_{DRV} = L_{DRV} =100 pF	I_{CC3}	2.25	4.00	6.17	
Operating Current 100 kHz	F_{sw} = 100 kHz, V_{CC} = 20 V	I_{CC4}	2.0	4.0	6.0	
Operating Current 500 kHz	F_{sw} = 500 kHz, V_{CC} = 10 V	I_{CC5}	9	13	16	
V_{CC} Overvoltage Protection Threshold	Latched event	$V_{CC(OVP)}$	26.6	27.8	29.2	V
V_{CC} Overvoltage Protection Timeout Delay		$t_{delay(Vcc\_OVP)}$	40	63	90	μs
SOFT−START						
Soft−Start Time	Ramp time for CS from 0 to I_{limit}	$t_{soft-start}$	6	7.5	9	ms
Forced DCM Time at the Beginning of Soft Start	RT = 33 kΩ (303 kHz)	t_{DCM_SS}	512	706	850	μs
Time at which FB is Compared to DTH Threshold	Time from the End of Soft Start to the ACF/DCM Assessment	t_{MODE_Sam}	13.5	16	18.5	ms
OSCILLATOR						
Minimum Oscillator Frequency in ACF Mode	VSW = 15 V, RT = 100 kΩ	$F_{osc\_ACF\_100}$	78	100	121	kHz
Minimum Oscillator Frequency in ACF Mode	VSW = 15 V, RT = 20 kΩ	$F_{osc\_ACF\_500}$	430	532	650	kHz

Table 4. ELECTRICAL CHARACTERISTICS (continued)
(V_{CC} = 12 V, V_{HV} = 120 V, V_{FLT} = open, V_{FB} = 2 V, RT1= 33 kΩ, V_{CS} = 0 V, C_{VCC} = 100 nF, A_{DRV} = 100 pF, L_{DRV} = 1.5 nF for typical values T_J = 25°C, for min/max values, T_J is −40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
OSCILLATOR						
Frequency Modulation Bounds	VSW = Modulated RT = 100 kΩ, 4.20 * F_{osc_ACF} RT = 42.2 kΩ, 4.20 * F_{osc_ACF} (Note 3)	 $F_{osc1\_LL\_ACF\_UB1}$ $F_{osc1\_LL\_ACF\_UB2}$	 310 700	 420 861	 530 1000	kHz
DCM Oscillator Frequency	RT = 20 kΩ, FB = DCM to ACF Trip Threshold −5 mV	$F_{osc\_DCM\_2}$	200	260	320	kHz
Maximum Duty Cycle	F_{osc}= 100 kHz, RT = 100 kΩ F_{osc} = 205 kHz ,RT = 49.9 kΩ F_{osc}= 500 kHz, RT = 20 kΩ, T_{min_OFF}	D_{Max_100} D_{Max_400} D_{Max_500}	53 60 53	75 79 69	96 92 88	%
Minimum Off Time for ADRV	Measured at 50% of Drive Voltage From Falling Edge to Rising Edge of LDRV	T_{min_OFF}	365	582	808	ns
TRANSITION MODE						
ACF to DCM Transition	ADRV LEM Soft Stop Time D00	$t_{ACF\_DCM\_Trans}$	1	0.506	1	ms
DCM to ACF Transition	ADRV LEM Soft Start Time D00	$t_{DCM\_ACF\_Trans1}$	3.5	4	4.7	ms
DCM to ACF Blanking Time after Transition	Time the DCM to ACF Comparator is Blanked	$t_{DCM\_ACF\_HOLD}$	0.9	1	1.1	ms
ACF to DCM Level Trip Time	Time the ACF to DCM Comparator must be High before Transition	$t_{ACF\_DCM\_HOLD}$	11	12	17	ms
Required DCM Cycles Before ACF	DCM Operation	NDCM	18			#
ATH FUNCTION						
Current Sourced From ATH	ATH = 2 V	I_{ATH}	9.4	10	10.5	μA
ATH BIN 0	50 mV	$_{ATH\_BIN0}$	1.00	1.04	1.07	–
ATH BIN 1	180 mV	$_{ATH\_BIN1}$	1.16	1.20	1.23	V
ATH BIN 2	220 mV	$_{ATH\_BIN2}$	1.326	1.36	1.394	V
ATH BIN 3	270 mV	$_{ATH\_BIN3}$	1.482	1.52	1.558	V
ATH BIN 4	330 mV	$_{ATH\_BIN4}$	1.638	1.68	1.722	V
ATH BIN 5	390 mV	$_{ATH\_BIN5}$	1.794	1.84	1.886	V
ATH BIN 6	460 mV	$_{ATH\_BIN6}$	1.95	2	2.05	V
ATH BIN 7	540 mV	$_{ATH\_BIN7}$	2.106	2.16	2.214	V
ATH BIN 8	630 mV	$_{ATH\_BIN8}$	2.262	2.32	2.378	V
ATH BIN 9	740 mV	$_{ATH\_BIN9}$	2.418	2.48	2.542	V
ATH BIN 10	870 mV	$_{ATH\_BIN10}$	2.574	2.64	2.706	V
ATH BIN 11	1.02 V	$_{ATH\_BIN11}$	2.73	2.8	2.87	V
ATH BIN 12	1.19 V	$_{ATH\_BIN12}$	2.886	2.96	3.034	V
ATH BIN 13	1.39 V	$_{ATH\_BIN13}$	3.042	3.12	3.198	V
ATH BIN 14	1.63 V	$_{ATH\_BIN14}$	3.198	3.28	3.362	V
DTH FUNCTION						
DTH Pin Pullup Current	RT = 100 kΩ	I_{DTH}	15.25	16.0	16.75	μA
DTH Trip Voltage	VDTH = 500 mV FB Decreasing VDTH = 1.5 V FB Decreasing VDTH = 3.0 V FB Decreasing	V_{FB_DTH1} V_{FB_DTH2} V_{FB_DTH3}	0.45 1.45 2.95	0.50 1.5 3.0	0.55 1.55 3.05	V

Table 4. ELECTRICAL CHARACTERISTICS (continued)
(V_{CC} = 12 V, V_{HV} = 120 V, V_{FLT} = open, V_{FB} = 2 V, RT1= 33 kΩ, V_{CS} = 0 V, C_{VCC} = 100 nF, A_{DRV} = 100 pF, L_{DRV} = 1.5 nF for typical values T_J = 25°C, for min/max values, T_J is −40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
SLOPE COMPENSATION						
Duty Cycle at which Ramp Compensation Begins	Both ACF and DCM Mode	D_{Slope_Start}	32	41.2	50	%
Slope of Compensating Ramp		S_{RAMP}	110	143	190	mV/μs
DCM MODE FREQUENCY FOLDBACK						
Feedback Voltage Below which CS Detected Peak Current is Frozen (at the FB Pin)		$V_{FB(Ipk\_freeze)\_0}$	740	792	850	mV
CS Pin Peak Current Floor Threshold Set when FB is Lower than $V_{FB(Ipk\_freeze)}$	RT = 100 kΩ RT = 33.3 kΩ RT = 20 kΩ	$V_{CS(Ipk\_freeze)\_0}$ $V_{CS(Ipk\_freeze)\_1}$ $V_{CS(Ipk\_freeze)\_2}$	160 280 390	220 349 475	270 410 560	mV
Minimum Oscillator Frequency	Operating Mode = DCM, V_{FB} = 400 mV	$F_{osc(min)}$	20.5	30	40	kHz
Oscillator Frequency in DCM Mode	RT = 20 kΩ FB = DCM to ACF Trip Threshold −5 mV	$F_{osc\_DCM\_2}$	220	260	305	kHz
Feedback Voltage at which Minimum Switching Frequency is Reached (at the FB Pin)	Fsw = $F_{osc(min)}$	$V_{Fosc(min)}$	370	400	440	mV
Feedback Voltage at which Skip Cycle Comparator Trips (at the FB Pin)	Feedback Falling	$V_{FB(skip)}$	370	400	440	mV
Skip Cycle Comparator Hysteresis	Feedback Rising (Positive)	$V_{FB(skip)\_hys}$	38	66	94	mV
Skip Wakeup Time	FB > ($V_{FB(skip)}$ + $V_{FB(skip)\_hys}$ + 100 mV)	T_{Skip_wake}	14	24	34	μs
FEEDBACK						
Open Pin Voltage		$V_{FB(open)}$	4.89	5.0	5.1	V
VFB to Internal Current Set Point Division Ratio	VFB = 4 V	K_{FB}	3.75	4.00	4.20	
Internal Pull−Up Resistor	V_{FB} = 0.4 V	R_{RFB_0}	16	20	24	kΩ
Internal Pull−Up Current	V_{FB} = 0.4 V	I_{FB_0}	83	99	114	μA
FLT PROTECTION						
Overvoltage Protection (OVP) Threshold	V_{FLT} Increasing	$V_{FLT\ (OVP)}$	2.9	3.0	3.1	V
OVP Detection Delay	V_{FLT} Increasing	$t_{delay(OVP)}$	21	35	49	μs
Over Temperature Protection (OTP) Threshold	V_{FLT} Decreasing (Note 2)	$V_{FLT(OTP\_in)}$	0.35	0.40	0.45	V
Over Temperature Protection Exiting Threshold	V_{FLT} Increasing (Note 2)	$V_{FLT(OTP\_out)}$	0.870	0.937	0.990	V
Over Temperature Protection Exiting Threshold on Startup	V_{FLT} Increasing with first V_{CC} Power on	$V_{FLT(OTP\_out\_1st)}$	0.370	0.418	0.470	V
OTP Detection Delay	V_{FLT} Decreasing	$t_{delay(OTP)}$	21	33	49	μs
OTP Pull−Up Current Source	V_{FLT} = $V_{FLT\ (OTP\_in)}$ + 0.2 V	$I_{FLT(OTP)}$	42.5	45.5	48.5	μA
FLT Input Clamp Voltage		$V_{FLT\ (clamp)}$	1.69	1.75	1.90	V
FLT Input Clamp Series Resistor		$R_{FLT\ (clamp)}$	1.26	1.58	1.90	kΩ
OVER POWER PROTECTION						
OPP Current GM	V_{HV} = 40 V V_{HV} = 120 V	HV_GM	112	188	265	nS
HV Update Time	Guaranteed by Design	T_{UPDATE}		30.7		ms

Table 4. ELECTRICAL CHARACTERISTICS (continued)
(V_{CC} = 12 V, V_{HV} = 120 V, V_{FLT} = open, V_{FB} = 2 V, RT1= 33 kΩ, V_{CS} = 0 V, C_{VCC} = 100 nF, A_{DRV} = 100 pF, L_{DRV} = 1.5 nF for typical values T_J = 25°C, for min/max values, T_J is −40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
CURRENT LIMIT PROTECTION						
Count of OCP Events Before Fault is Declared	$V_{CS} > V_{ILIM(OCP)}$	N_{OCP}		5		k #
Count of SCP Events Before Fault is Declared	$V_{CS} > V_{ILIM(SCP)}$	N_{SCP}	5	5	5	#
Restart Timer for Auto − Recovery		T_{auto_retry}	1460	1600	1755	ms
CS Pin Internal Pull−up Current	V_{CS} = 0.8 V	I_{bias}	0.7	1	1.3	μA
CURRENT SENSE						
Cycle by Cycle Current Limit Threshold Over Current Protection (OCP)	DCM threshold	$V_{ILIM(OCP)\_DCM}$	740	785	825	mV
Cycle by Cycle Current Limit Threshold ACF	RT = 100 kΩ					mV
	FSW = 100 kHz	$V_{(OCP)\_ACFC1\_100}$	740	785	825	
	FSW = 166 kHz	$V_{(OCP)\_ACFC1\_166}$	740	785	825	
	FSW = 175 kHz	$V_{(OCP)\_ACFC1\_175}$	710	750	795	
	FSW = 213 kHz	$V_{(OCP)\_ACFC1\_213}$	670	710	750	
	FSW = 238 kHz	$V_{(OCP)\_ACFC1\_238}$	635	680	725	
	FSW = 250 kHz	$V_{(OCP)\_ACFC1\_250}$	610	650	688	
	FSW = 263 kHz	$V_{(OCP)\_ACFC1\_263}$	580	620	660	
	FSW = 300 kHz	$V_{(OCP)\_ACFC1\_300}$	550	590	630	
	FSW = 400 kHz	$V_{(OCP)\_ACFC1\_400}$	550	590	630	
Cycle by Cycle Current Limit Threshold Over Current Protection (OCP) During LEM	In Transition Mode (ACF to DCM or DCM to ACF)	$V_{ILIM(OCP)\_Trans}$	1.12	1.19	1.26	V
Short Circuit Protection (SCP) Threshold	Both ACF and DCM	$V_{ILIM(SCP)}$	1.12	1.19	1.26	V
Short Circuit Protection (SCP) Threshold During LEM	In Transition Mode (ACF to DCM or DCM to ACF)	$VI_{LIM(SCP)\_Trans}$	1.31	1.391	1.48	V
OCP Leading Edge Blanking Delay	D00	$T_{LEB(OCP)0}$		195 121	230 141	ns
SCP Leading Edge Blanking Delay	D00	$T_{LEB(SCP)0}$		38	83	ns
OCP Propagation Delay	CS ramped from 0 to 1 V at dv/dt = 20 V/μs to LDRV 8.5 V falling edge	$T_{PROP(OCP)}$		38	78	ns
SCP Propagation Delay	CS ramped from 0 to 1.6 V at dv/dt = 20 V/μs to LDRV 8.5 V falling edge	$T_{PROP(SCP)}$		43	78	ns
CS Switch Discharge Resistance	Measured with 5 mA Pull Up Current	$R_{DS(ON)\_CS}$			80	Ω
DEAD TIME MANAGEMENT IN ACF MODE						
Resonant Mode to Energy Storage Voltage Threshold	Falling Edge of SW Pin Voltage	$D_{T\_R\_E\_VTH}$	8	9.6	10.7	V
Energy Storage to Resonant Mode Voltage Threshold	Rising Edge of SW Pin Voltage	$D_{T\_E\_R\_VTH}$	9	9.6	11	V
Dead Time from Energy Storage to Resonant Mode	$V_{SW} > D_{T\_E\_R\_VTH}$ to ADRV 2.5 V	$D_{T\_E\_R1}$	20	46	76	ns
Maximum Dead Time (Timer Starts at ADRV Falling Edge and is Reset when $D_{T\_R\_E}$ Expires)	D00	$D_{T\_Max\_1}$	229	276	320	ns
ZVS Reference Time for Frequency Modulation (Timer Starts at ADRV Falling Edge and is Reset when D_{T_Max})	D00	$T_{\_ZVS\_1}$		160		ns

Table 4. ELECTRICAL CHARACTERISTICS (continued)
(V_{CC} = 12 V, V_{HV} = 120 V, V_{FLT} = open, V_{FB} = 2 V, RT1= 33 kΩ, V_{CS} = 0 V, C_{VCC} = 100 nF, A_{DRV} = 100 pF, L_{DRV} = 1.5 nF for typical values T_J = 25°C, for min/max values, T_J is −40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
LOW SIDE DRIVER						
LDRV Rise Time	V_{LDRV} = 2.4 V to 8.5 V V_{CC} = $V_{CC(off)}$ + 0.5 V V_{CC} = 18 V	 T_{LS_rise} $T_{LS\_rise(Clamp)}$	 2 2	 10.7 10.6	 20 20	ns
LDRV Fall Time	V_{LDRV} = 8.5 V to 2.4 V V_{CC} = $V_{CC(off)}$ + 0.5 V V_{CC} = 18 V	 T_{LS_fall} $T_{LS\_fall(Clamp)}$	 1 1	 6.5 5.9	 15 15	ns
LDRV Source Current	V_{CC} = $V_{CC(off)}$ + 0.5 V V_{CC} = 18 V	I_{LS_src}		0.855 0.847		A
LDRV Sink Current	V_{CC} = $V_{CC(off)}$ + 0.5 V V_{CC} = 18 V	I_{LS_snk}		1.41 1.55		A
LDRV Clamp Voltage	V_{CC} = 18 V, R_{DRV} = 10 kΩ	$V_{LDRV(Clamp)}$	10.5	11.75	12.6	V
ADRV						
ADRV Rise Time	V_{ADRV} = 1V to 3V with 920 pF Load	T_{ADRV_rise}	15	28.5	49	ns
ADRV Fall Time	V_{ADRV} = 3V to 1V with 920 pF Load	T_{ADRV_fall}	7	12.2	21	ns
ADRV Source Current	V_{ADRV} = 2.5 V	I_{ADRV_SRC}		65		mA
ADRV Sink Current	V_{ADRV} = 2.5 V	I_{ADRV_SNK}		150		mA
Minimum Pulse Width Allowed		MIN_{PW_GD}	196	234	280	ns
ADRV Clamp Voltage	R_{DRV} = 10 kΩ	$V_{ADRV(Clamp)}$	4.25	4.75	5.25	V
THERMAL SHUTDOWN						
Thermal Shutdown	Temperature Increasing	T_{SHDN}		150		°C
Thermal Shutdown Hysteresis	Temperature Decreasing	$T_{SHDN(HYS)}$		40		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. On first startup the $V_{FLT(OTP\_out)}$ is set to $V_{FLT(OTP\_out\_1st)}$. If the FLT voltage decreases below $V_{FLT(OTP\_out)}$ after the first soft start the $V_{FLT(OTP\_out)}$ changed to 900 mV.
3. Operating at switching frequencies beyond those specified in the data sheet may result in damage to the IC or system and functionality cannot be guaranteed.

Introduction

The NCP1568D implements an active clamp flyback converter utilizing current mode architecture where the main switch turn off event is dictated by the peak current. The NCP1568D is an ideal candidate for high frequency high density modules, open frame power supplies, Power Over Ethernet (POE) and many more applications. The NCP1568D incorporates advanced control and power management techniques as well as multimode operation to meet stringent regulatory requirements. The NCP1568D is also enhanced with non−dissipative overpower protection (OPP), and frequency modulation in both ACF and DCM mode of operation for optimized efficiency over the entire power range. The controller can meet low standby power requirements at light loads with a combination of burst mode operation and low current consumption.

High Voltage Startup

The NCP1568D integrates a high voltage startup circuit accessible through the HV pin. A low value resistor in series with the HV pin can be used to limit current in the event of a pin short or surge. The series resistance of the HV pin should not exceed 3 kΩ, as the function of line detection and HV startup will be hampered. A value of 10 Ω is recommended.

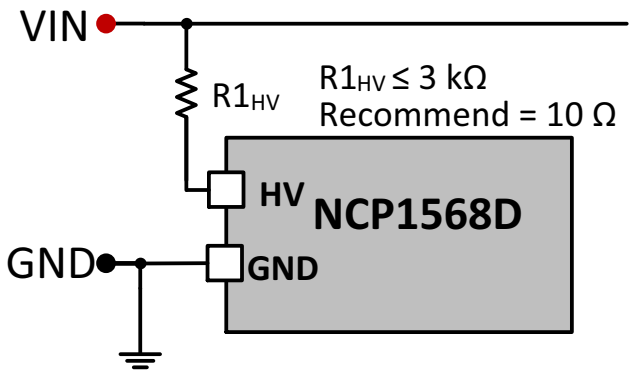


Figure 4. Typical HV Pin Connection

The HV startup regulator consists of constant current sources that supply current from the input voltage (V_{in}) to the supply a capacitor on the V_{CC} pin (C_{CC}). When the input voltage is greater than $V_{HV(MIN)}$, current is sourced from the HV pin to the V_{CC} pin at I_{start1}, typically 0.5 mA until the voltage on the V_{CC} pin exceeds $V_{CC(inhibit)}$, typically 700 mV. Once the $V_{CC(inhibit)}$ threshold has been exceeded, the startup circuit current increases to I_{start2}, typically 3.25 mA. The NCP1568D will continue to source I_{start2} from the HV pin to the V_{CC} pin when the voltage is below $V_{CC(on)}$ and the voltage on the HV pin is above $V_{HV(MIN)}$. I_{start2} is disabled if the V_{CC} pin falls below $V_{CC(inhibit)}$. In this condition, the startup current is reduced to I_{start1}. The internal high voltage startup circuits eliminate the need for external startup components. In addition, these current sources reduce no load power and increase the system efficiency as the HV startup circuit has negligible power consumption in the normal, light load, and standby operations.

Once the V_{CC} capacitor C_{CC} is charged to the startup threshold, $V_{CC(on)}$, the HV pin startup current sources are disabled the IC then checks for faults before entering soft start. If a fault is flagged the IC will take the appropriate action. If a fault remains for any length of time the V_{CC} energy will need to be replenished periodically. The startup current sources remain disabled until V_{CC} falls below the minimum operating voltage threshold, $V_{CC(off)}$ after the $tdelay_{(Vcc\_off)}$ expires. Once the threshold is reached, the current sources are again enabled to charge V_{CC} up to $V_{CC(on)}$. Figure 5 shows a typical startup sequence. If a fault is detected on the FLT pin, the part will continue to operate by providing current to the V_{CC} capacitor as needed in HVBC until all faults are cleared. Once the $V_{CC(on)}$ threshold is exceeded and no faults are flagged, the part will charge up to $V_{CC(on)}$ and the soft start sequence will begin.

A dedicated comparator monitors V_{CC} and latches the controller into a low power state if V_{CC} exceeds $V_{CC(OVP)}$ for $t_{delay(Vcc\_OVP)}$. To reset the OVP fault, the V_{CC} voltage must decrease to less than $V_{CC(reset)}$.

The C_{CC} provides power to the controller during power up. The capacitor must be sized such that a V_{CC} voltage greater than $V_{CC(off)}$ is maintained while the auxiliary supply voltage is ramping up. Otherwise, V_{CC} will collapse and the controller will turn off. The operating IC bias current, I_{CC4}, the high side driver current, and gate charge load at the low side and high side driver outputs must be considered to correctly size C_{CC}. The increase in current consumption due to external gate charge is calculated using Equation 2. Since the switching frequency is ramped from 31 kHz to the desired switching frequency, a trapezoidal shape is assumed for the frequency both in the DCM mode, the LEM operation, and ACF mode. The high side driver has no gate drive losses during DCM operation, thus the frequency is set to zero and the switch only has the average of the applied switching time from LEM and ACF operations as shown in Equation 1.

(eq. 1)

$$f_{SW} = \frac{\left(FSW_{MIN} + \frac{FSW_{DCM\_MAX} - FSW_{MIN}}{2}\right) \cdot T_{DCM} + \left(FSW_{DCM\_MAX} + \frac{FSW_{ACF\_MAX} - FSW_{DCM\_MAX}}{2}\right) \cdot (T_{SS} - T_{DCM})}{T_{SS}} \rightarrow$$

$$220.3\ kHz = \frac{\left(31.25\ kHz + \frac{50\ kHz - 31.25\ kHz}{2}\right) \cdot 695\ \mu s + \left(50\ kHz + \frac{420\ kHz - 50\ kHz}{2}\right) \cdot (8\ ms - 695\ \mu s)}{8\ ms}$$

Assuming a typical gate charge of 17 nC for the high side and low side MOSFETs.

$$I_{ICC(gate\_Charge\_Total)} = fsw\_ls \cdot Q_{g\_ls} + fsw\_hs \cdot Q_{g\_hs} \rightarrow \quad \text{(eq. 2)}$$
$$7.7\ mA = 218.1\ kHz \cdot 17 \cdot nC + 235\ kHz \cdot 17 \cdot nC \rightarrow$$

Equation 2 has f_{SW} as the average soft start switching frequency of the low side or high side MOSFET and Qg is the gate charge of the external MOSFETs.

Once the C_{CC} is charged to the startup threshold, a delay of $t_{delay(start)}$ is used to stabilize all internal power supplies and ensure biasing is up before operation and level setting can continue. After $t_{delay(start)}$ expires, the IC will not start switching until timers expire as shown in Figure 6.

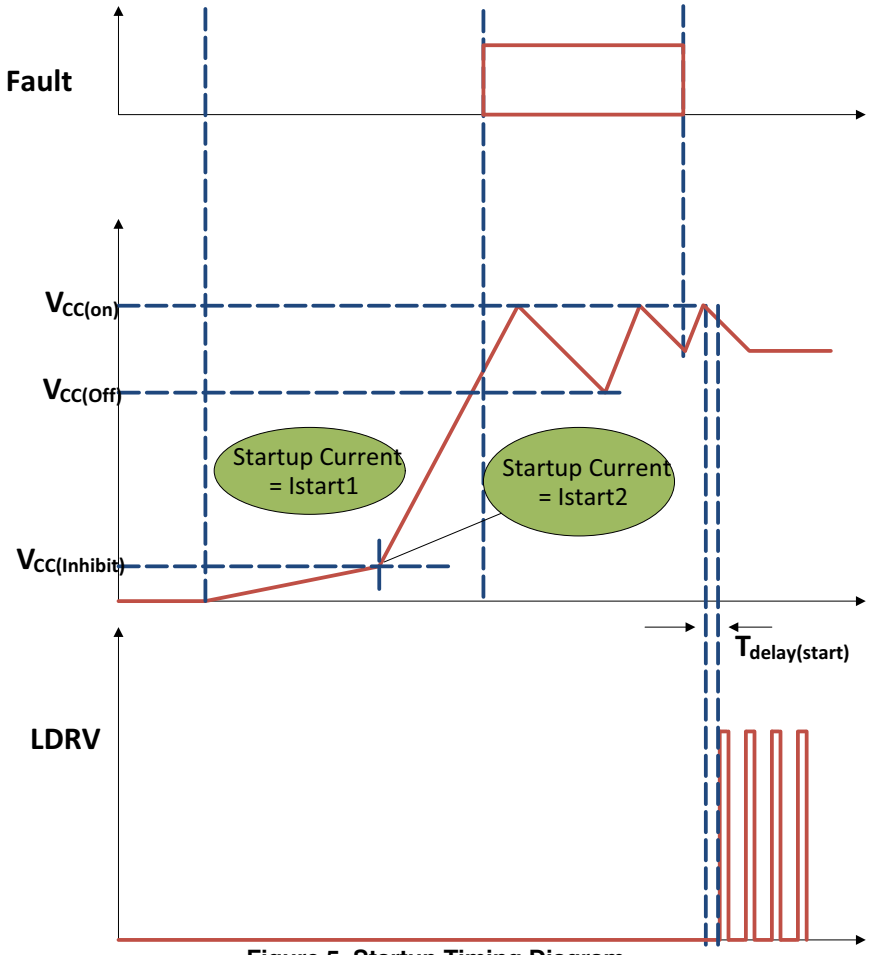


Figure 5. Startup Timing Diagram

The V_{CC} capacitor value must account for the startup delay time, soft start time, and all of the currents provided during that time. Equation 3 shows the calculated capacitance to soft start without the V_{CC} voltage dipping below the $V_{CC(OFF)}$ threshold. The capacitance value provided by the equation should be increased by 20% to allow for capacitor tolerances. Further increases may be made by the designer to account for operating temperature range.

$$C_{VCC\_MIN} = \frac{\left(T_{Delay(Start)}\right) \cdot \left(I_{CC1A} + I_{DRVQ}\right) + \left(T_{Soft\_start1} + T_{MODE\_SAM1}\right) \cdot \left(I_{CC3} + I_{DRV} + I_{CC(gate\ charge)}\right)}{V_{CCON} - V_{CCOFF}} \quad \text{(eq. 3)}$$

$$64.3\ \mu F = \frac{(34\ \mu s) \cdot (0.24\ mA + 0.250\ mA) + (8\ ms + 16\ ms) \cdot (4.0\ mA + 2.5\ mA + 7.85\ mA)}{15.2\ V - 9.9\ V}$$

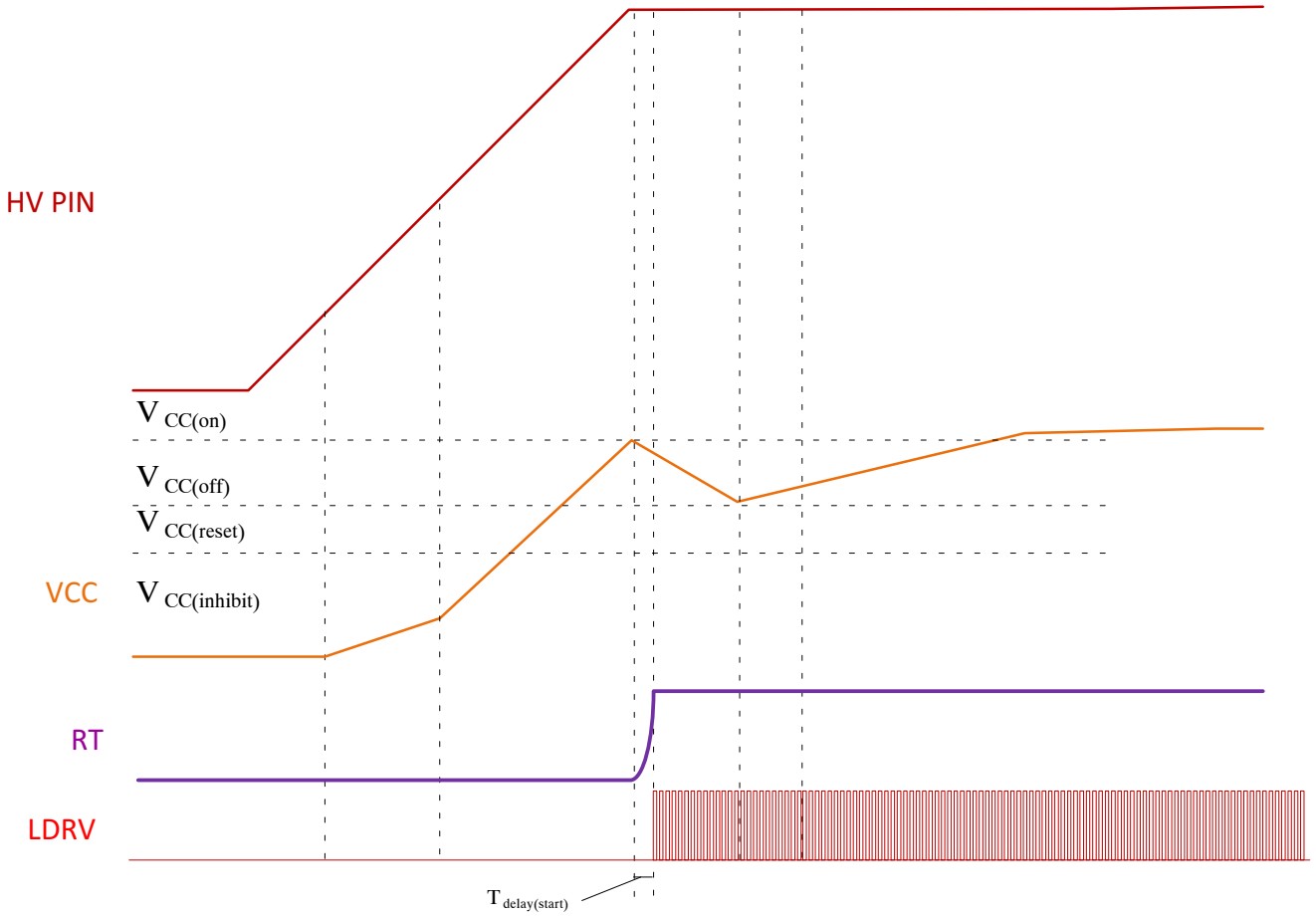


Figure 6. Normal Startup Timing Diagram and Delays

HV Currents and No load Operation

When considering no load operation, it is important to understand that the NCP1568D has a static loss on the HV pin due to off state leakage currents. The DC leakage currents on the pin are shown in the datasheet as $I_{HV(Off1)}$, $I_{HV(Off2)}$, and $I_{HV(Off3)}$.

Line Detection

The input voltage measured at the HV pin. The Over Power Protection (OPP) is changed based on the input voltage detection. Please refer to appropriate sections for more information. The controller compares a divided version of VHV to internal line select thresholds. The default power−up mode of the controller is low voltage. No line changes are applied until after the soft start has completed and soft start wait or the forced ACF period has ended to ensure a repeatable reliable soft start free from glitches. Once soft start wait has completed, the system is free to apply changes to parameters based on line voltage. The HV detector uses internal comparators and a divided down version of the HV voltage to digitally track the line as it increases and decreases.

PWM Architecture

The NCP1568D implements peak current mode control architecture for pulse width modulation. Peak current mode control simplifies the loop compensation and typically will result in a simple Type II compensator. With relatively simple compensation schemes, aggressive bandwidths can be achieved compared to a standard voltage mode control. Further, current mode control inherently provides current limiting while also providing a line feed forward, resulting in excellent line transient response. However, peak current mode control is susceptible to subharmonic oscillation for duty cycles greater than 50%. Subharmonic oscillation is characterized by alternating narrow and wide pulse widths. To prevent subharmonic oscillation, NCP1568D also features internal slope compensation.

The NCP1568D features multi−mode operation to optimize efficiency across line and load conditions. Below are the modes of operation:

1. Active Clamp Operation with Variable Frequency
2. Transition into and out of ACF Operation from DCM Operation
3. Discontinuous Conduction Mode with Frequency Foldback
4. Skip Mode

Multi Mode Algorithm

Multi mode algorithm is implemented in the NCP1568D to optimize the efficiency across load conditions. The magnetizing current is in Continuous Conduction Mode (CCM) in active clamp operation. Therefore, when the power supply is in standby condition, the active clamp flyback topology will work at high peak currents and the primary side clamp FET along with the main FET will form a synchronous buck boost structure with magnetizing current traversing both the first and the third quadrants.

If an IC were to remain in the ACF operation at a fixed frequency in all line and load conditions, the result would be high peak currents leading to high conduction losses, core losses, and copper losses while achieving ZVS as the load decreases. At light load, ZVS will not offset the three large loss contributors and the efficiency will be lower compared to DCM operation.

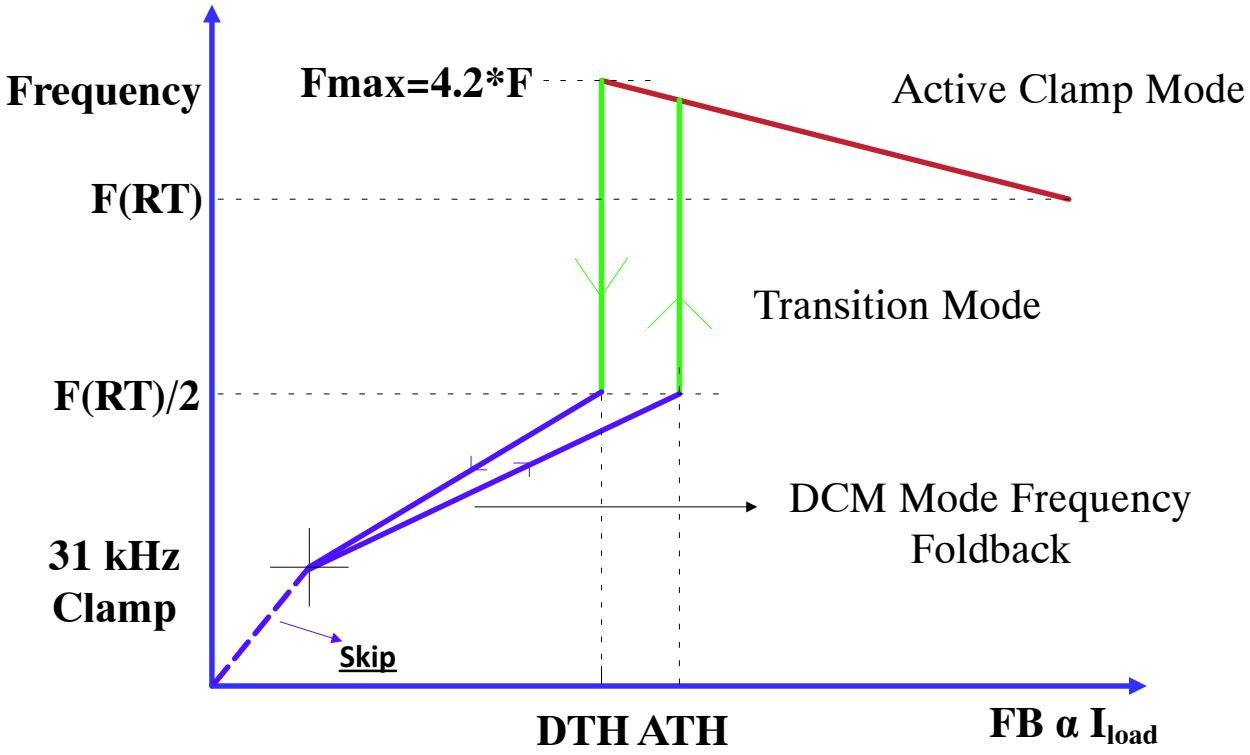


Figure 7. Frequency Transition from No Load to Full Load and DCM to ACF Operation

Oscillator

The RT resistor sets the minimum frequency of operation for the internal oscillator.

An internal amplifier forces 2 V on the RT pin and the current sourced from the resistor on the RT pin is used by the internal oscillator to set the minimum switching frequency.

The frequency set by the RT resistor follows Equation 4 noted below:

$$F_{OSC} = \frac{1}{RT \cdot 100\ pF} \rightarrow 100\ kHz = \frac{1}{100\ k\Omega \cdot 100\ pF} \quad \text{(eq. 4)}$$

where F_{OSC} is the frequency set by the RT resistor value

The frequency programmed at the RT pin sets the minimum ACF switching frequency. Typically, for an active clamp flyback topology, minimum frequency is selected to be at its lowest input voltage, lowest output voltage, and maximum load current. Figure 8 shows the RT resistor versus the oscillator frequency from 10 kΩ to 100 kΩ. The minimum RT resistor value is 10 kΩ.

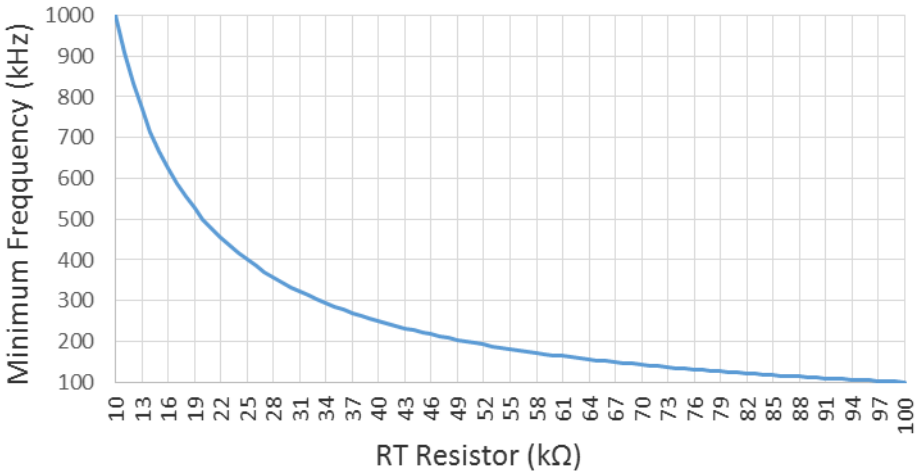


Figure 8. Minimum ACF Operating Oscillator Frequency vs. RT

Switching Cycle On and Off Time Restrictions

The NCP1568D has an internally set minimum off time of 590 ns that is always imposed in ACF mode. The minimum off time is to ensure that enough time remains in each switching cycle to fully execute a successful high side pulse. The minimum off time is constant, but the IC also has a maximum duty cycle of approximately 78% to allow for recharging of the high side driver boot capacitance and to avoid transformer saturation. The maximum duty cycle is therefore not constant, as the minimum off time must be maintained to continue ACF operation past a certain operating frequency. With a constant off time of 590 ns, the maximum duty cycle is governed by the minimum off time past 350 kHz. The resulting frequency versus duty cycle plot is shown in Figure 9. Equation 5 shows the maximum duty ratio.

(eq. 5)

$$\begin{bmatrix} \text{Duty\_Ratio} = 133\text{ns} * (\text{FSW}) + 73.7\% \\ \text{Duty\_Ratio} = 1 - \text{FSW} \cdot 0.59 \cdot \mu\text{s} \end{bmatrix} \begin{bmatrix} \text{FSW} < 350\ \text{kHz} \\ \text{FSW} > 350\ \text{kHz} \end{bmatrix}$$

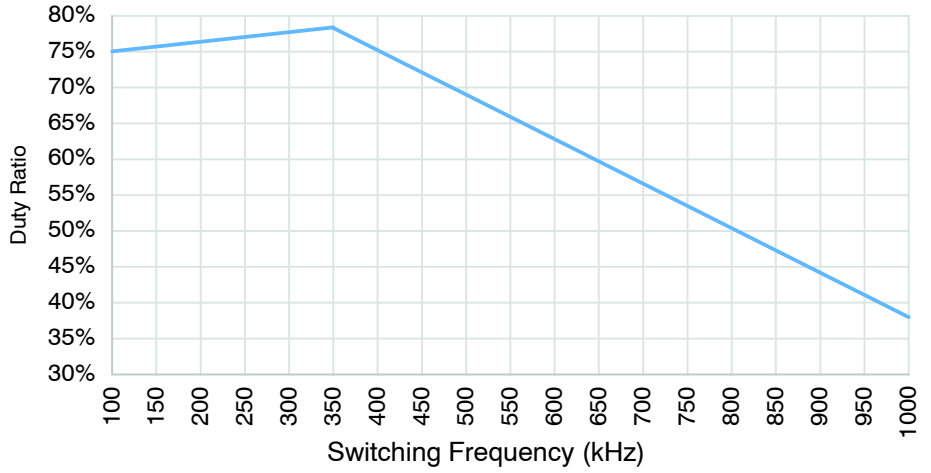


Figure 9. Maximum Duty Ratio vs. Switching Frequency

ACF Oscillator Operation

In order to minimize the power loss in ACF operation, as load and input voltage change, the frequency of operation needs to change such that additional circulating current is kept to a minimum. The negative current needed for ZVS is typically in the order of −0.5 A for super junction FETs. The current could be lower for wide bandgap semiconductors such as gallium nitride (GaN) as their COSS is typically lower. Keeping the negative magnetization current sufficient to achieve ZVS is accomplished digitally by adjusting the frequency of the oscillator until the SW node fall time is modulated to a predetermined dead time across line and load conditions.

A time reference T_ZVS is internally programmed in the NCP1568D and an error signal is accumulated based on the time the switch node takes to fall from the falling edge of ADRV to the sensing of ZVS at the switch node by the ZVS comparator. If the switch node decreases quickly and ZVS occurs before the reference time T_ZVS, then there is more than enough energy to reset the node and therefore the frequency of operation should be increased which effectively reduces the off time. The increased frequency will result in less energy available for resetting the switch node, and as such will result in less required on time for the low side switch and a smaller Δ IM. The smaller Δ IM results in fewer losses in the system. If the switch node ZVS occurs coincident with the time reference T_ZVS, no frequency adjustment is necessary. If the ZVS occurs after the T_ZVS, the frequency is too high and needs to be reduced to ensure good ZVS. Finally, if the ZVS never occurs and instead reaches a maximum allowable time limit (D_{T_Max}), the current switching cycle ends and the LDRV is driven on, but the frequency reduction will be applied to the following switching cycle.

The net result is that the duty ratio would be maintained, the load current would be supported, and the frequency would adjust with load to provide enough energy to achieve ZVS. The TZVS is composed of 2 internally programmable times T_ZVS_A and TZVS_B. T_ZVS_A is half of the D_{T_Max} time. The T_ZVS_A is a course adjustment to the total T_ZVS time. The T_ZVS_B is a fine adjustment to the total T_ZVS time. See part number decode for available options. T_ZVS it the addition of T_ZVS_A and T_ZVS_B as shown below.

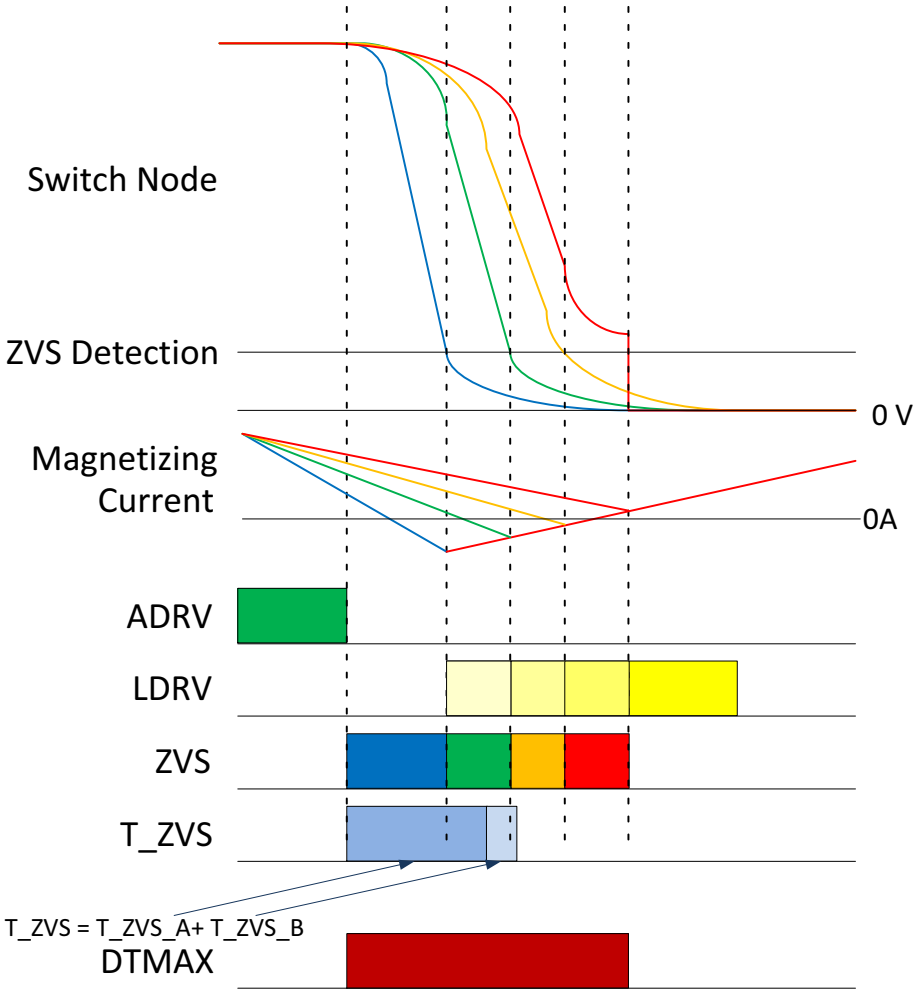


Figure 10. Time Referenced Digital Modulation of Operating Frequency Regulating the ZVS Point

DCM Oscillator Operation

In DCM mode of operation, the frequency is dependent on the DCM to ACF threshold setting and the FB voltage. The maximum oscillator frequency is 1/2 of the minimum ACF frequency set by the RT resistor. A frequency foldback proportional to the FB pin voltage is also implemented in the DCM mode. Please refer to the frequency foldback section for a description.

Frequency Foldback

In DCM operation, the frequency is the highest once the FB reaches a settable V_{ATH} threshold. The frequency of operation is reduced as FB voltage falls to its lowest point at the $V_{FB(skip)}$ skip threshold. Since the DCM to ACF threshold is programmable, the VCO must change slopes based on the selected V_{ATH} threshold as shown in Figure 11. In frequency foldback mode, the NCP1568D on time is set with the FB voltage and the peak current. The FB voltage also sets the frequency of operation from the $V_{TH\_DCM\_ACF}$ threshold to the $V_{FB(Ipk\_freeze)}$ threshold. Once the FB voltage reaches $V_{FB(Ipk\_freeze)}$ on the FB pin, the peak current floor is frozen to the $V_{CS(\ Ipk\_freeze)}$ value. The IC can produce a peak current that is greater than the $V_{CS(\ Ipk\_freeze)}$ if the PWM comparator requires a longer on time to satisfy the control loop. Freezing the peak current to a minimum value accelerates the slope of the frequency foldback. The peak current is frozen and the oscillator frequency is changed to maintain output voltage regulation. As the load decreases, the frequency will keep decreasing until it stops at the minimum frequency clamp of $F_{OSC(min)}$ 31 kHz. The minimum frequency occurs at the $V_{FB(skip)}$ threshold, typically at 400 mV on the FB pin. At $V_{FB(skip)}$ threshold, skip cycle operation is enabled.

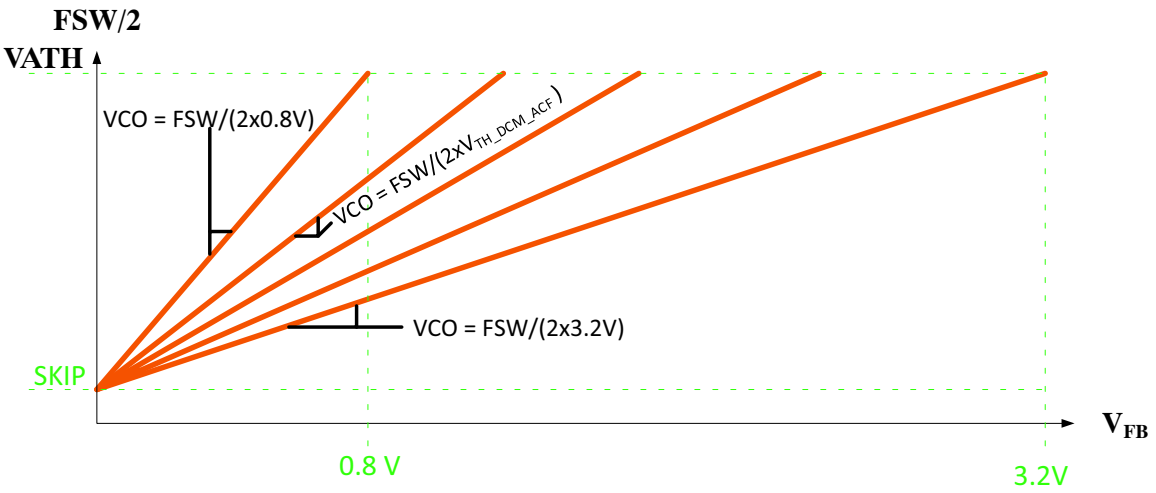


Figure 11. VCO Frequency Change with V_{ATH} Voltage Selection

DCM Minimum Frequency Clamp and Skip Mode

The minimum switching frequency clamp prevents the switching frequency from dropping below $F_{OSC(min)}$ (31 kHz typical). When the switching cycle is longer than 40 µs, a new switching cycle is initiated. Since the NCP1568D forces a minimum peak current and a minimum frequency, the power delivery cannot be continuously controlled to zero load. Instead, the circuit starts skipping pulses when the FB voltage drops below the skip level, $V_{FB(skip)}$, and recovers operation when V_{FB} exceeds $V_{FB(skip)} + V_{FB(skip)\_hys}$. The skip mode method provides an efficient method of control during light loads.

DCM TO ACF Transition (ADRV Soft Start)

Once all of the criteria to transition from DCM to ACF operation have been met, the NCP1568D soft starts the ADRV employing Leading Edge Modulation (LEM). The ADRV soft start slowly discharges the energy stored in the clamp capacitor in DCM operation to the output. During the ADRV soft start time, $T_{DCM\_ACF\_Trans}$, ADRV pulses will increase from a minimum of approximately 250 ns to 1−D in a controlled progression.

Figure 12 shows leading edge modulation of ADRV during the DCM to ACF transition. The secondary current shape starts to resemble that of resonant current during the LEM period and eventually resonant current can be seen throughout the 1−D cycle as the ADRV soft start finishes.

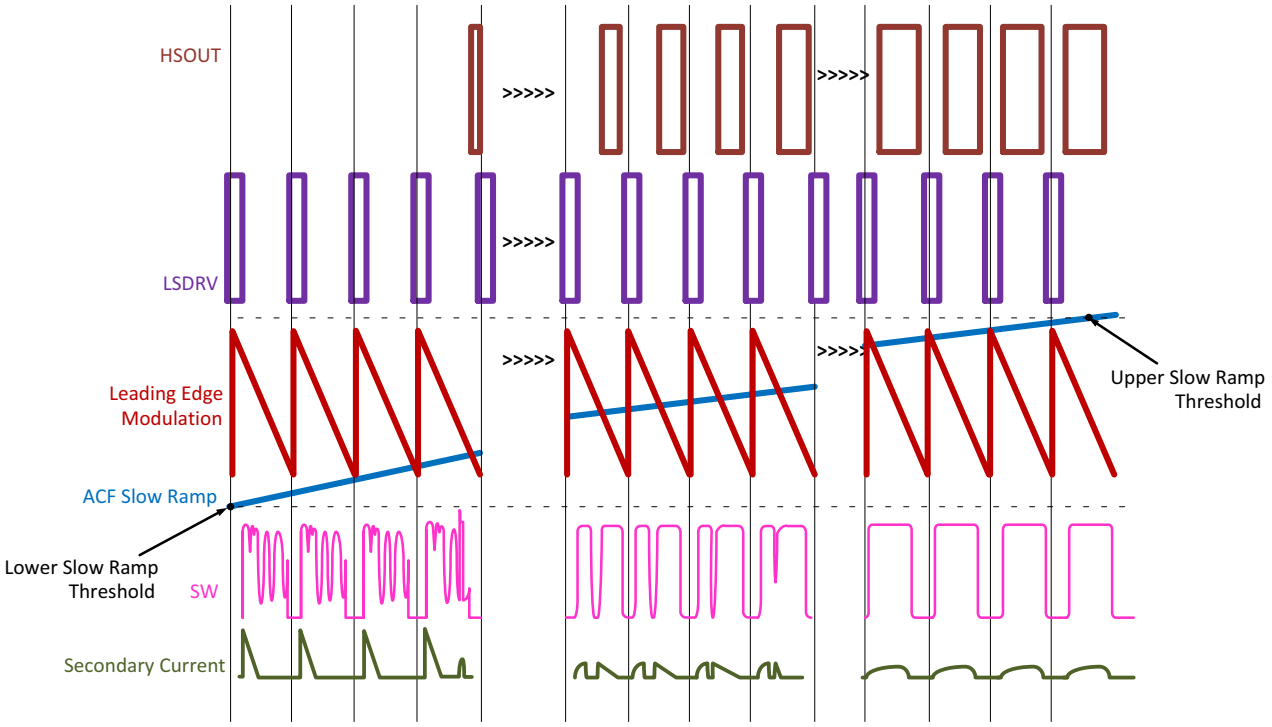


Figure 12. Leading Edge Modulation of ADRV During DCM to ACF Transition

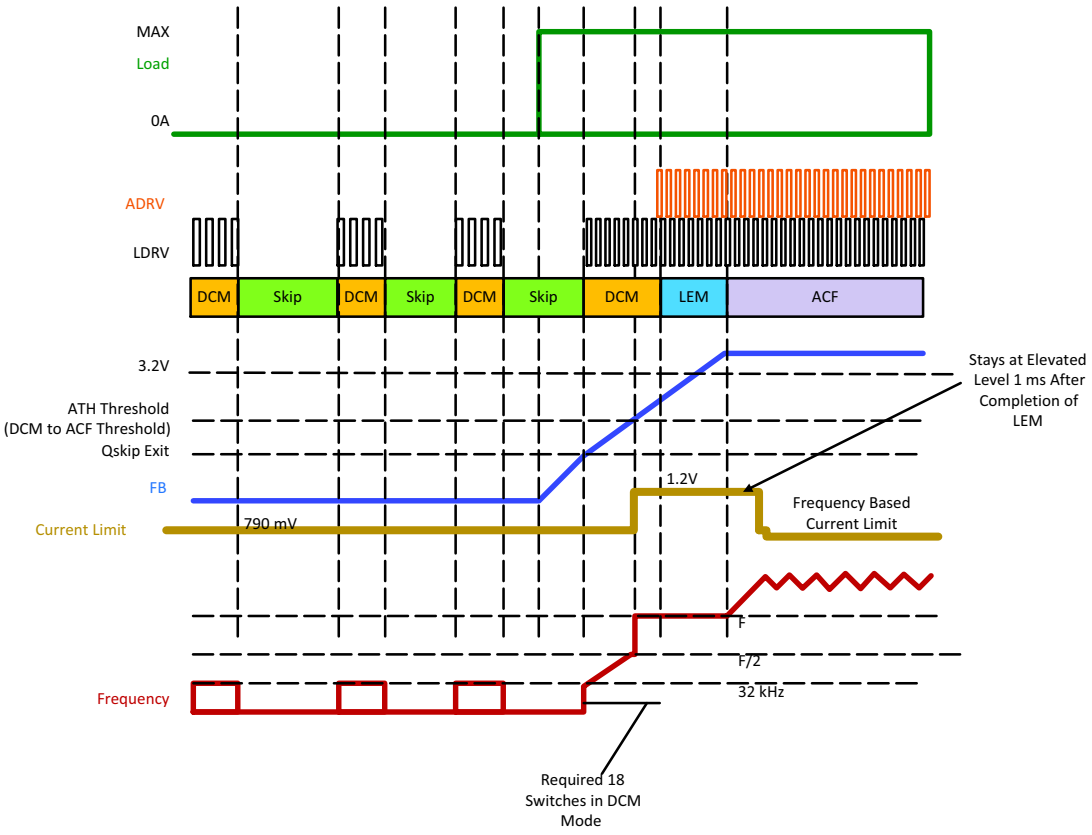


Figure 13. Typical Transition

Transition Hard Switch Avoidance

Before the high side switch begins the LEM process, the switch node demagnetizes and rings as a classic flyback would. During the start of LEM, the switch node demagnetization is interrupted by the switch node pulling up to the clamp capacitor voltage. The time the switch node is pulled up to the clamp capacitor voltage steadily increases and the demagnetization switch node signature continues to increase the amplitude of resonation. Either the LEM finishes with no ringing to ground and is in full ACF mode of operation, or the switch node is clamped on a falling edge ring to ground by the body diode of the low side FET. When the body diode of the low side FET is conducting, turning on the high side switch creates a disturbance to the system, drains the energy in the clamp capacitor, and causes large spikes on the primary and secondary side of the transformer. The NCP1568D has a proprietary algorithm to sense the switch node edges and predict the ideal times to turn on the high side switch.

ACF to DCM Transition (ADRV Soft Stop)

In ACF operation, if the FB voltage is below the externally set DTH for $T_{ACF\_DCM\_HOLD}$, then the system will start the transition from ACF switching to DCM switching using LEM. During the $T_{ACF\_DCM\_trans}$ time, the active clamp FET (ADRV) duty cycle is decreased in a controlled fashion over multiple cycles. At the same time, a non−linear frequency foldback to half the frequency ($1/2*F_{osc}$) set by the RT resistor is also implemented.

A leading edge modulation technique is employed to soft stop the active clamp FET. The soft stop time $T_{ACF\_DCM\_trans}$ is typically around 500 μs, a diagram of the soft stop is shown in Figure 14.

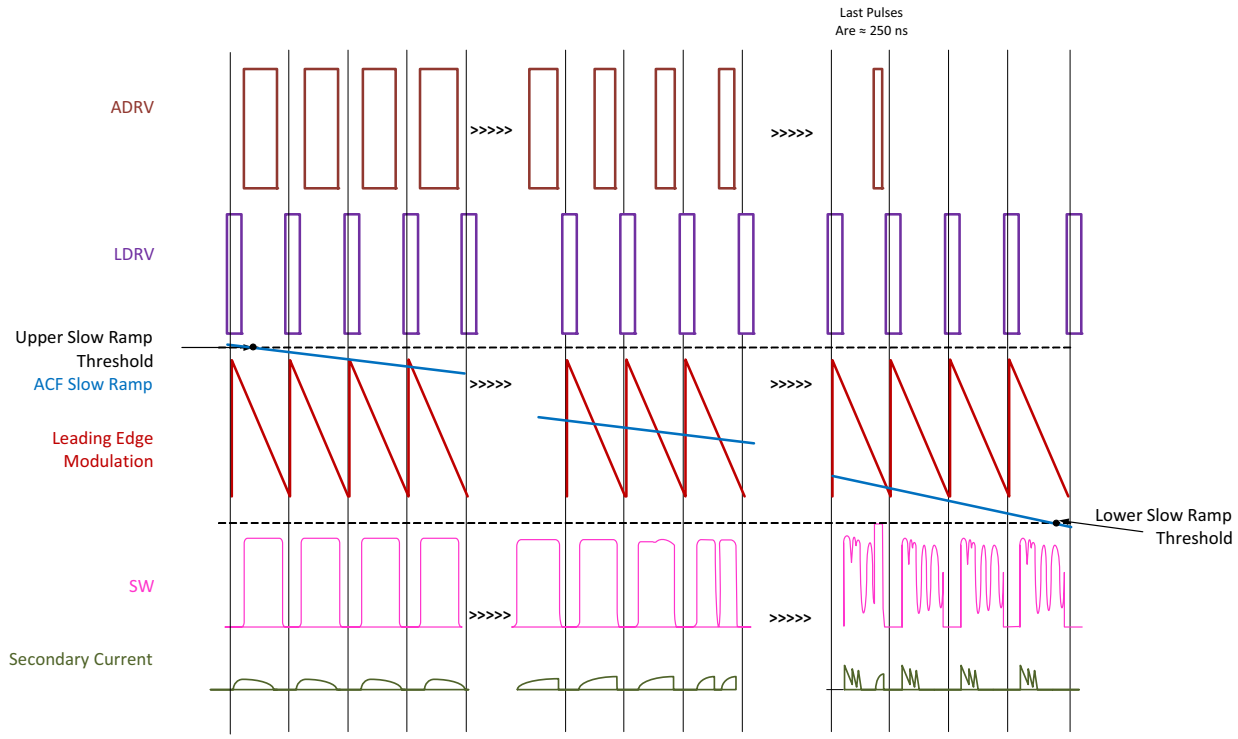


Figure 14. ACF to DCM Transition Waveforms

ATH Pin Functionality

The function of the ATH pin is to set the DCM to ACF threshold. The threshold is set with a fixed current and a resistor to create an analog voltage. The analog voltage is quantized into bins; each bin is mapped to a precise internal reference voltage which is compared against feedback to transition into ACF operation.

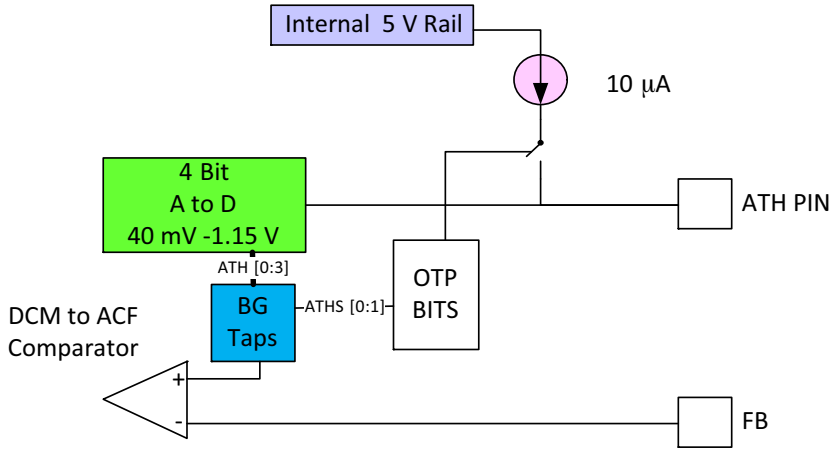


Figure 15. ATH Setting Threshold System Diagram

ATH Pin Turn On and Sourcing Current

The ATH pin current is sourced once V_{CC} exceeds the V_{CC}(on) threshold. The sourced current is 10 μA ± 5%. Current is sourced from the ATH pin during all normal operating conditions, DCM operation, ACF operation, and skip. Turn on timing for the ATH pin current source is shown in Figure 16 where the ATH pin current source turns on once $V_{CC(on)}$ is reached and remains on during DCM and ACF operation.

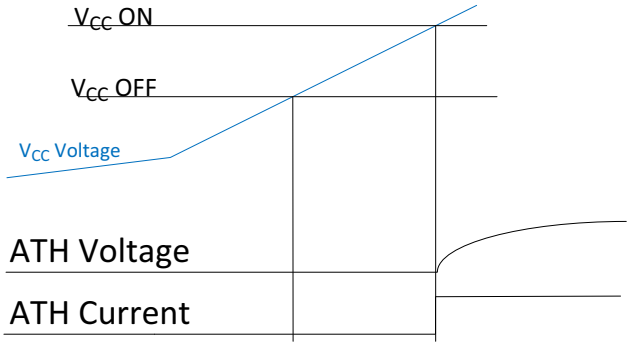


Figure 16. ATH Setting Threshold

Resistor Setting Range

Once a bin is selected, the selected bin maps to a set internal voltage. The voltage measured on the ATH pin only serves to select a digital bin and its tolerance does not affect the internally selected voltage. The mapped reference taps have a tolerance of approximately 2.5%. Table 5 includes the DCM to ACF binning thresholds and resistor map.

Table 5. ATH RESISTOR SET VALUES

R96 Resistor (kΩ)	Internal Reference for FB Trip Point (V)
161.2	3.28
139.6	3.12
118	2.96
102.2	2.8
86.4	2.64
74.8	2.48
63.2	2.32
53.4	2.16
46.4	2
39.2	1.84
33	1.68
27.4	1.52
22	1.36
18.2	1.2
8	1.04

DTH Pin Functionality

The DTH pin is a real time pin that is observed continuously once soft start has completed and forced ACF time (please refer to soft start section) has expired. Once V_{CC} has exceeded the V_{CC}(on) threshold, the DTH pin will begin sourcing 16 μA. The size of the capacitor placed on the ATH pin governs the delay the designer will see before the pin reaches its steady state voltage. A 100 nF capacitance is the standard recommended value for noise cancellation and timing. The resistance range that will be applied to the DTH pin can range from 0 Ω to 187.5 kΩ to set a voltage threshold between 0 V and 3 V. The most common anticipated ACF to DCM thresholds are shown in Figure 17. The DTH current source is turned off in DCM operation.

$$V_{DTH} = IDTH * RDTH$$

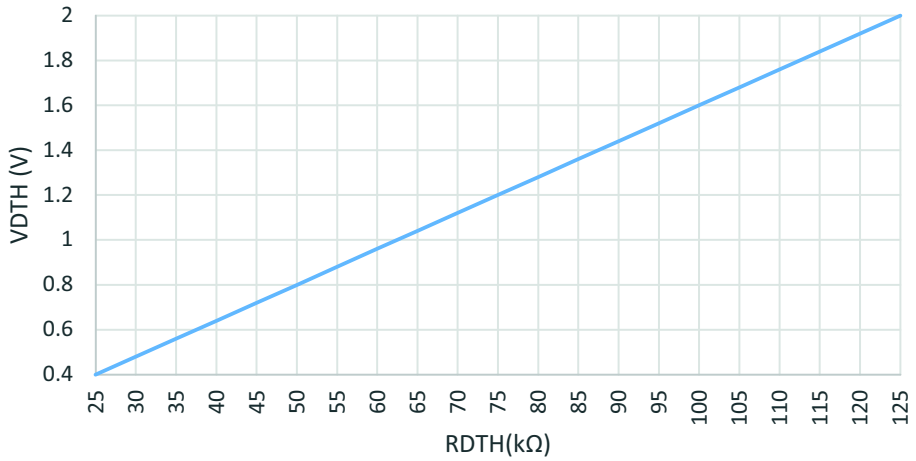


Figure 17. Setting Threshold for DTH PIN

Soft Start

The soft start of the NCP1568D is initiated once all of the criteria has been satisfied for the V_{CC} to reach $V_{CC(on)}$, no other faults are present, and $t_{delay(start)}$ has expired. Before the first pulses of the LDRV are initiated, the FB voltage is held high by the internal pull up current source and resistor tied to an internal 5 V source. During normal operation, the optocoupler and current sources regulate the FB node, but in soft start it is not regulated until the output voltage is greater than the secondary side reference voltage and the forward diode drop of the optocoupler. The IC will want to transition to ACF mode immediately on the first switching pulse, as the FB voltage will be higher than any threshold that can be set by the ATH pin. The IC's natural tendency is to transition to ACF operation when heavy loads are applied to the output. Thus, all of the criteria are met to enter the ACF during soft start, but the boot pin for the high voltage level shifter and driver is not charged. The NCP1568D works in DCM operation for the first part of the soft start T_{DCM_SS} (typically 706 μs) to make sure that the boot capacitor is charged. During the soft start, the PWM pulse width is gradually increased by ramping the internal current limit reference to its final value. After T_{DCM_SS}, the IC slowly increases the ADRV on time via the LEM process. Once the internal current limit reaches its maximum value, the IC then operates in ACF mode. The IC must wait for an additional time referred to as T_{MODE_Sam} (typically, twice the soft start time), to allow the output voltage to reach regulation and the FB node to stabilize. After T_{MODE_Sam} expires, the ACF detection circuits and logic are no longer manipulated, but are allowed to transition as the output load requires to achieve optimal frequency.

Forced DCM

The forced DCM operation allows a sufficient number of low side pulses to charge the high side drivers, boot capacitor, and to allow the driver sufficient time to perform internal startup sequences. The maximum current provided to the output for the first few switching cycles is regulated by the minimum on time. Minimum on time is a sum of LEB, propagation delay of CS comparator, gate drive, and the FET turn off. To reduce primary and secondary start up current stress, the frequency is ramped to half the oscillator frequency set by RT during T_{DCM_SS} typically 706 μs.

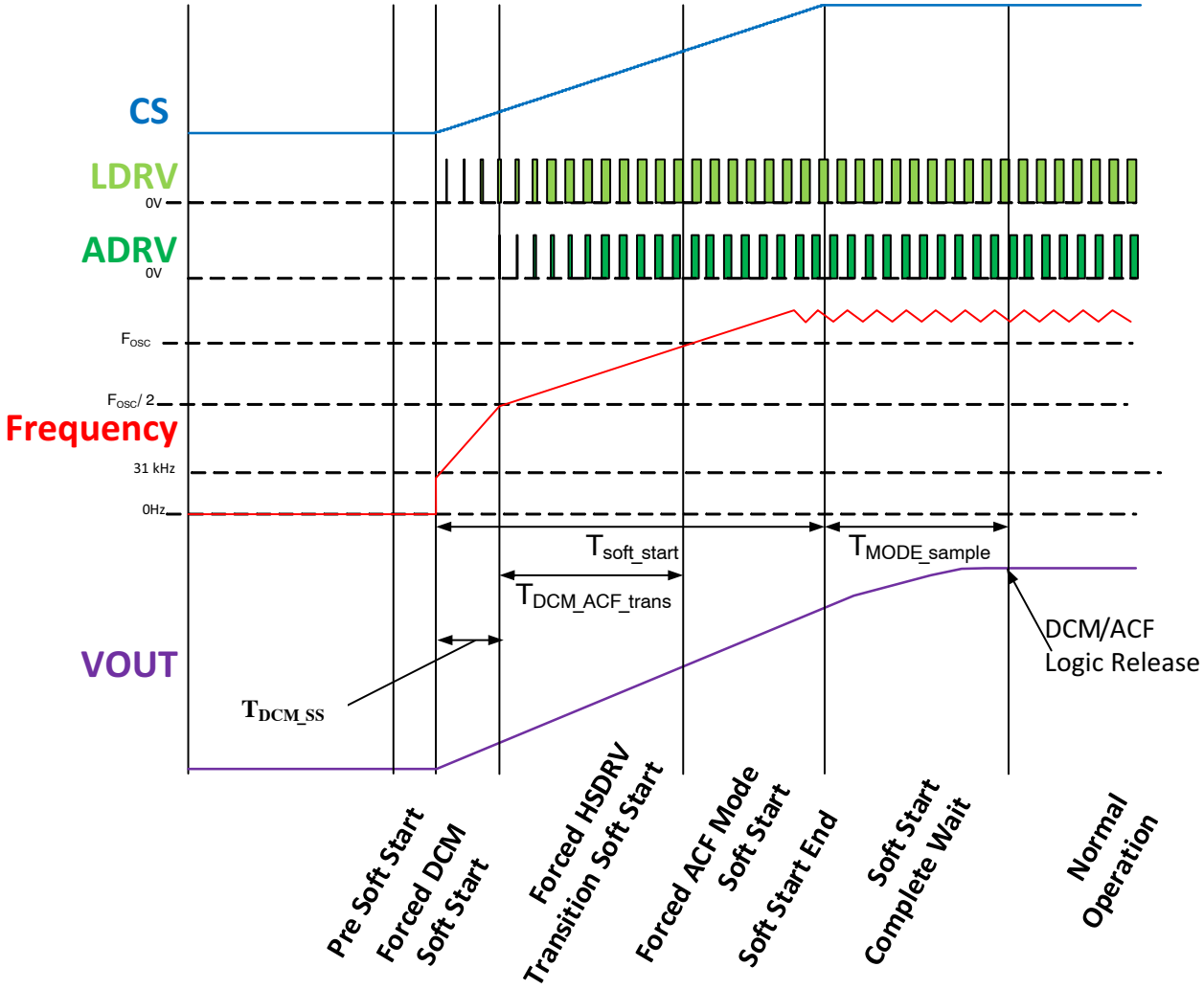


Figure 18. Duty Cycle and Frequency Modulation

Slope Compensation

Fixed frequency peak current mode control architecture is prone to subharmonic oscillation for duty cycles greater than 50%. Subharmonic oscillations are typically characterized by observing the SW node alternating wide and narrow pulse widths. An additional compensating ramp, if either added to the sensed inductor current or subtracted from the loop error voltage (FB), will prevent the subharmonic oscillations. In a flyback topology employing current mode control, the slope of this stabilizing ramp also known as slope compensation, is proportional to the down slope of the power converter (duty cycle greater than 50%). The minimum amount of slope compensation to negate the oscillation is equal to 1/2 the down slope. However, for dead band compensation, the ramp is equal to the down slope. Note that with higher slope compensation, the power converter's ac characteristics will start resembling that of voltage mode control. Slope compensation is set to 143 mV/μs.

Feedback Pin

The FB pin is equipped with a 100 μA pullup current source and a 20 kΩ resistor. The pullup current source and resistor work in conjunction with the optocoupler to regulate the system output voltage.

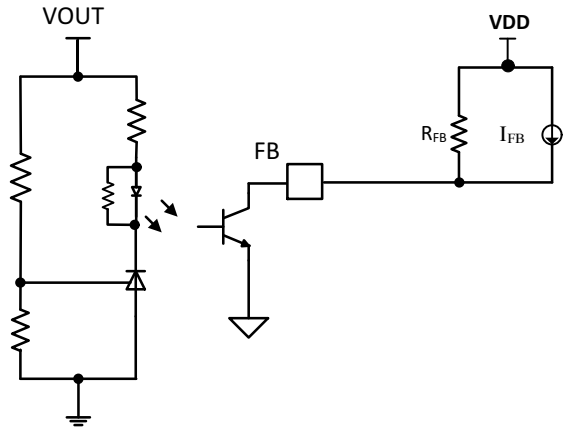


Figure 19. FB Resistor and Current Pullup Diagram

Low Side Driver

The low side driver is a ground based driver and is suitable for direct driving high capacitance switches, as its sourcing current is I_{LS_src} (typically 1.3 A) resulting in a rise time of T_{LS_rise} (typically 10.7 ns) with a 1.5 nF load. No additional pull down circuitry is needed as the sinking current I_{LS_snk} (typically 2.5 A) results in a fall time of T_{LS_fall} (typically 6.5 ns) with a 1.5 nF load. The low side driver is also equipped with an internal clamp $V_{LDRV(low)}$ (typically 11.75 V) to prevent the voltage on the gate from exceeding the maximum rating if the V_{CC} voltage of the controller increases beyond 20 V and to minimize losses in the system. The IC draws I_{CC3} (typically 3.9 mA) when the IC is switching both LDRV and ADRV drivers at 500 kHz with 100 pF load, but increases to I_{CC4} and I_{CC5} when fully loaded at 100 kHz and 500 kHz to 4.0 mA and 13 mA, respectively with a 1.5 nF load.

Active Clamp Driver

The Active Clamp Driver ADRV ground based driver is suitable for sending 5 V logic square wave signals to a high side driver with a built in level shifter to modulate the on time of the active clamp FET. The drive with 95 mA of sourcing current and 231 mA of sinking current is also sufficient to drive a pulse transformer.

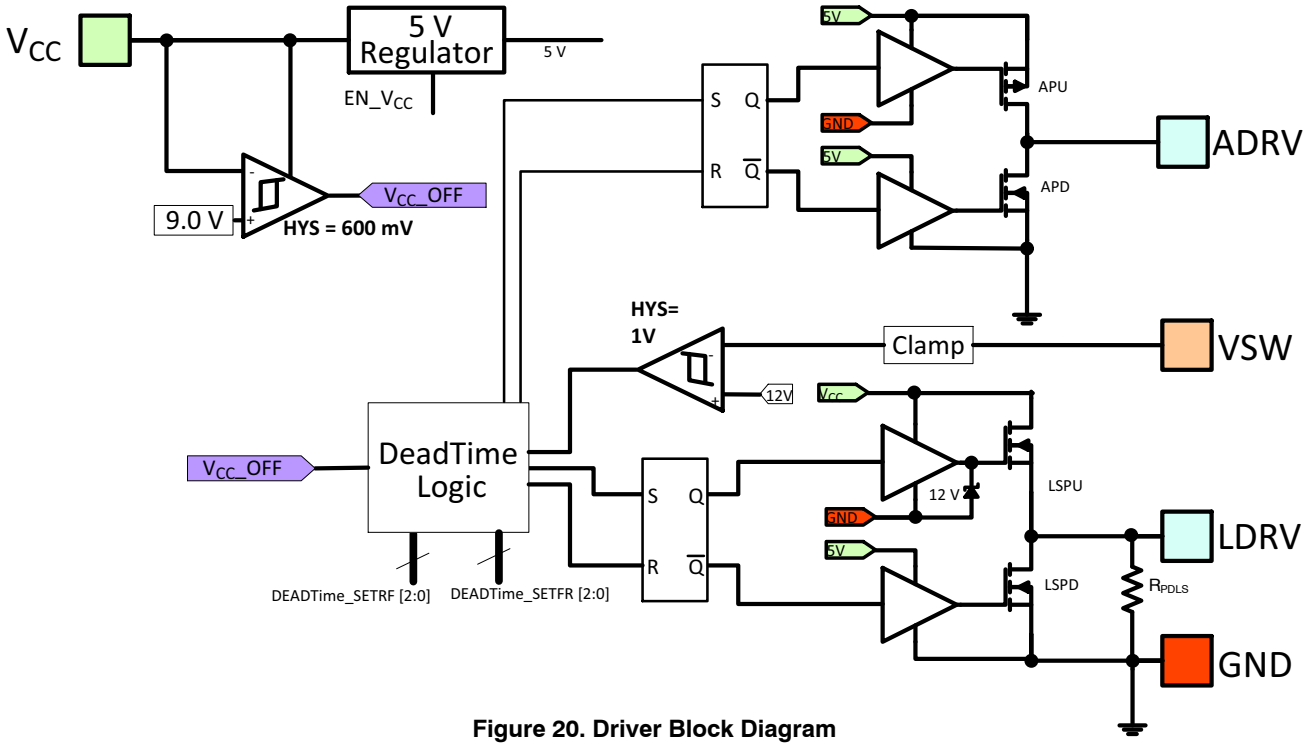


Figure 20. Driver Block Diagram

Adaptive Dead Time

The NCP1568D implements a built in adaptive dead time that maximizes the efficiency of an active clamp flyback converter. The dead time for the active clamp topology can be described by first identifying the two modes of operation of the switch node (SW) or bridge node. When the topology is actively clamping and the SW is high, current can flow into and out of the clamp capacitor. The time that the energy is stored and recycled in the clamp capacitor is referred to as the resonant mode and is identified with a high voltage on the switch node. During the resonant mode, the high side FET or body diode is conducting. When the low side FET is conducting, the SW is near ground potential when the primary inductor current has a positive slope, and is referred to as energy storage mode. The magnetizing inductance current is ramped up during the energy storage mode until the low side drive transitions from high to low. The switch node is then pulled high by the circulating currents. The rate at which the SW changes voltage is dependent on the voltage controlled parasitic capacitance of the selected FETs at the bridge node, the primary current, the magnetizing inductance, the leakage inductance, and other factors. Since

many of the governing factors determining the rise and fall time of the switch node are design specific, an active dead time control circuitry must be employed to optimize efficiency for a wide range of applications. During the energy storage to resonant mode SW node transition, the majority of the transition time is spent charging the relatively large C_{OSS} capacitance of the low side FET when the SW node is near ground potential and the C_{OSS} capacitance of the high side FET as the SW node nears the clamp voltage. The resulting slope of the voltage change at low voltages is in the order of 100 MV/s. Once the switch node has started to charge the C_{OSS}, the capacitance decreases rapidly and the slope can increase on the switch node to as much as 10 GV/s. The active dead time control starts a timer once the LDRV internal logic has transitioned from TTL logic level high to low referred to as D_{T_Max}. The D_{T_Max} is a fail safe dead timer that ensures normal operation. After the low side driver logic transition is tripped, the part will monitor the voltage at SW to determine when it has exceeded 10 V. Once the 10 V threshold is exceeded, a second timer is started called DT_E_R. After the DT_E_R timer has expired, the ADRV will generate a 5 V logic level high to turn on the high side FET so that the high side FET will start conducting. If the D_{T_Max} timer expires before the 10 V threshold is met, and the additional DT_E_R timer has not expired, this failure will be counted, but the ADRV will not be forced on. Once the SW is high and the high side FET is conducting, the high side drive will remain high until the end of the cycle. At the end of the cycle, the ADRV will output a 5 V logic level low. When the internal prelevel shifted ADRV TTL logic transitions from high to low, a D_{T_Max} timer is started. The switch node then discharges until it reaches DT_R_E_TH, at which time the DT_R_E timer is started. Once either the DT_R_E or the D_{T_Max} timer has expired, the LDRV will transition from low to high and the process will continue. The dead time D_{T_Max} only applies to the full ACF mode of operation and as such is blanked from ACF to DCM and DCM to ACF transitions when the ADRV pulses are phased in and out with LEM. Further, D_{T_Max} is not observed during the LEM portion of soft start of ACF.

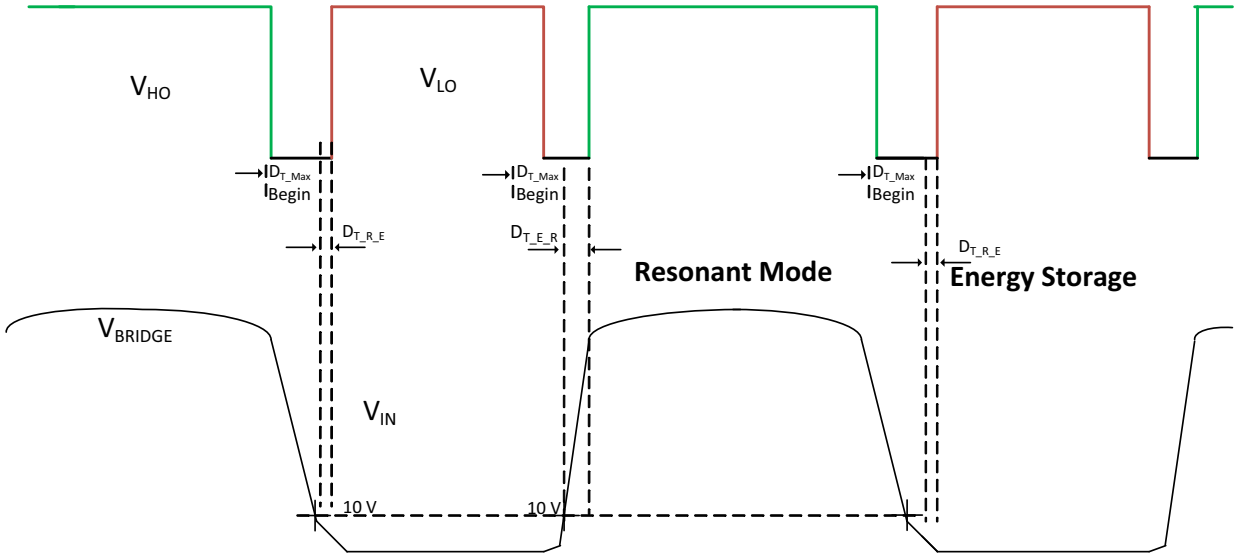


Figure 21. Dead Time and Mode Identification

OTHER PROTECTION FEATURES

FLT Input

The NCP1568D includes a dedicated fault input accessible via the FLT pin. The controller can be latched off or restarted by pulling the pin up above the upper fault threshold (typically 3.0 V). Likewise, the controller can be latched off or restarted if the FLT pin voltage, V_{FLT}, is pulled below the lower fault threshold (typically 0.4 V). The controller operates normally while the FLT pin voltage is maintained within the upper and lower fault thresholds. Figure 22 shows the architecture of the FLT input.

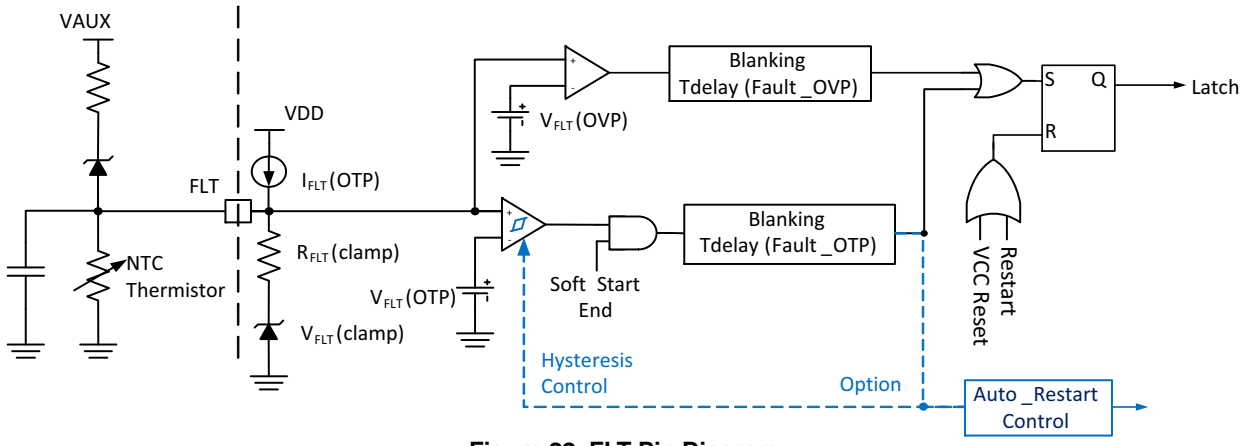


Figure 22. FLT Pin Diagram

OTP FLT Threshold and Fault Handling

The primary purpose of the lower FLT threshold is to detect an over temperature fault using an NTC thermistor. A pull up current source, (typically 45.5 μA) generates a voltage drop across an external thermistor. The resistance of the NTC thermistor decreases as the temperature rises, resulting in a lower voltage across the thermistor. The controller detects a fault once the thermistor voltage drops below the $V_{FLT(OTP\_in)}$ threshold. The FLT voltage must drop below the threshold for longer than $t_{delay(OTP)}$ (typically 33 μs), then the IC will take the appropriate action. If the IC is programmed to latch, the V_{CC} voltage must go below Vcc(reset) before normal operation can continue. If the IC is programmed to restart, the part will initiate a soft start once the temperature decreases and the corresponding NTC voltage has increased enough to exceed the $V_{FLT(OTP\_out)}$ threshold (typically 937 mV).

OTP FLT Threshold Startup

A bypass capacitor is usually connected between the FLT and GND pins and it will take some time for VFLT to reach its steady state value once IFLT(OTP) is enabled. The IC is prevented from switching as long as the FLT voltage is below the $V_{FLT(OTP\_in)}$ threshold. When adapters are produced they must go through a burn in process. The process calls for the adapter to be heated up to higher ambient temperatures (typically 65°C), then powered on and allowed to operate for an extended period of time to catch any assembly or part defects early before they are shipped to end customers. With the above burn in process, the FLT pin can cause the NTC to trip and keep the part off during the burn in process. To prevent the adapter from failing the burn in test, the adapter must start up when the FLT voltage exceeds $V_{FLT(OTP\_out\_1st)}$ (typically 418 mV), rather than $V_{FLT(OTP\_out)}$ (typically 937 mV). Further, the IC must successfully complete a soft start by reaching the end of forced ACF without triggering a V_{CC} off as shown in Figure 23.

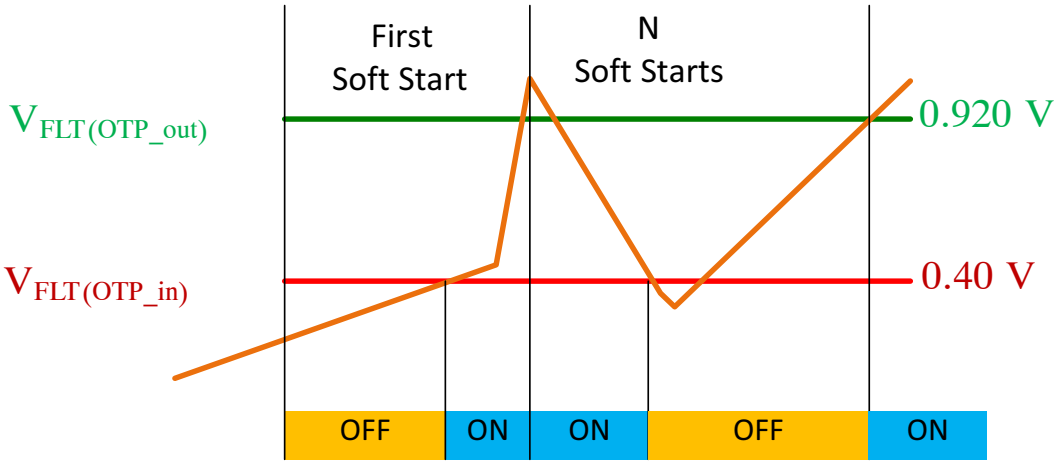


Figure 23. FLT Pin Diagram

The IC is enabled above $V_{FLT(OTP\_out\_1st)}$ in soft start only, rather than $V_{FLT(OTP\_out)}$. The rest of the functionality of the FLT pin after a successful soft start is unchanged. Therefore, a lower fault (i.e. over temperature) is acknowledged under the $V_{FLT(OTP\_out\_1st)}$ threshold in soft start, holding the part in reset until the threshold is clear. When the FLT pin is below the $V_{FLT(OTP\_in)}$ threshold, the current draw of the IC is I_{CC1A} (typically 240 μA).

OVP FLT Threshold

The upper fault threshold is intended to be used to prevent an overvoltage using a zener diode and a resistor in series from the auxiliary winding voltage (V_{AUX}) to ground with the FLT pin connected at the anode as shown in Figure 22. To reach the upper threshold, the external pull up current has to be greater than the pull down capability of the clamp $V_{FLT\ (clamp)}$ (typically 1.75 V) and $R_{FLT\ (clamp)}$ (typically 1.57 kΩ) the resistor in series. The FLT voltage must increase above the threshold for longer than $t_{delay(OTP)}$ (typically 33 μs), then the IC will take the appropriate action of latching or restarting. If the IC is programmed to latch, the V_{CC} voltage must go below $V_{CC(reset)}$ before normal operation can continue. If the IC is programmed to restart, the part will initiate the restart timer once V_{AUX} voltage decreases below the hysteresis of the OVP comparator. The internal clamp prevents the FLT pin voltage from reaching the upper latch threshold if the pin is open. When the FLT pin is above the $V_{FLT(OVP)}$ threshold, the current draw of the IC is I_{CC1B} (typically 240 μA).

When the auto recovery option is selected for the fault pin, $I_{FLT(OTP)}$ remains enabled while the lower fault is present independent of V_{CC} in order to provide temperature hysteresis. The controller can detect an upper OVP fault once V_{CC} exceeds $V_{CC(reset)}$. Once the controller is latched, it is reset if V_{CC} is cycled down to its reset level, $V_{CC(reset)}$. In the typical application these conditions occur only if the ac voltage is removed from the system.

Over Power Protection

The maximum power delivered by an isolated power converter is controlled by limiting the peak inductor current on a pulse by pulse basis on the primary side. Power converters typically do not deliver the same maximum output power across all line conditions. Energy delivery is influenced by duty ratio, line voltage, and switching frequency. The duty ratio changes with line voltage and hence with a fixed peak current, the average inductor current varies over line voltage. The slope of the current increases as the line voltage increases, delivering more energy with a fixed propagation delay in high line operation. An internal line OPP compensation is provided where line sensed discrete steps provide an approximate transconductance (g_m) of 188 nA/V sourced out of the CS pin such that a designer can compensate for the selected inductance. The propagation delays of all comparators connected to the CS pin such as SCP, OCP, peak current freeze, and the PWM comparator all benefit from the line compensation.

Current Limit

The current passing through the primary main FET is sensed via a resistor at the CS pin. The ramping current sensed by the CS pin is used to modulate the loop error voltage (FB) to generate PWM signals; it is also used for cycle by cycle peak current limit control and detection of a short circuit condition. Figure 24 below shows the block diagram of the current limit circuitry.

Internal Leading Edge Blanking (LEB) circuitry masks the current sense information before applying it to the current monitoring comparators. LEB prevents unwanted noise from terminating the drive pulses prematurely. Placing a small RC filter (typically 47 pF and 732 Ω) close to the CS pin to suppress additional noise is suggested. The LEB period begins once LDRV reaches approximately 2 V. An internal switch $R_{CS(switch)}$ discharges and holds the CS pin low at the conclusion of every cycle for 100 ns. In DCM operation, LEB is implemented by pulling the CS pin low for the LEB period at the beginning of LDRV pulse.

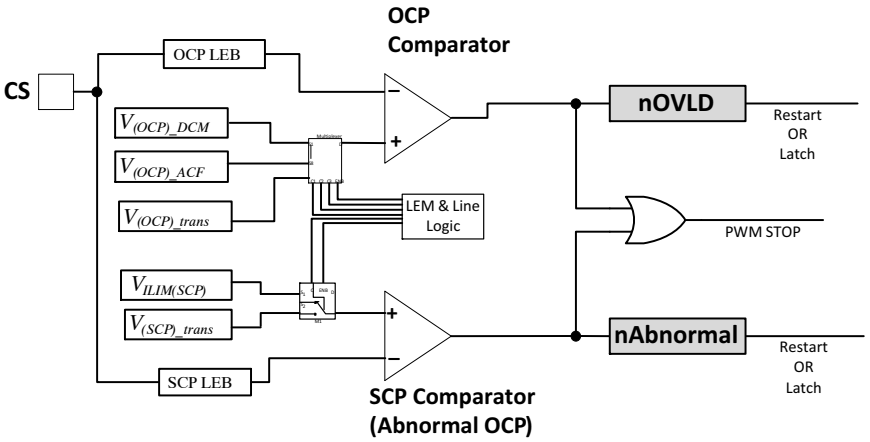


Figure 24. Current Limit Comparators

Cycle by Cycle Current Limiting

Cycle by Cycle (CBC) current limiting is implemented using the OCP comparator and terminates the LSDRV drive pulse if the CS voltage exceeds the $V_{ILIM\ (OCP)}$ threshold in ACF and DCM modes of operation. In transition mode of operation this threshold is raised to $V_{ILIM\ (OCP)\ Trans}$ to facilitate the increased ΔIm while transitioning into or out of ACF operation. When the CS voltage crosses the $V_{ILIM\ (OCP)}$, an error flag is asserted and the counter counts up 2 counts. If a single cycle occurs in which the $V_{ILIM\ (OCP)}$ is not triggered, the counter counts down 1 count. The counter update is done at switching frequency. Hence depending upon the mode of operation (ACF vs. DCM) and line and load conditions, the time it takes to reach full count varies. If the counter has reached full count, a latch or auto recover is initiated dependent on options selected referred to as OCP reaction.

The OCP threshold depends on mode of operation, i.e., DCM versus ACF and frequency pf operation. In the DCM operation, the OCP threshold is 784 mV. However, in ACF operation, the OCP comparator trip voltage varies with the frequency of operation from $V_{(OCP)\_ACF\_C1\_100}$ to $V_{(OCP)\_ACF\_C1\_400}$, this feature is implemented to compensate for higher frequency of operation in a variable environment. Please refer to the electrical table for frequency vs OCP level.

Table 6. CURRENT LIMIT COUNTS AND TIMING

Switching Frequency (kHz)	Counts (k)	Limiting Time (ms)
100	5	25
250	5	10
500	5	5
1000	5	2.5

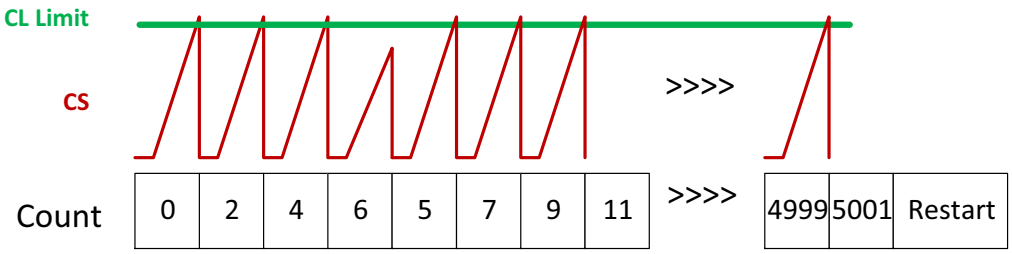


Figure 25. Current Limit Counting Scheme

Short Circuit Protection

A sharp rise in the CS pin sensed current can occur in the primary side if a winding is shorted or a component is faulty. Short circuit protection is implemented using the SCP comparator; it terminates the drive pulse if the CS voltage exceeds the $V_{ILIM\ (SCP)}$ threshold in ACF, DCM, and skip mode of operation after the $T_{LEB(SCP)}$ blanking time. The time $T_{LEB(SCP)}$ is shorter than the $T_{LEB(OCP)}$ by approximately 50 ns to ensure a short circuit is properly identified. When the SCP comparator trips, a count is incremented and a counter tracks the number of SCP events. Once the number of consecutive SCP events crosses N_{SCP} as defined in the electrical table, then the part latches or restarts according to the OTP bits programmed referred to as SCP reaction.

OCP and SCP Level During Transition

The OCP and SCP have two discrete voltage trip levels at an operating point. In ACF mode, the current limit is modulated with frequency change. The NCP1568D ZVS frequency modulation scheme increases the frequency as the line voltage increases. The current limit must be decreased to compensate for the increased available output power when the voltage and frequency increases. The SCP and OCP levels described in the above section are steady state normal protections. When the system is transitioning from ACF operation to DCM operation or DCM operation to ACF operation via the LEM process described in the corresponding sections, the current limits are changed. When the system is undergoing the transition, the OCP and SCP levels are increased from the $V_{(OCP)\_ACF\_100}$ (784 mV at low line) to the $V_{ILIM(OCP)\_Trans}$ 1.2 V and the $V_{ILIM(SCP)}$ 1.2 V to $V_{ILIM(SCP)\_Trans}$ 1.4 V. The current limit levels are increased on the rising edge of the first low side drive pulse of the transition and remain at that level for 1 ms after the transition process has completed, as shown in Figure 26.

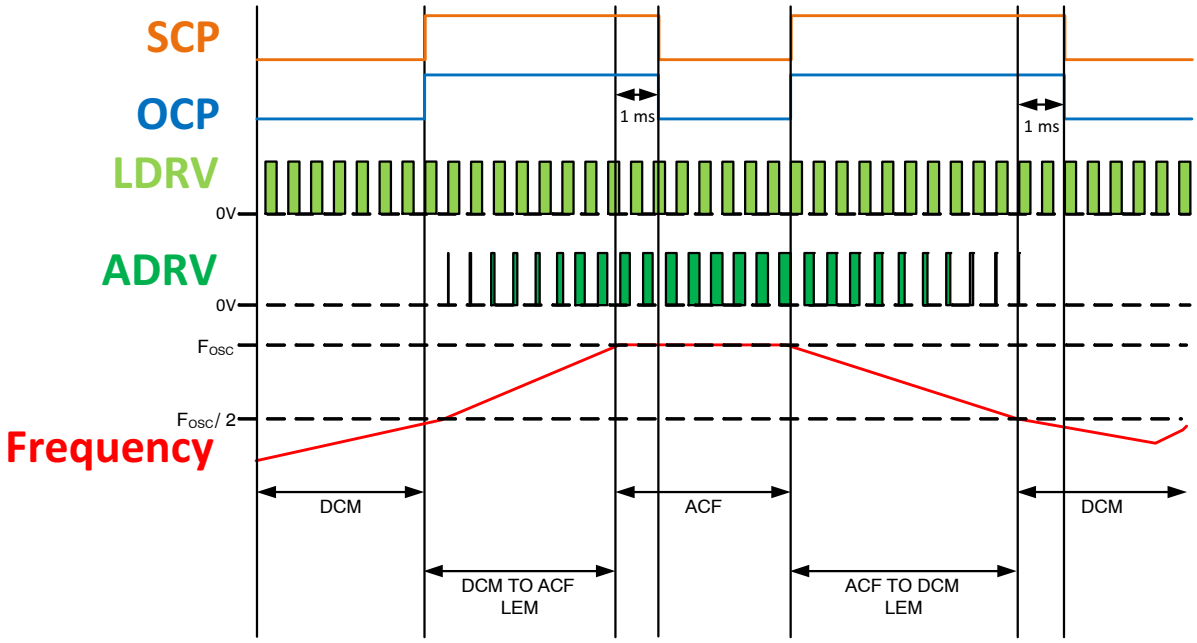


Figure 26. OCP and SCP Timing

HV Bias Cycle (HVBC)

When the IC is not switching due to a fault condition and is either waiting for restart or in latched state the IC's VCC power is maintained by sourcing I_{start2} from the HV pin to the VCC pin. The V_{CC} pin is charged to the $V_{CC(on)}$ threshold, at which time it will turn off. The part dissipates a small amount of power monitoring critical nodes and tracking restart timers while waiting to take the next action. The standby current slowly discharges the V_{CC} pin voltage until the $V_{CC(off)}$ threshold is tripped. Once the $V_{CC(off)}$ threshold is tripped, the part will source I_{start2}, charging the V_{CC} capacitor to maintain critical functions. The charging and discharging of the V_{CC} voltage, also referred to as HV Bias Cycle (HVBC), will continue until the HV pin's voltage is removed, the V_{CC} voltage drops below $V_{CC(reset)}$, T_{auto_retry} has expired.

Auto Recovery and Latch

The auto recovery fault behavior is used to protect the end user from any abnormal conditions, to reduce power consumption during a fault condition, and to allow the adapter to recover quickly as soon as the issue has been resolved without the need to unplug and replug the power supply. If a fault occurs when the IC is configured to auto recovery, ADRV and LDRV are driven low and the part remains off for T_{auto_retry} time maintaining V_{CC} voltage through the HVBC process. At the end of T_{auto_retry}, the IC is allowed to restart via the soft start process once $V_{CC(on)}$ is reached.

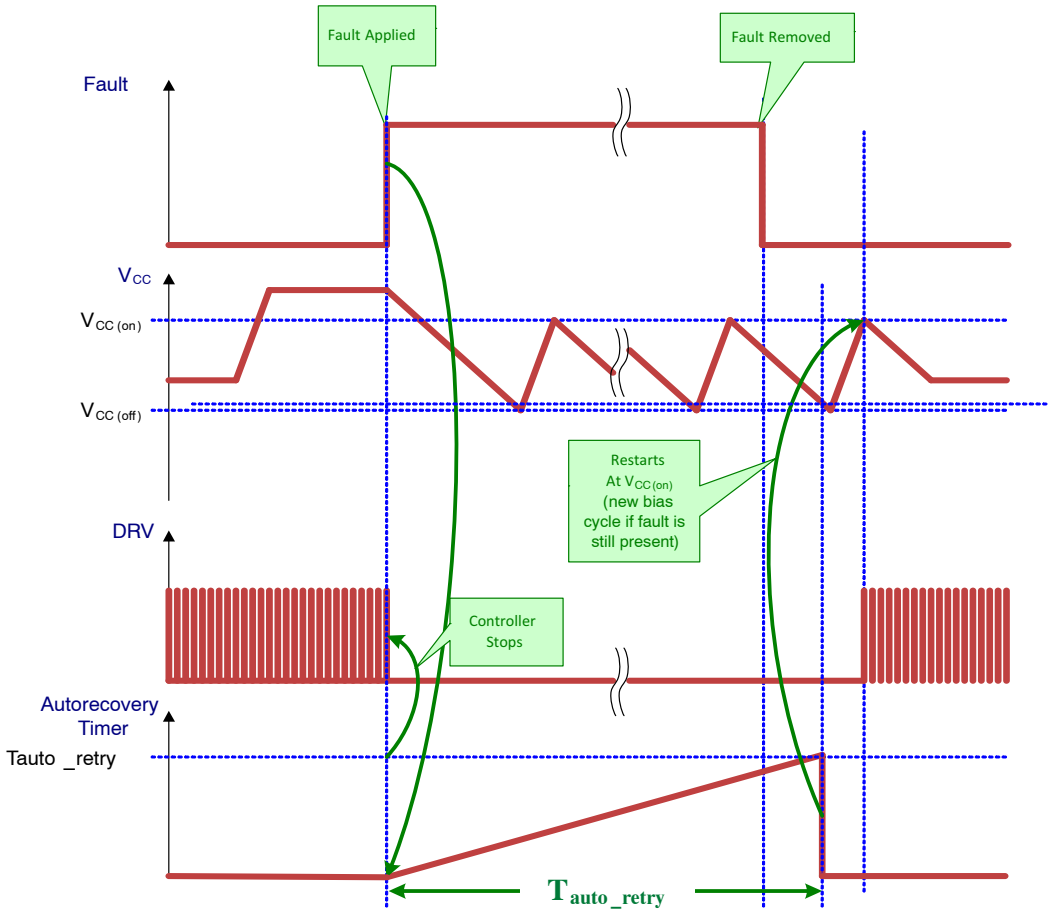


Figure 27. Fault Recovery Behavior

Latching Fault Behavior

The purpose of a latch fault is to require user intervention to restore proper operation of the adapter or power supply. The user is expected to unplug and replug the adapter to enable the power supply to attempt regulation. If a fault occurs and the NCP1568D is configured to have a latch fault in ACF operation or DCM operation once the current clock cycle expires, both LDRV and ADRV are terminated. In skip operation since there are no pulses, no pulses will be produced as a result of a latch fault. The part then monitors the line to determine when power has been removed and maintains V_{CC} voltage by HVBC. When the FLT pin initiates a latch fault, the current draw of the IC is I_{CC1C} (typically 220 μA).

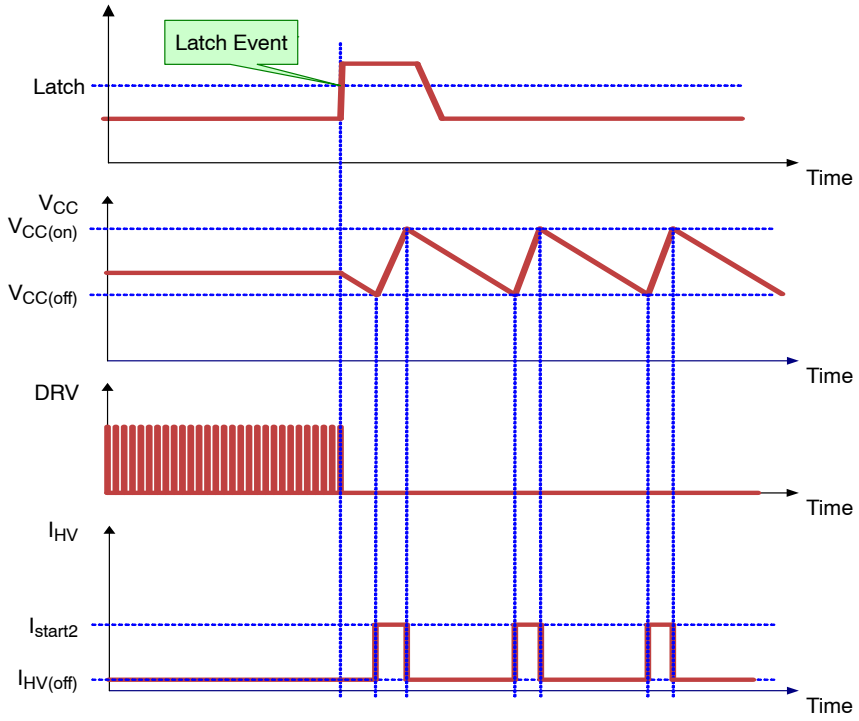


Figure 28. Fault Latched Behavior

Thermal Shutdown

An internal thermal shutdown circuit monitors the junction temperature of the controller. The controller is disabled if the junction temperature exceeds the thermal shutdown threshold, T_{SHDN} (typically 150°C). When a thermal shutdown fault is detected, the controller enters a nonlatching fault mode and remains there until the junction temperature drops below T_{SHDN} by the thermal shutdown hysteresis, $T_{SHDN(HYS)}$, (typically 40°C). The thermal shutdown is also cleared if V_{CC} drops below $V_{CC(reset)}$, or a line removal fault is detected. A new power up sequence commences at the next $V_{CC(on)}$.

TYPICAL CHARACTERISTICS

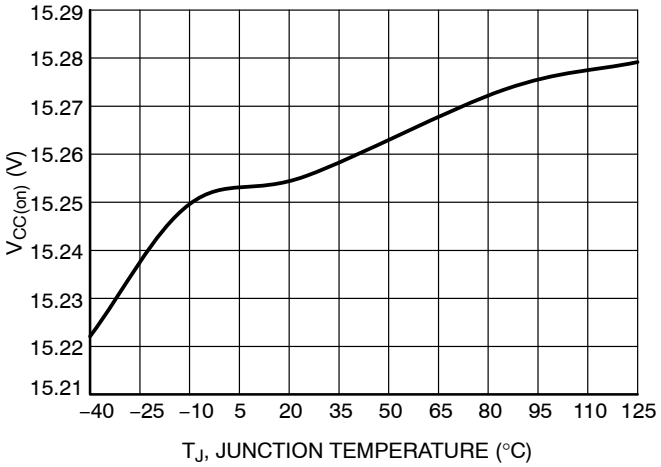


Figure 29. $V_{CC(on)}$ vs. Temperature

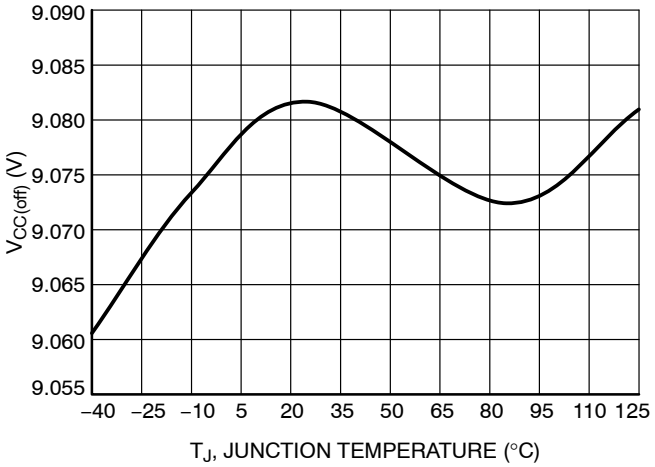


Figure 30. $V_{CC(off)}$ vs. Temperature

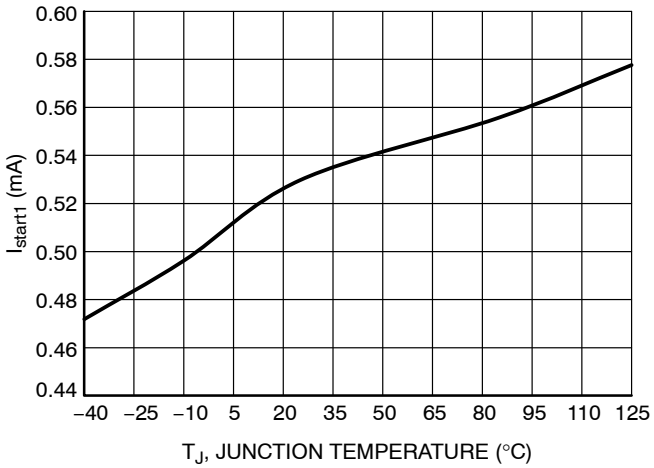


Figure 31. I_{start1} vs. Temperature

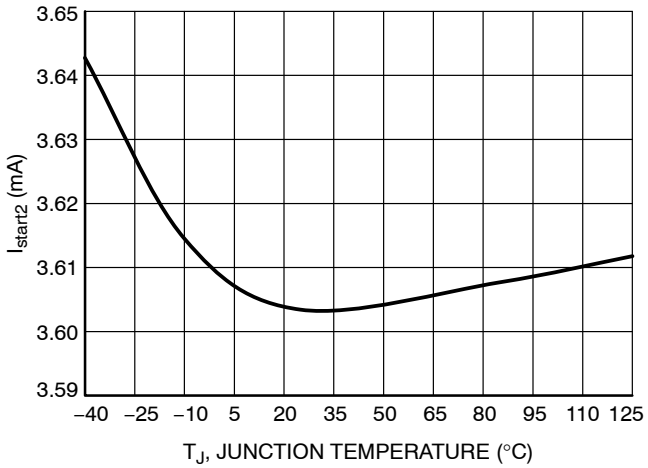


Figure 32. I_{start2} vs. Temperature

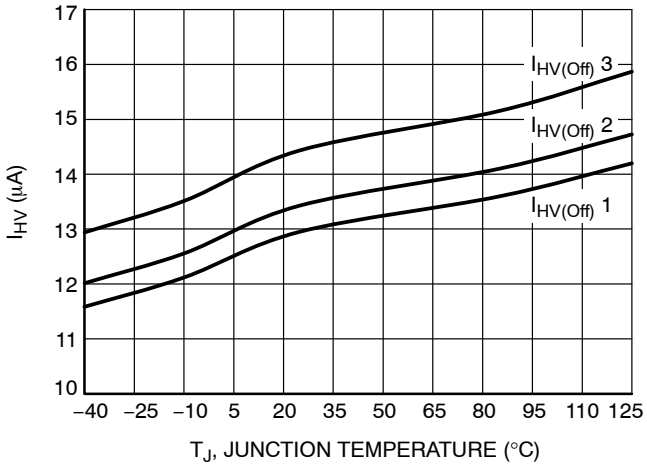


Figure 33. $I_{HV(off)}$ vs. Temperature

TYPICAL CHARACTERISTICS (Continued)

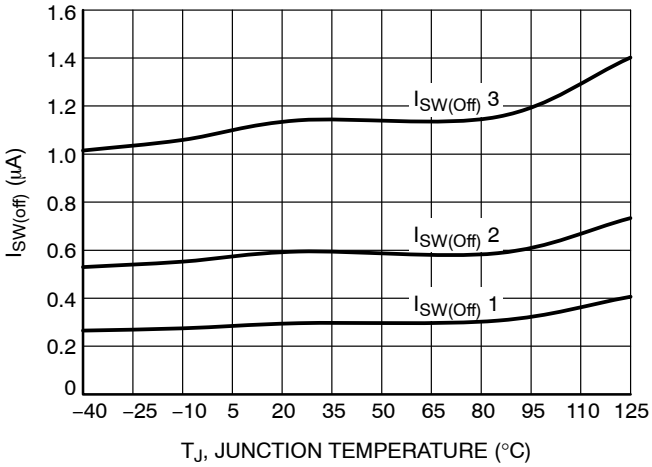


Figure 34. $I_{SW(off)}$ vs. Temperature

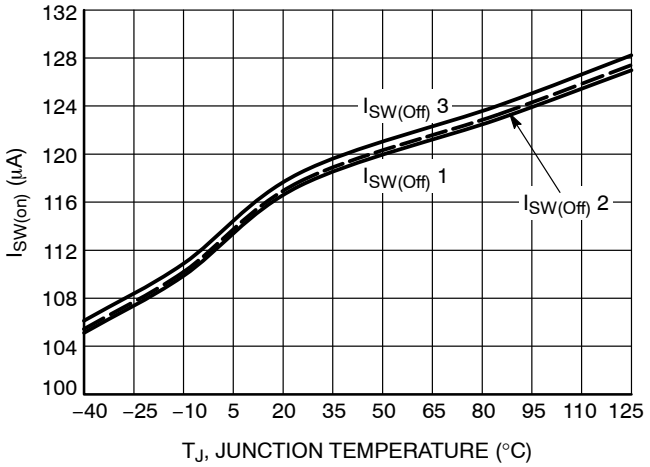


Figure 35. $I_{SW(on)}$ vs. Temperature

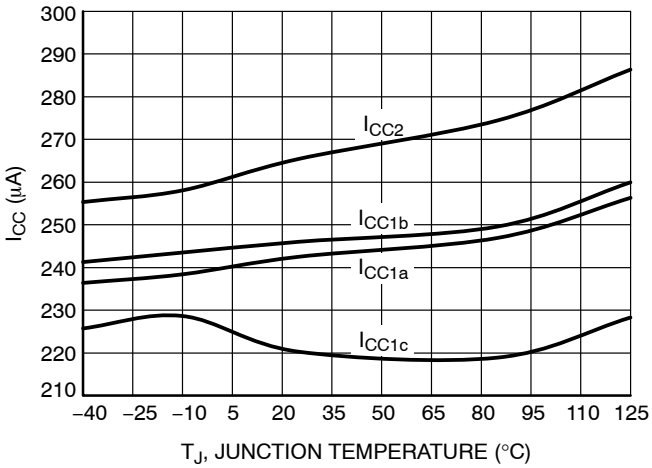


Figure 36. I_{CC1} and I_{CC2} vs. Temperature

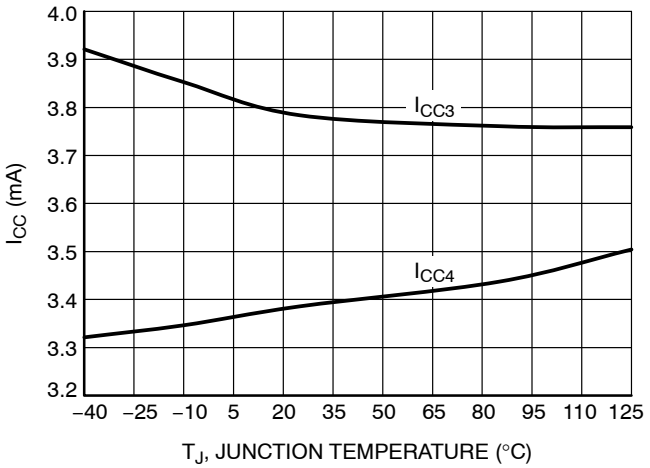


Figure 37. I_{CC3} and I_{CC4} vs. Temperature

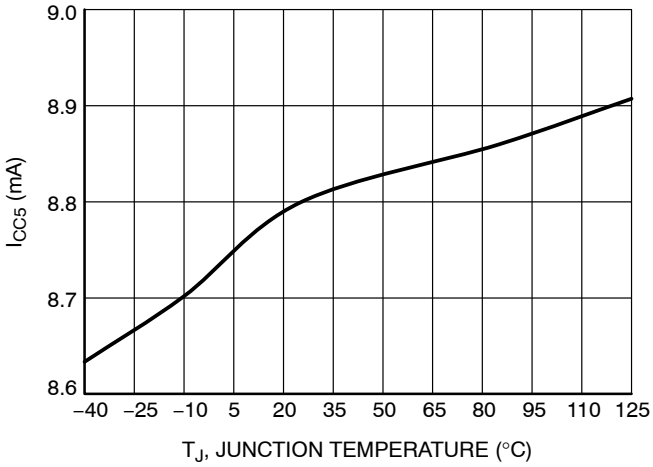


Figure 38. I_{CC5} vs. Temperature

TYPICAL CHARACTERISTICS (Continued)

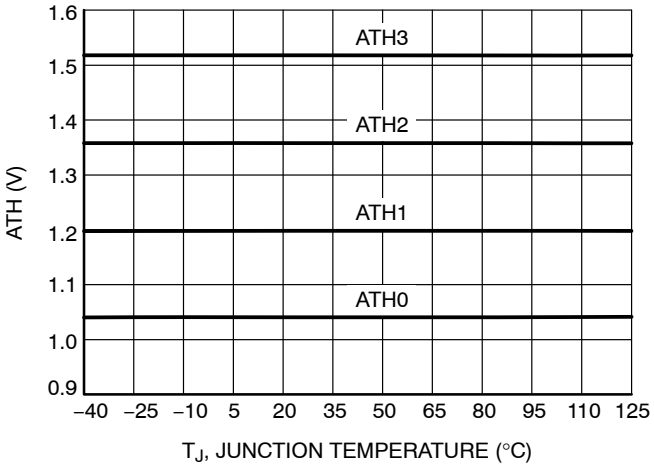


Figure 39. ATH 0−3 vs. Temperature

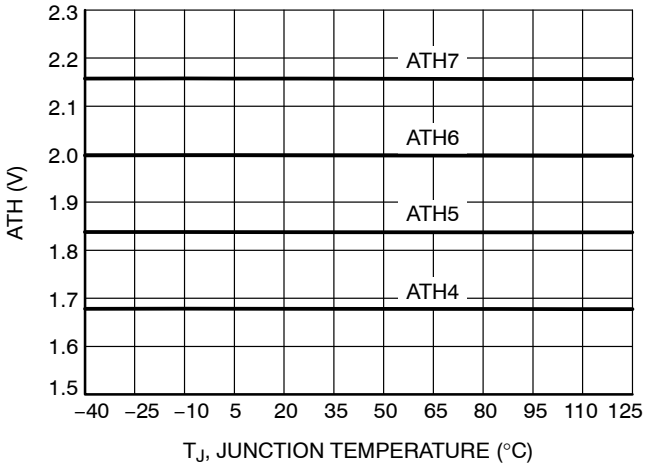


Figure 40. ATH 4−7 vs. Temperature

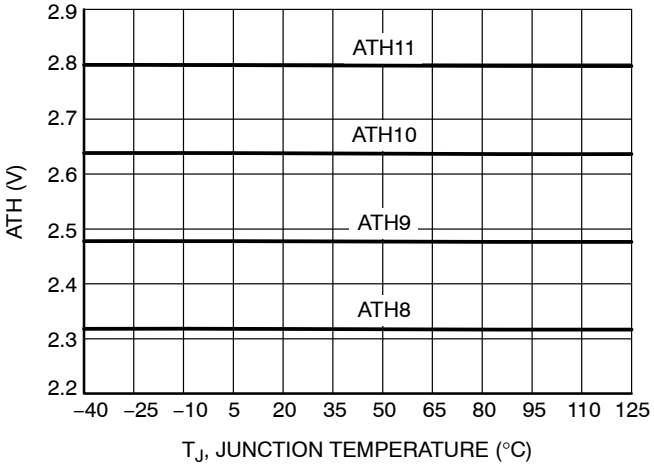


Figure 41. ATH 8−11 vs. Temperature

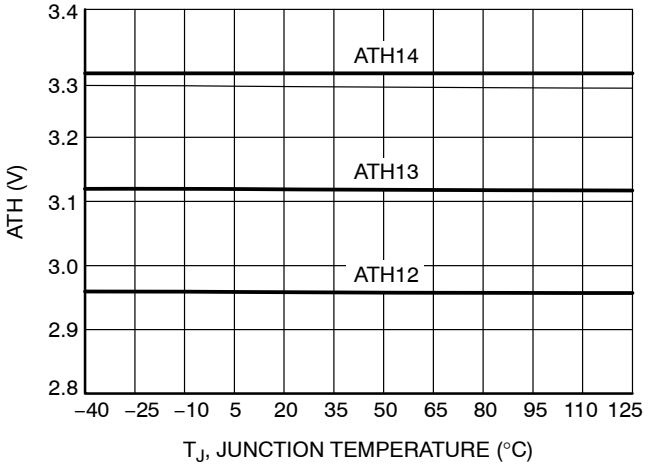


Figure 42. ATH 12−14 vs. Temperature

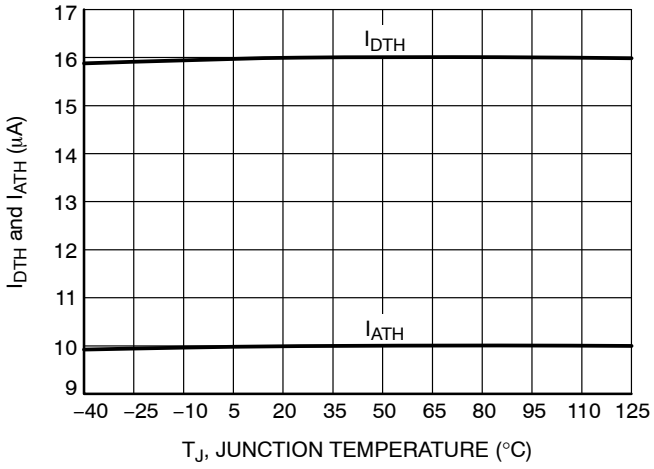


Figure 43. I_{DTH} and I_{ATH} vs. Temperature

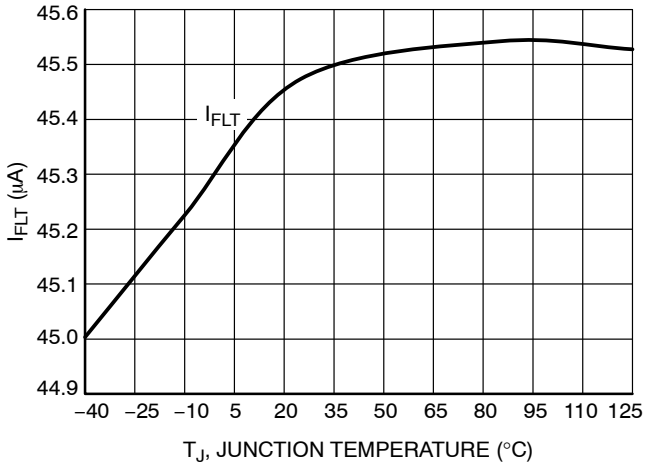


Figure 44. I_{FLT} vs. Temperature

TYPICAL CHARACTERISTICS (Continued)

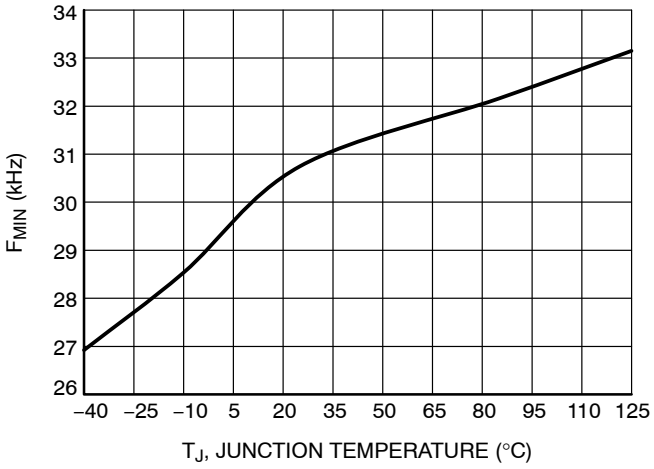


Figure 45. F_{MIN} vs. Temperature

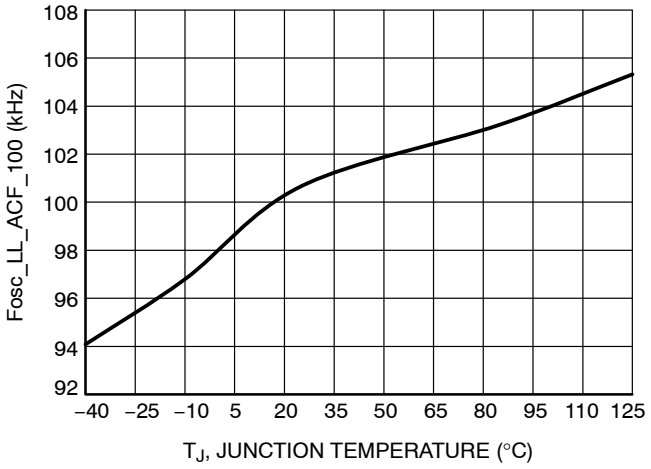


Figure 46. Fosc_LL_ACF_100 vs. Temperature

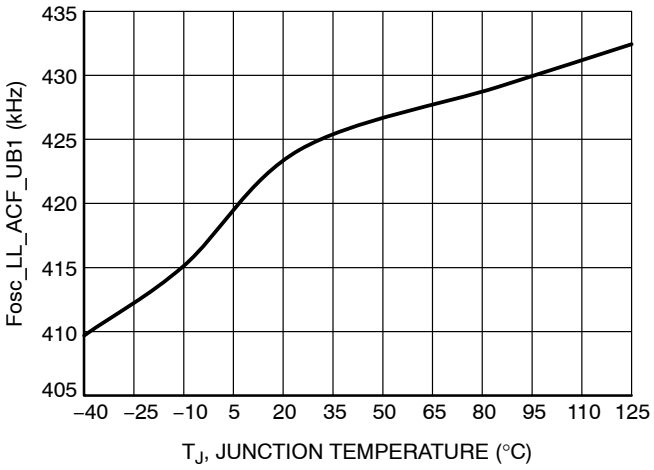


Figure 47. Fosc_LL_ACF_UB1 vs. Temperature

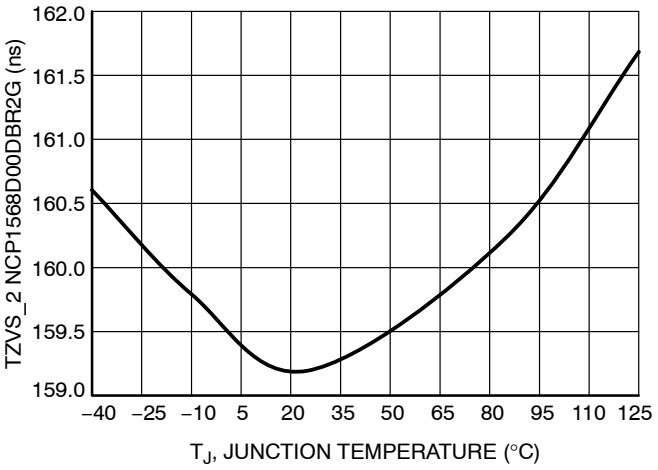


Figure 48. TZVS_2 NCP1568D00DBR2G vs. Temperature

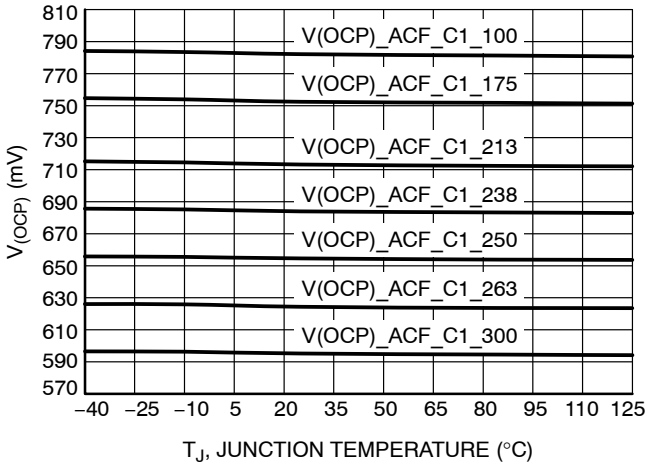


Figure 49. $V_{(OCP)}$ vs. Temperature

TYPICAL CHARACTERISTICS (Continued)

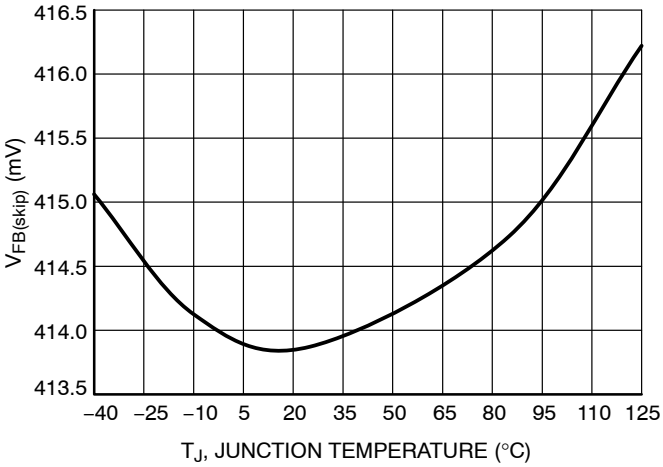


Figure 50. $V_{FB(skip)}$ vs. Temperature

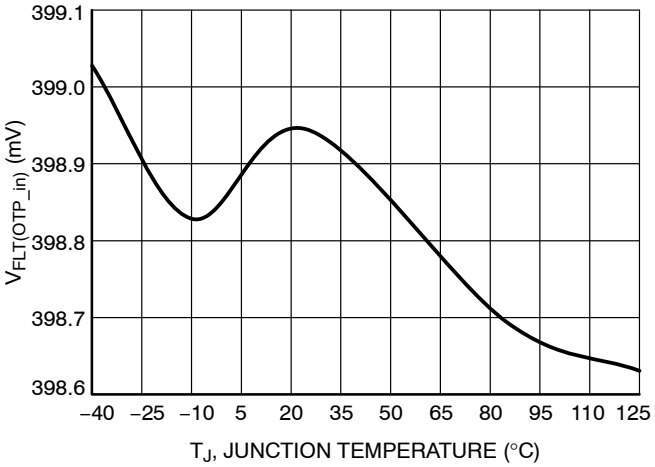


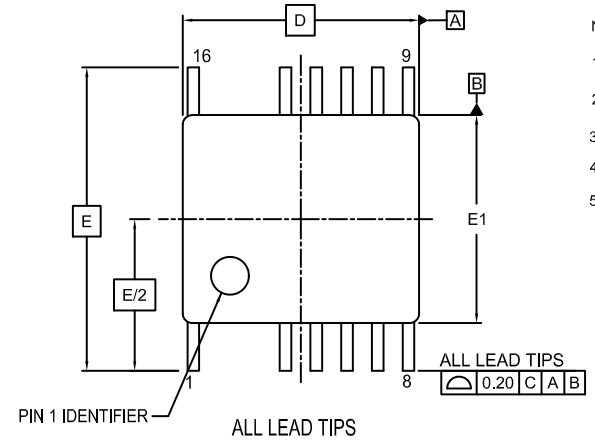
Figure 51. $V_{FLT(OTP\_in)}$ vs. Temperature

PART NUMBER DECODING INFORMATION

Parameter									NCP1568DDBR2G
Disable OPP Sampling	EN	Dis							Dis
Enable NDTMAX	EN	Dis							Dis
ATH Pin Mapping	I = 1.72 E = 0	I = 1.92 E = 1	I = 2.36 E = 2	I = 2.68 E = 2					I = 1.92 E = 1
ATH Internal = I / External = E	I	E							E
Select DCM Lockout Time (ms)	1	2	4	0					1
LEM Collision Avoidance Enable	EN	Dis							EN
OPP Disable	EN	Dis							EN
LDRV OFF to HDRV or ADRV ON) (Fixed Dead-Time from	0	20	50	75	100	125	150	200	0
Restart Timer (ms)	200	400	800	1600					1600
Consecutive SCP Events (#)	5	Dis							5
Consecutive OCP Events (k#)	5	10	15	20					5
FB Pullup Current (μA)	100	50	200	0					100
FB Pullup Resistor (kΩ)	400	200	100	20					20
Slope Comp Ramp (mV/μs)	360	200	135	80					135
Skip Type /Skip Disable	Q	H							H
Disable Fast Freq Step	EN	Dis							EN
Frozen Peak Onset (V)	0,8	1	1,2	1,4					0,8
ACF Soft Stop (ms)	2	4	0,5	0					0.5
ACF FET Soft start Time (ms)	2	0,5	2	4					4
Disable Slope Comp	EN	Dis							EN
DCM Oscillator Frequency Max	F(RT)/2	F(RT)/3	F(RT)/4	F(RT)					F(RT)/2
ATH Threshold/ ACF Only	TH	ACF							ACF
VHV Hyst	14	9							14
VHV	112	105	98	114					112
FLT Pin OVP (Latch = L Reset = R)	R	L							R
FLT Pin OTP (Latch = L Reset = R)	R	L							R
OCP Reaction (Latch = L Reset = R)	R	L							R
SCP Reaction (Latch = L Reset = R)	R	L							R
T_ZVSB (ns)	0	20	40	60	80	100	150	200	40
LEB/ DTMAX/ T_ZVSA (ns)	178 / 420/ 210	99 / 240 / 120	175 / 240/ 120	225 / 600 / 300	378 / 600 / 300	299 / 600 / 300	327 / 600 / 300	425 / 600 / 300	99 / 240/ 120
Soft Start Time (ms)	4	8	16	32					8
Part Number Extension 2									0
Part Number Extension 1									0
Switch Technology	D								D
Part Number									NCP1568DDBR2G

PACKAGE DIMENSIONS

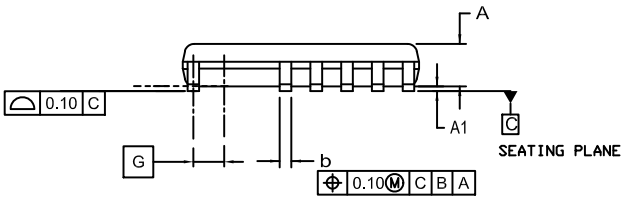
TSSOP16 MINUS PINS 2,3,14 & 15
CASE 948BW
ISSUE O

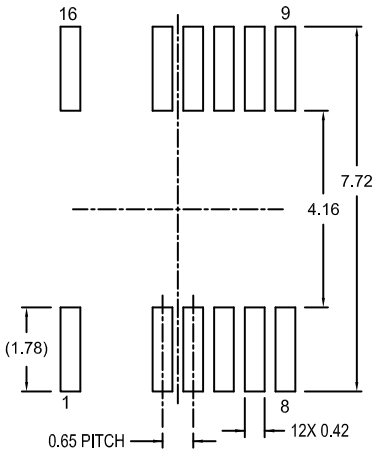


NOTES:

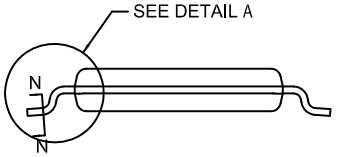
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.10 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT BE IN 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

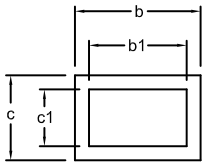
DIM	MILLIMETERS MIN.	MAX.
A	---	1.20
A1	0.05	0.15
b	0.19	0.30
b1	0.19	0.25
c	0.09	0.20
c1	0.09	0.16
D	4.90	5.10
E	6.40 BSC	
E1	4.30	4.50
G	0.65 BSC	
L	0.50	0.75
M	0°	8°



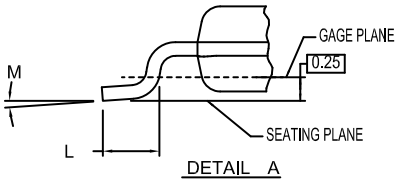


RECOMMENDED MOUNTING FOOTPRINT





SECTION N-N



DETAIL A

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