

# High-Voltage Switcher for Low Power Offline SMPS

## NCP10670B, NCP10671B, NCP10672B

The NCP1067X products integrate a fixed frequency current mode controller with a 700 V MOSFET. Available in a SOIC-7 package, the NCP1067X offer a high level of integration, including soft-start, frequency-jittering, short-circuit protection, skip-cycle, ramp compensation, and a Dynamic Self-Supply (eliminating the need for an auxiliary winding).

During nominal load operation, the NCP1067X switches at one of the available frequencies (60 or 100 kHz). When the output power demand diminishes, the IC automatically enters into a skip mode to reduce the standby consumption down.

Protection features include: a timer to detect an overload or a short-circuit event, Overvoltage Protection with auto-recovery.

For improved standby performance, the connection of an auxiliary winding or supplying the IC from the output, stops the DSS operation and helps to reduce input power consumption below 25 mW at high line.

NCP1067x can be seamlessly used both in non-isolated and in isolated topologies.

### Features

- Built-in 700 V MOSFET with  $R_{DS(on)}$  of 34  $\Omega$  (NCP10670/1) and 12  $\Omega$  (NCP10672)
- Large Creepage Distance Between High-Voltage Pins
- Current-Mode Fixed Frequency Operation – 60 or 100 kHz
- Fixed Ramp Compensation
- Direct Feedback Connection for Non-isolated Converter
- Skip-Cycle Operation at Low Peak Currents Only
- Dynamic Self-Supply: No Need for an Auxiliary Winding
- Internal 4 ms Soft-Start
- Auto-Recovery Output Short Circuit Protection with Timer-Based Detection
- Auto-Recovery Overvoltage Protection with Auxiliary Winding Operation
- Frequency Jittering for Better EMI Signature
- No Load Input Consumption < 25 mW
- These Devices are Pb-Free and are RoHS Compliant

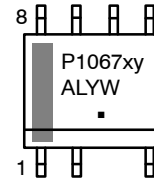
### Applications

- Auxiliary / Standby Isolated and Non-Isolated Power Supplies
- Power Meter SMPS
- Wide Vin Low Power Industrial SMPS



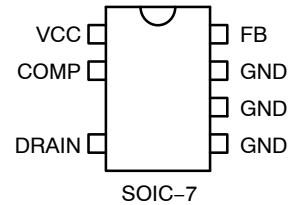
SOIC8  
CASE 751EV

### MARKING DIAGRAM



- P1067 = Specific Device Code
- x = Current Limit (0, 1, 2)
- y = Frequency (060, 100)
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- = Pb-Free Package

### PIN CONNECTION



### ORDERING INFORMATION

See detailed ordering and shipping information on page 23 of this data sheet.

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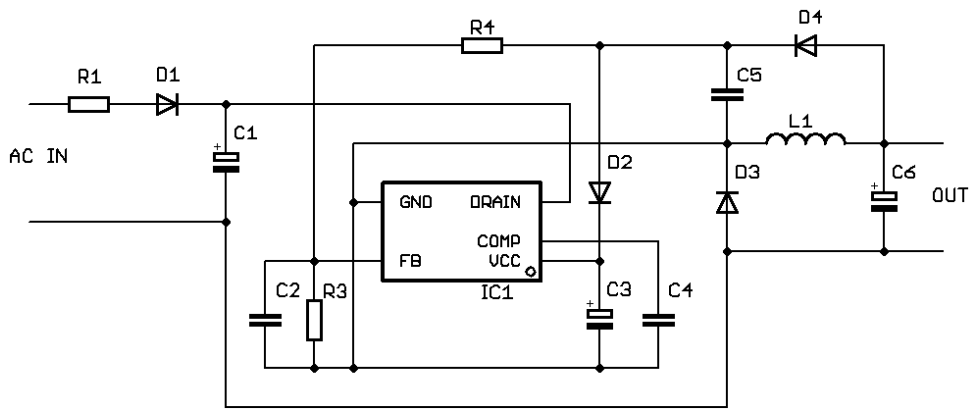
**Table 1. PRODUCTS INFOS & INDICATIVE MAXIMUM OUTPUT POWER**

Product	$R_{DS(on)}$	$I_{PK(0)}$	230 Vac $\pm 15\%$		85 – 265 Vac	
			Adapter	OpenFrame	Adapter	OpenFrame
NCP10670 60 kHz	34 $\Omega$	100 mA	1.1 W	2.7 W	0.6 W	1.5 W
NCP10671 60 kHz	34 $\Omega$	250 mA	2.7 W	6.7 W	1.5 W	3.7 W
NCP10672 100 kHz	12 $\Omega$	780 mA	6.2 W	15.5 W	3.3 W	7.8 W

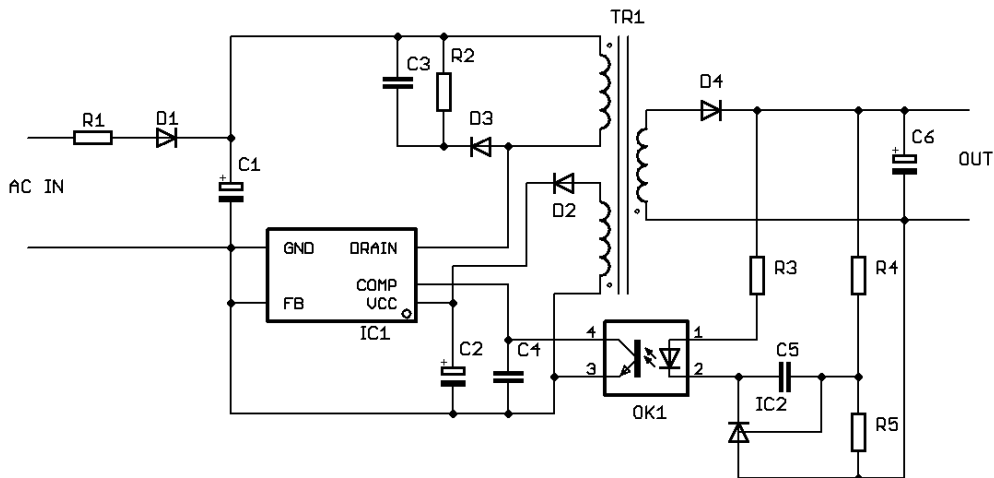
1. Informative values only, with  $T_{amb} = 25^{\circ}C$ ,  $T_{case} = 100^{\circ}C$ , Self supply via Auxiliary winding and circuit mounted on minimum copper area as recommended.

**Table 2. SELECTION TABLE**

Device	Frequency	$R_{DS(on)}$	$I_{PK(0)}$	Package Type
NCP10670	60 kHz	34	100 mA	SOIC-7 (Pb-Free)
NCP10670	100 kHz	34	100 mA	
NCP10671	60 kHz	34	250 mA	
NCP10671	100 kHz	34	250 mA	
NCP10672	60 kHz	12	780 mA	
NCP10672	100 kHz	12	780 mA	



**Figure 1. Typical Non-Isolated Application (Buck Converter)**



**Figure 2. Typical Isolated Application (Flyback Converter)**

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## PIN DESCRIPTION

Pin No.	Name	Function	Description
1	V <sub>CC</sub>	Powers the internal circuitry	This pin is connected to an external capacitor. The V <sub>CC</sub> includes an auto-recovery over voltage protection.
2	Comp	Compensation	The error amplifier output is available on this pin. The network connected between this pin and ground adjusts the regulation loop bandwidth. Also, by connecting an opto-coupler to this pin, the peak current set point is adjusted accordingly to the output power demand.
3			This missing pin ensures adequate creepage distance
4	Drain	Drain connection	The internal drain MOSFET connection
5-7	GND	The IC Ground	
8	FB	Feedback signal input	This is the inverting input of the trans conductance error amplifier. It is normally connected to the switching power supply output through a resistor divider.

**Table 3. TYPICAL APPLICATION**

Non Isolated Buck	
	<ul style="list-style-type: none"> <li>• If the output voltage is above 9.0 V typ. (between V<sub>CC(on)</sub> level and V<sub>OVP</sub> level) VCC is supplied from output via D2</li> <li>• If the output voltage is below 9.0 V, D2 is redundant, the IC is supplied from DSS</li> <li>• Direct feedback, resistive divider formed by R3, R4 sets output voltage</li> </ul>
	<ul style="list-style-type: none"> <li>• If the output voltage is above 9.0 V typ. (between V<sub>CC(on)</sub> level and V<sub>OVP</sub> level) VCC is supplied from output via D3</li> <li>• If the output voltage is below 9.0 V, D3 is redundant, the IC is supplied from DSS</li> <li>• Optocoupler feedback, output voltage is set by D4</li> </ul>
Non Isolated Buck-Boost (Invert)	
	<ul style="list-style-type: none"> <li>• If the output voltage is above 9.0 V typ. between V<sub>CC(on)</sub> level and V<sub>OVP</sub> level, VCC is supplied from output via D2</li> <li>• If the output voltage is below 9.0 V, D2 is redundant, the IC is supplied from DSS</li> <li>• Direct feedback, resistive divider formed by R3, R4 sets output voltage</li> </ul>

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**Table 3. TYPICAL APPLICATION**

<b>Non Isolated Flyback</b>	
	<ul style="list-style-type: none"> <li>• If the output voltage is above 9.0 V typ. between <math>V_{CC(on)}</math> level and <math>V_{OVP}</math> level <math>-V_{CC}</math> supplied from output via D4</li> <li>• If the output voltage is below 9.0 V, D4 is redundant, the IC is supplied from DSS</li> <li>• Resistive divider formed by R2, R3 sets output voltage</li> </ul>
<b>Isolated Flyback</b>	
	<ul style="list-style-type: none"> <li>• VCC supplied from auxiliary winding</li> <li>• Optocoupler feedback, resistive divider formed by R6, R7 sets output voltage</li> </ul>

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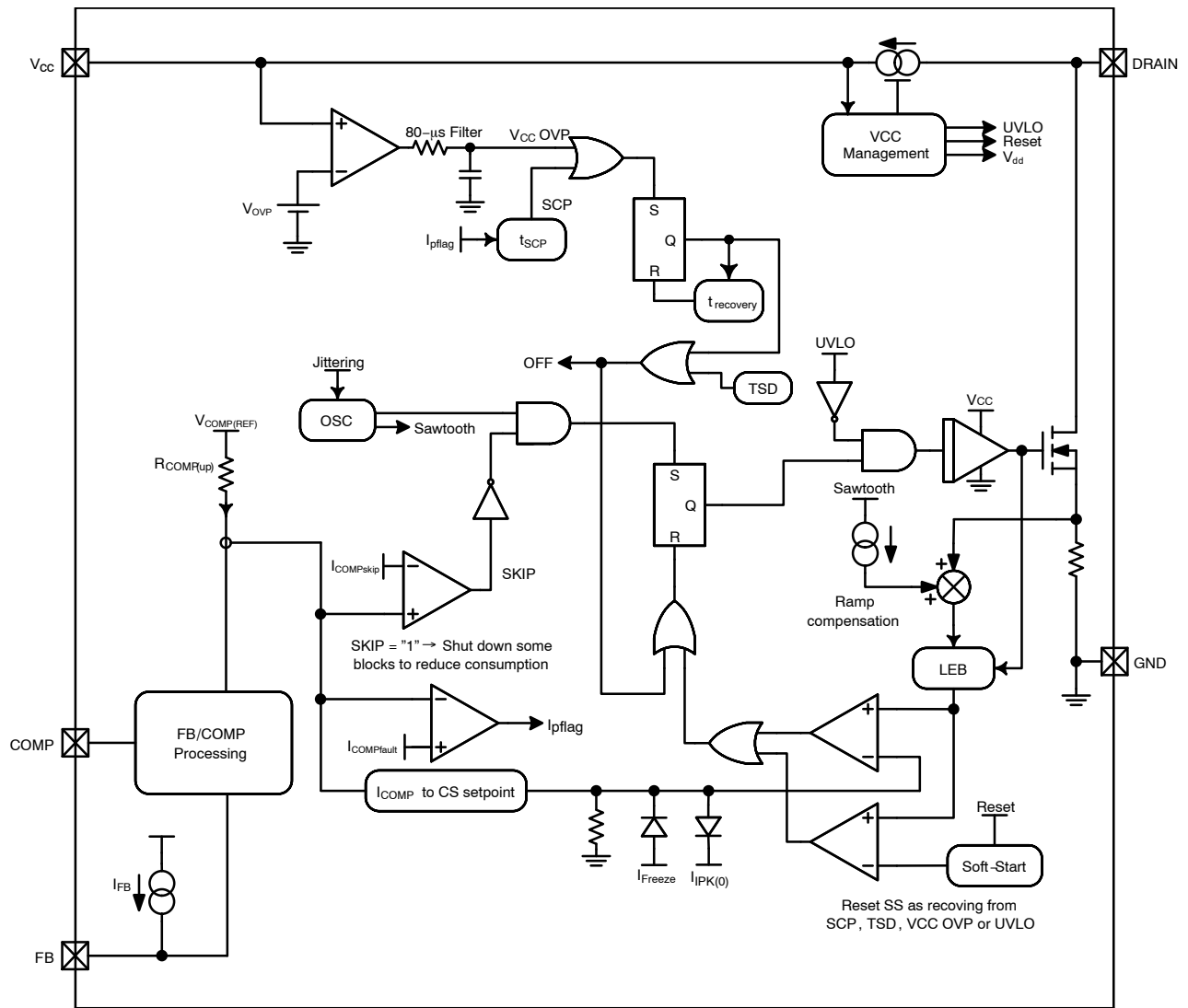


Figure 3. Simplified Internal Circuit Architecture

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## MAXIMUM RATINGS (All voltages related to GND terminal)

Symbol	Parameter	Rating	Units
$V_{CC}$	Power supply voltage, $V_{CC}$ pin, continuous voltage	-0.3 to 20	V
$V_{inmax}$	Voltage on all pins, except Drain and $V_{CC}$ pin	-0.3 to 10	V
$BV_{dss}$	Drain voltage	-0.3 to 700	V
$I_{CC}$	Maximum Current into $V_{CC}$ pin	10	mA
$I_{DS(PK)}$	Drain Current Peak during Transformer Saturation ( $T_J = 150^\circ\text{C}$ ):		
	NCP10670	300	mA
	NCP10671	300	mA
	NCP10672	850	mA
	Drain Current Peak during Transformer Saturation ( $T_J = 125^\circ\text{C}$ ):		
	NCP10670	335	mA
	NCP10671	335	mA
	NCP10672	950	mA
	Drain Current Peak during Transformer Saturation ( $T_J = 25^\circ\text{C}$ ):		
NCP10670	520	mA	
NCP10671	520	mA	
NCP10672	1500	mA	
$R_{\theta J-A}$	Thermal Resistance Junction-to-Air – NCP10670(1) SOIC7 with 200 mm <sup>2</sup> of 35- $\mu$ copper area	116	$^\circ\text{C}/\text{W}$
$R_{\theta J-A}$	Thermal Resistance Junction-to-Air – NCP10672 SOIC7 with 200 mm <sup>2</sup> of 35- $\mu$ copper area	102	$^\circ\text{C}/\text{W}$
$T_{JMAX}$	Maximum Junction Temperature	150	$^\circ\text{C}$
	Storage Temperature Range	-60 to +150	$^\circ\text{C}$
HBM	Human Body Model ESD Capability per JEDEC JESD22-A114F	2	kV
CDM	Charged-Device Model ESD Capability per JEDEC JESD22-C101E	1	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. This device contains latch-up protection and exceeds 100 mA per JEDEC Standard JESD78.

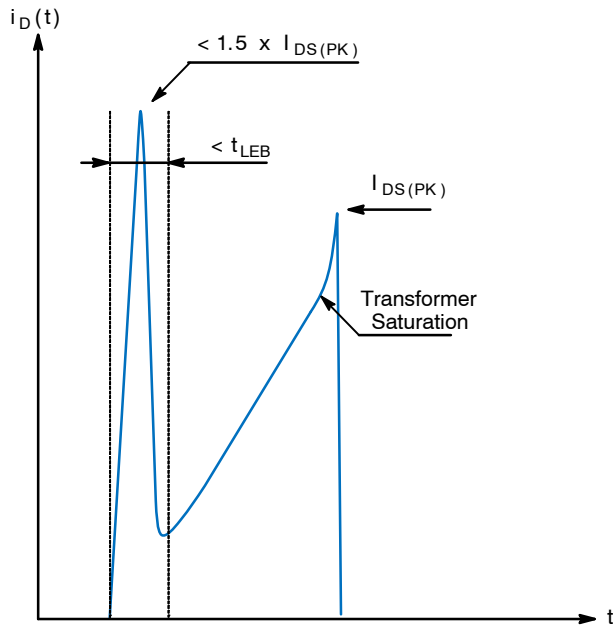


Figure 4. Spike Limits

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## ELECTRICAL CHARACTERISTICS

(T<sub>j</sub> = 25°C, for min/max values T<sub>j</sub> = -40°C to +125°C, V<sub>CC</sub> = 14 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
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### SUPPLY SECTION AND V<sub>CC</sub> MANAGEMENT

V <sub>CC(on)</sub>	V <sub>CC</sub> increasing level at which the switcher starts operation	1	8.4	9.0	9.5	V
V <sub>CC(min)</sub>	V <sub>CC</sub> decreasing level at which the HV current source restarts	1	7.0	7.5	7.8	V
V <sub>CC(off)</sub>	V <sub>CC</sub> decreasing level at which the switcher stops operation (UVLO)	1	6.7	7.0	7.2	V
I <sub>CC1</sub>	Internal IC consumption, NCP10670 switching at 60 kHz Internal IC consumption, NCP10670 switching at 100 kHz Internal IC consumption, NCP10671 switching at 60 kHz Internal IC consumption, NCP10671 switching at 100 kHz Internal IC consumption, NCP10672 switching at 60 kHz Internal IC consumption, NCP10672 switching at 100 kHz	1	-	0.84 0.88 0.84 0.88 0.91 1.00	1.05 1.10 1.05 1.10 1.15 1.25	mA
I <sub>CCskip</sub>	Internal IC consumption, COMP is 0 V (No switching on MOSFET)	1	-	340	-	μA

### POWER SWITCH CIRCUIT

R <sub>DS(on)</sub>	Power Switch Circuit on-state resistance NCP10670, NCP10671 (I <sub>d</sub> = 50 mA) T <sub>j</sub> = 25°C T <sub>j</sub> = 125°C NCP10672 (I <sub>d</sub> = 50 mA) T <sub>j</sub> = 25°C T <sub>j</sub> = 125°C	4	-	34 65	41 72	Ω Ω
BV <sub>DSS</sub>	Power Switch Circuit & Startup breakdown voltage (I <sub>D(off)</sub> = 120 μA, T <sub>j</sub> = 25°C)	4	700	-	-	V
I <sub>DSS(off)</sub>	Power Switch & Startup breakdown voltage off-state leakage current T <sub>j</sub> = 125°C (V <sub>ds</sub> = 700 V) T <sub>j</sub> = 25°C (V <sub>ds</sub> = 700 V)	4	-	7 1	-	μA μA
t <sub>r</sub> t <sub>f</sub>	Switching characteristics (R <sub>L</sub> = 50 Ω, V <sub>DS</sub> set for I <sub>drain</sub> = 0.7 × I <sub>lim</sub> ) Turn-on time (90% - 10%) Turn-off time (10% - 90%)	4	-	20 10	-	ns ns
t <sub>on(min)</sub>	Minimum on time NCP10670 NCP10671 NCP10672	4	-	200 200 230	-	ns ns ns

### INTERNAL START-UP CURRENT SOURCE

I <sub>start1</sub>	High-voltage current source, V <sub>CC</sub> = V <sub>CC(on)</sub> - 200 mV	4	4	8	12	mA
I <sub>start2</sub>	High-voltage current source, V <sub>CC</sub> = 0 V	4	-	0.4	-	mA
V <sub>CCTH</sub>	V <sub>CC</sub> Transient level for I <sub>start1</sub> to I <sub>start2</sub> toggling point	1	-	1.2	-	V
V <sub>start(min)</sub>	Minimum startup voltage, V <sub>CC</sub> = 0 V	4	-	-	22	V

### CURRENT COMPARATOR

I <sub>IPK</sub>	Maximum internal current setpoint at 50% duty cycle FB = 2 V, T <sub>j</sub> = 25°C NCP10670 NCP10671 NCP10672	-	-	83 208 650	-	mA mA mA
I <sub>IPK(0)</sub>	Maximum internal current setpoint at beginning of switching cycle FB = 2 V, T <sub>j</sub> = 25°C NCP10670 NCP10671 NCP10672	-	85 223 702	100 250 780	115 277 858	mA mA mA
I <sub>IPKSW</sub>	Final switch current with a primary slope of 200 mA/μs, F <sub>SW</sub> = 60 kHz (Note 3) NCP10670 NCP10671 NCP10672	-	-	120 258 740	-	mA mA mA

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## ELECTRICAL CHARACTERISTICS

(T<sub>j</sub> = 25°C, for min/max values T<sub>j</sub> = -40°C to +125°C, V<sub>cc</sub> = 14 V unless otherwise noted) (continued)

Symbol	Rating	Pin	Min	Typ	Max	Unit
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### CURRENT COMPARATOR

I <sub>PKSW</sub>	Final switch current with a primary slope of 200 mA/μs, F <sub>SW</sub> = 100 kHz (Note 3) NCP10670 NCP10671 NCP10672		-	120 250 710	-	mA mA mA
t <sub>SS</sub>	Soft-start duration (guaranteed by design)	-	-	4	-	ms
t <sub>prop</sub>	Propagation delay from current detection to drain OFF state	-	-	70	-	ns
t <sub>LEB</sub>	Leading Edge Blanking Duration NCP10670 NCP10671 NCP10672	-	-	130 130 160	-	ns ns ns

### INTERNAL OSCILLATOR

f <sub>OSC</sub>	Oscillation frequency, 60 kHz version, T <sub>j</sub> = 25°C (Note 4)	-	54	60	66	kHz
f <sub>OSC</sub>	Oscillation frequency, 100 kHz version, T <sub>j</sub> = 25°C (Note 4)	-	90	100	110	kHz
f <sub>jitter</sub>	Frequency jittering in percentage of f <sub>OSC</sub>	-	-	±6	-	%
f <sub>swing</sub>	Jittering swing frequency	-	-	300	-	Hz
D <sub>max</sub>	Maximum duty-cycle	-	62	66	72	%

### ERROR AMPLIFIER SECTION

V <sub>REF</sub>	Voltage Feedback Input (V <sub>COMP</sub> = 2.5 V)	8	3.2	3.3	3.4	V
I <sub>FB</sub>	Input Bias Current (V <sub>FB</sub> = 3.3 V)	8	-	1	-	μA
G <sub>M</sub>	Transconductance	2	-	2	-	mS
I <sub>OTAlim</sub>	OTA maximum current capability (V <sub>FB</sub> > V <sub>OTAen</sub> )	2	-	+150/-150	-	μA
V <sub>OTAen</sub>	FB voltage to disable OTA	8	0.7	1.3	1.7	V

### COMPENSATION SECTION

I <sub>COMPfault</sub>	COMP current for which Fault is detected	2	-	-40	-	μA
I <sub>COMP100%</sub>	COMP current for which internal current set-point is 100% (I <sub>PK(0)</sub> )	2	-	-44	-	μA
I <sub>COMPfreeze</sub>	COMP current for which internal current set-point is: I <sub>Freeze1, 2 or 3</sub> (NCP10670/1/2)	2	-	-80	-	μA
V <sub>COMP(REF)</sub>	Equivalent pull-up voltage in linear regulation range (Guaranteed by design)	2	-	2.7	-	V
R <sub>COMP(up)</sub>	Equivalent feedback resistor in linear regulation range (Guaranteed by design)	2	-	17.7	-	kΩ

### SKIP CYCLE

I <sub>COMPskip</sub>	The COMP pin current level to enter skip mode	2	-	-120	-	μA
I <sub>Freeze1</sub>	Internal minimum current setpoint (I <sub>COMP</sub> = I <sub>COMPFreeze</sub> ) in NCP10670	-	-	35	-	mA
I <sub>Freeze2</sub>	Internal minimum current setpoint (I <sub>COMP</sub> = I <sub>COMPFreeze</sub> ) in NCP10671	-	-	92	-	mA
I <sub>Freeze3</sub>	Internal minimum current setpoint (I <sub>COMP</sub> = I <sub>COMPFreeze</sub> ) in NCP10672	-	-	270	-	mA

### RAMP COMPENSATION

S <sub>a(60)</sub>	The internal ramp compensation @ 60 kHz: NCP10670 NCP10671 NCP10672	-	-	2.8 8.4 15.6	-	mA/μs mA/μs mA/μs
S <sub>a(100)</sub>	The internal ramp compensation @ 100 kHz: NCP10670 NCP10671 NCP10672	-	-	4.7 14 26	-	mA/μs mA/μs mA/μs



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## ELECTRICAL CHARACTERISTICS

(T<sub>j</sub> = 25°C, for min/max values T<sub>j</sub> = -40°C to +125°C, V<sub>CC</sub> = 14 V unless otherwise noted) (continued)

Symbol	Rating	Pin	Min	Typ	Max	Unit
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### PROTECTIONS

t <sub>SCP</sub>	Fault validation further to error flag assertion	-	35	48	-	ms
t <sub>recovery</sub>	OFF phase in fault mode	-	-	400	-	ms
V <sub>OVP</sub>	V <sub>CC</sub> voltage at which the switcher stops pulsing	1	17.0	18.0	18.8	V
t <sub>OVP</sub>	The filter of V <sub>CC</sub> OVP comparator	-	-	80	-	μs

### TEMPERATURE MANAGEMENT

TSD	Temperature shutdown (Guaranteed by design)	-	150	163	-	°C
TSD <sub>HYST</sub>	Hysteresis in shutdown (Guaranteed by design)	-	-	20	-	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- The final switch current is:  $I_{PK(0)} / (V_{in}/L_P + S_a) \times V_{in}/L_P + V_{in}/L_P \times t_{prop}$ , with S<sub>a</sub> the built-in slope compensation, V<sub>in</sub> the input voltage, L<sub>P</sub> the primary inductor in a flyback, and t<sub>prop</sub> the propagation delay..
- Oscillator frequency is measured with disabled jittering.

## TYPICAL CHARACTERISTICS

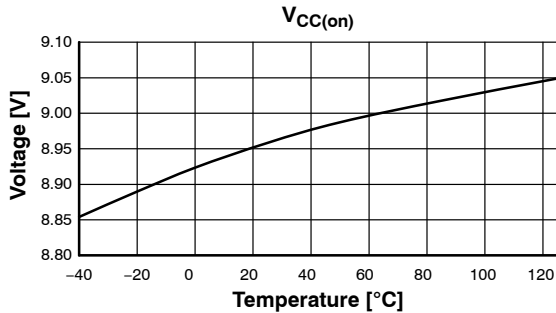


Figure 5. V<sub>CC(on)</sub> vs. Temperature

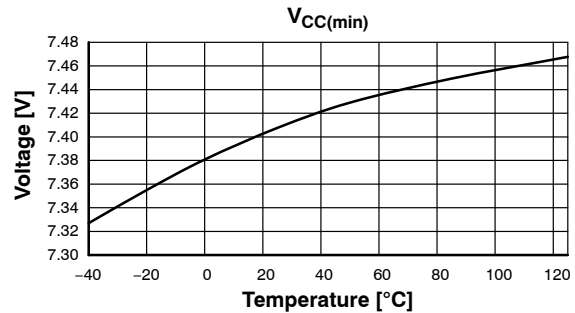


Figure 6. V<sub>CC(min)</sub> vs. Temperature

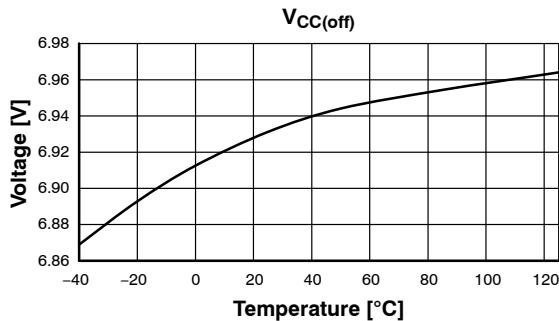


Figure 7. V<sub>CC(off)</sub> vs. Temperature

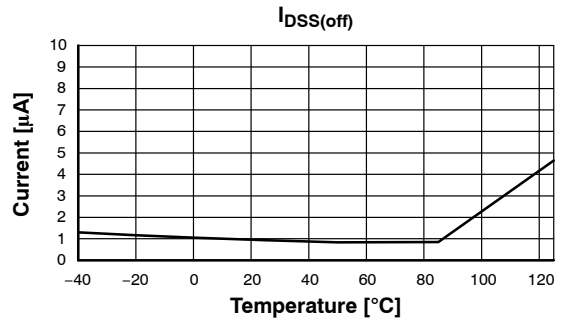


Figure 8. I<sub>DSS(off)</sub> vs. Temperature

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## TYPICAL CHARACTERISTICS (continued)

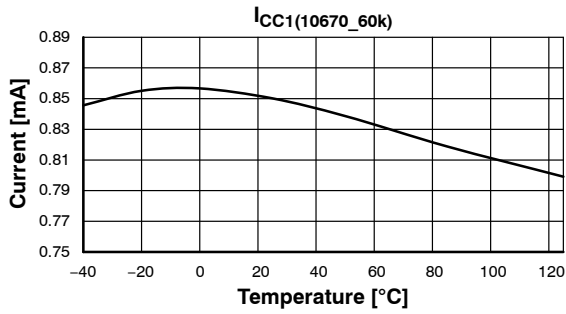


Figure 9.  $I_{CC1}(10670_{60k})$  vs. Temperature

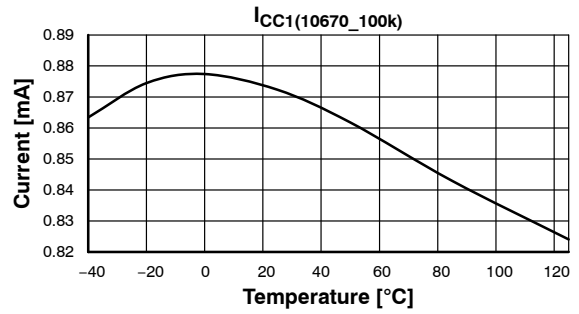


Figure 10.  $I_{CC1}(NCP10670_{100k})$  vs. Temperature

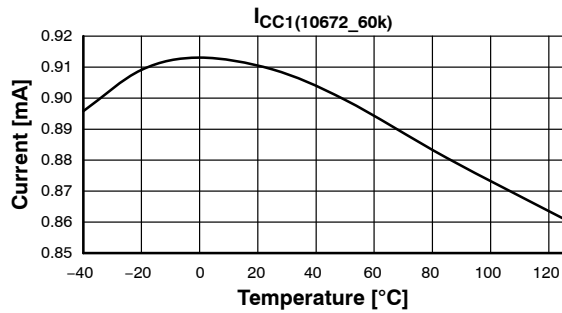


Figure 11.  $I_{CC1}(10672_{60k})$  vs. Temperature

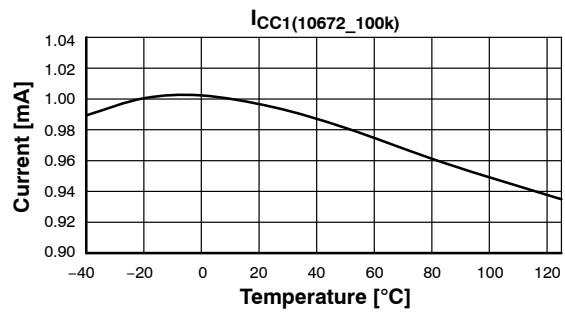


Figure 12.  $I_{CC1}(10672_{100k})$  vs. Temperature

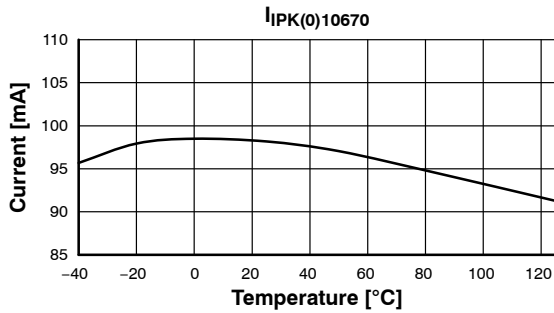


Figure 13.  $I_{PK(0)10670}$  vs. Temperature

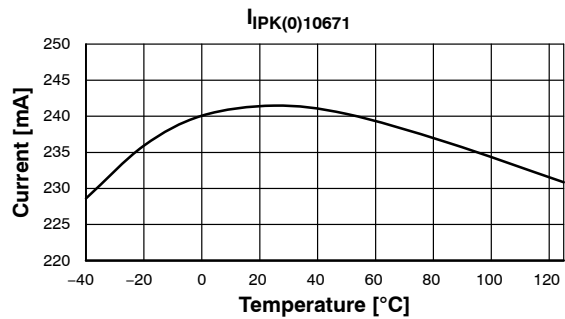


Figure 14.  $I_{PK(0)10671}$  vs. Temperature

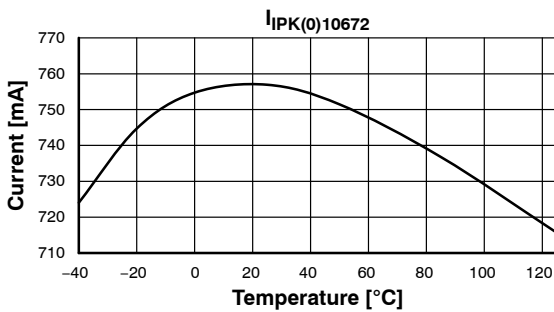


Figure 15.  $I_{PK(0)10672}$  vs. Temperature

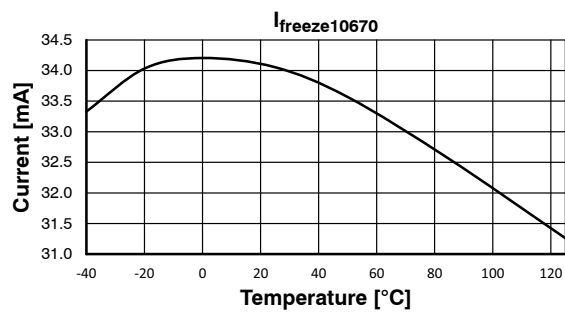


Figure 16.  $I_{freeze10670}$  vs. Temperature

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## TYPICAL CHARACTERISTICS (continued)

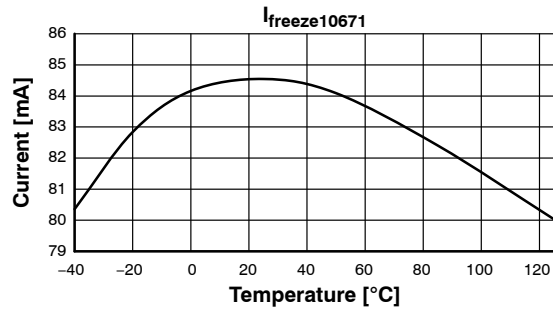


Figure 17.  $I_{freeze10671}$  vs. Temperature

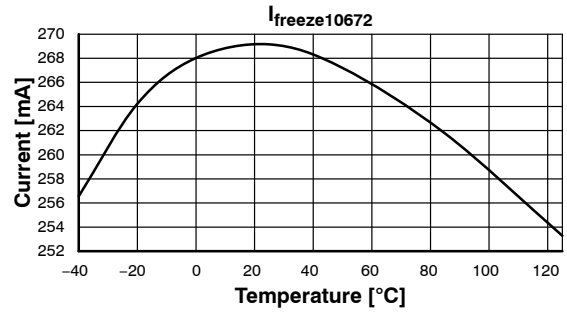


Figure 18.  $I_{freeze10672}$  vs. Temperature

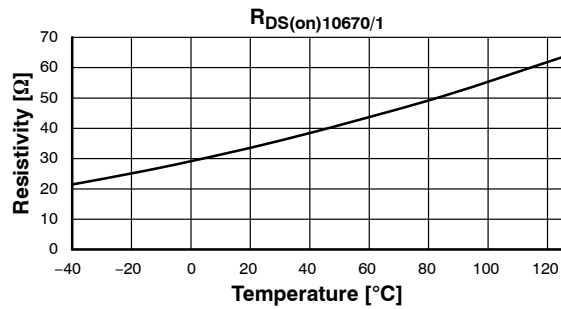


Figure 19.  $R_{DS(on)10670/1}$  vs. Temperature

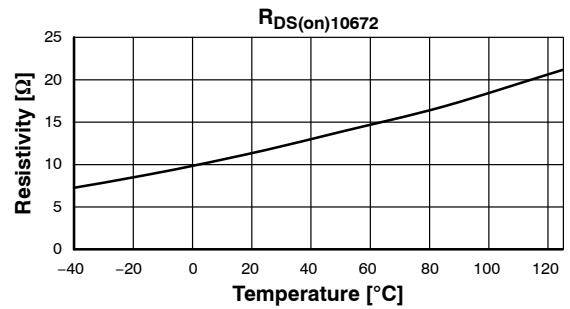


Figure 20.  $R_{DS(on)10672}$  vs. Temperature

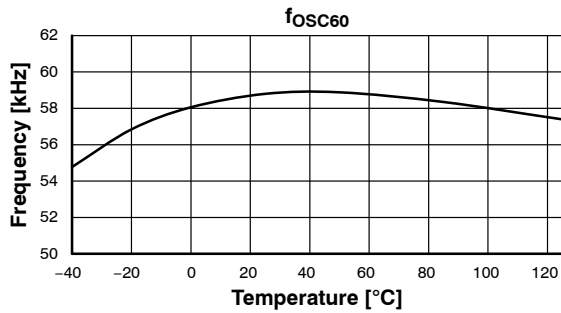


Figure 21.  $f_{osc60}$  vs. Temperature

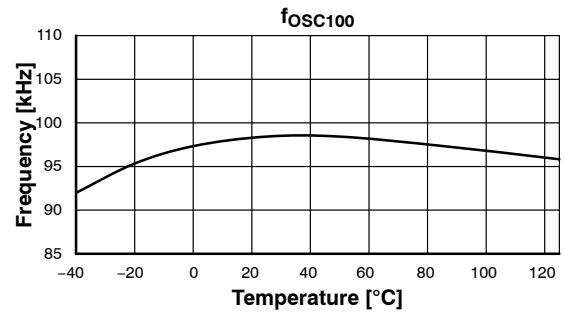


Figure 22.  $f_{osc100}$  vs. Temperature

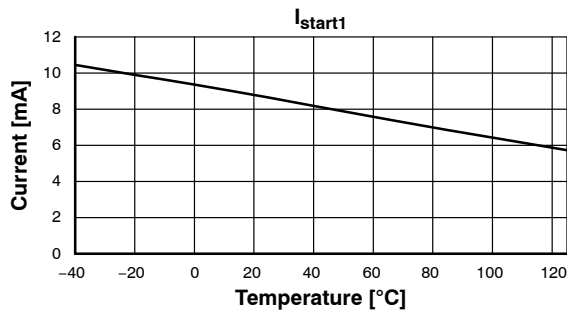


Figure 23.  $I_{start1}$  vs. Temperature

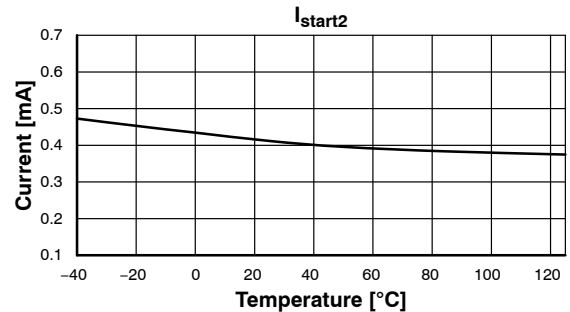


Figure 24.  $I_{start2}$  vs. Temperature

TYPICAL CHARACTERISTICS (continued)

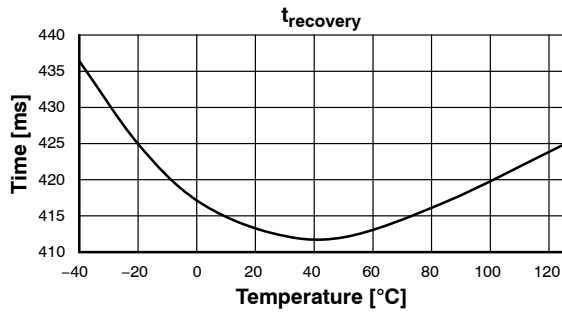


Figure 25.  $t_{\text{recovery}}$  vs. Temperature

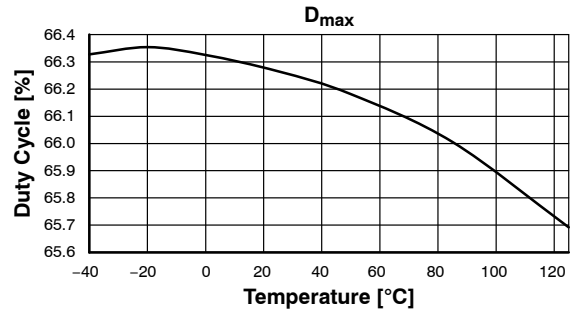


Figure 26.  $D_{\text{(max)}}$  vs. Temperature

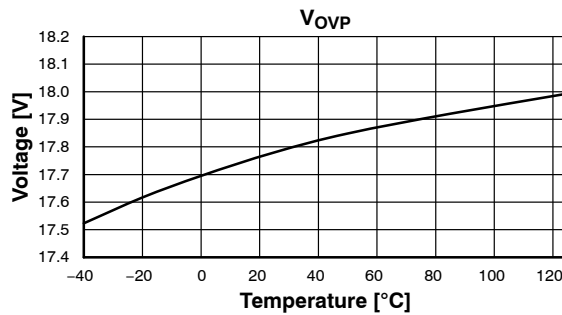


Figure 27.  $V_{\text{OVP}}$  vs. Temperature

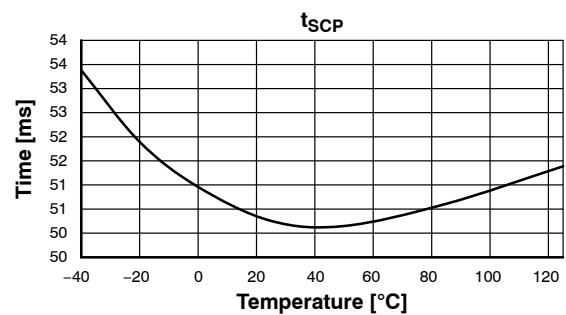


Figure 28.  $t_{\text{SCP}}$  vs. Temperature

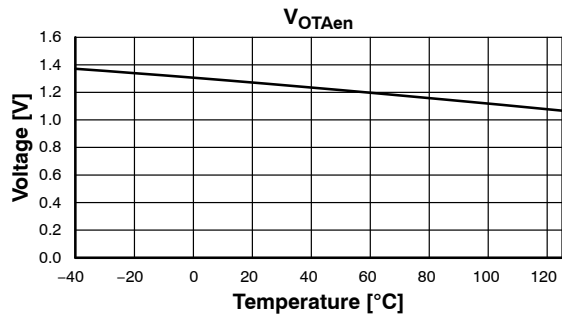


Figure 29.  $V_{\text{OTAen}}$  vs. Temperature

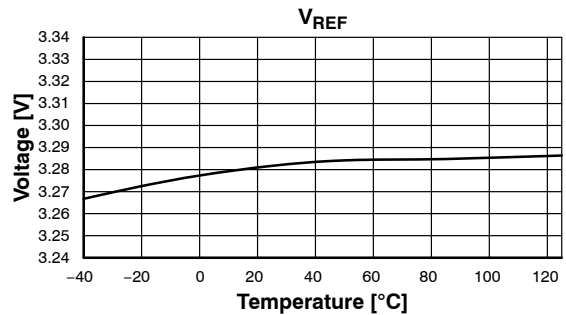


Figure 30.  $V_{\text{REF}}$  vs. Temperature

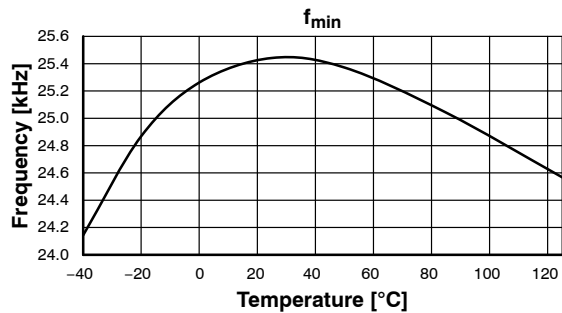


Figure 31.  $f_{\text{min}}$  vs. Temperature

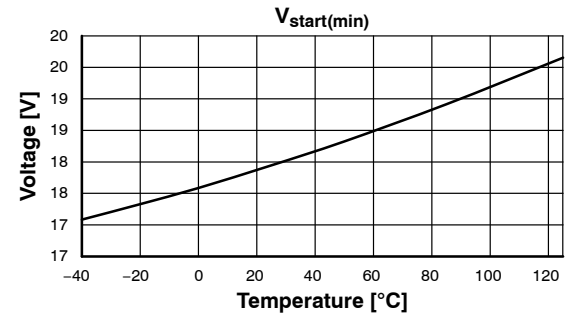


Figure 32.  $V_{\text{start(min)}}$  vs. Temperature



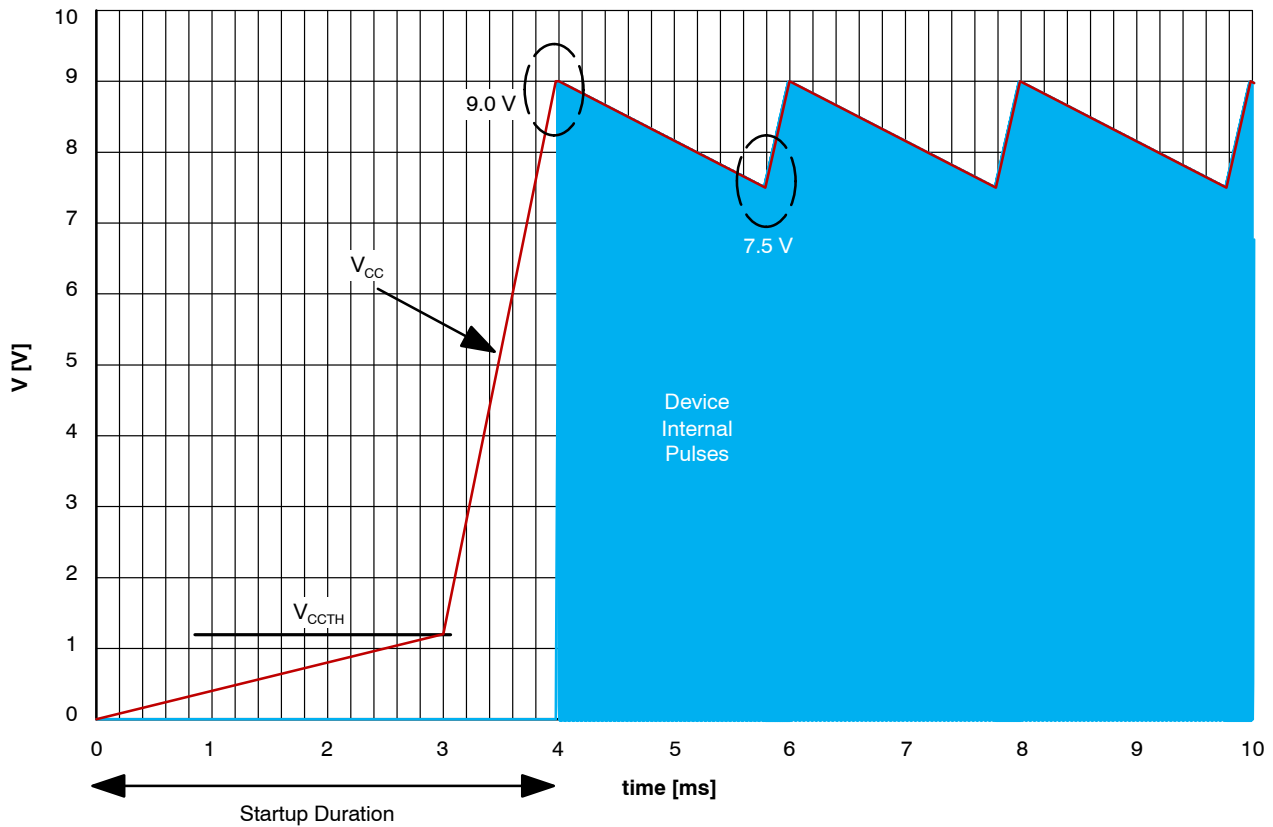


Figure 34. The Charge/Discharge Cycle Over a 1  $\mu$ F  $V_{CC}$  Capacitor

As one can see, even if there is auxiliary winding to provide energy for  $V_{CC}$ , it happens that the device is still biased by DSS during start-up time or some fault mode when the voltage on auxiliary winding is not ready yet. The  $V_{CC}$  capacitor shall be dimensioned to avoid  $V_{CC}$  crosses  $V_{CC(off)}$  level, which stops operation. The  $\Delta V$  between  $V_{CC(min)}$  and  $V_{CC(off)}$  is 0.5 V. There is no current source to charge  $V_{CC}$  capacitor when driver is on, i.e. drain voltage is close to zero. Hence the  $V_{CC}$  capacitor can be calculated using

$$C_{VCC} \geq \frac{I_{CC1} D_{max}}{f_{OSC} \cdot \Delta V} \quad (\text{eq. 1})$$

Take the 60 kHz device as an example.  $C_{VCC}$  should be above

$$\frac{0.84 \text{ m} \cdot 72\%}{54 \text{ kHz} \cdot 0.5} = 22 \text{ nF} \quad (\text{eq. 2})$$

A margin that covers the temperature drift and the voltage drop due to switching inside FET should be considered, and thus a capacitor above 0.1  $\mu$ F is appropriate.

The  $V_{CC}$  capacitor has only a supply role and its value does not impact other parameters such as fault duration or the frequency sweep period for instance. As one can see on Figure 33, an internal OVP comparator, protects the switcher against lethal  $V_{CC}$  runaways. This situation can occur if the feedback loop optocoupler fails, for instance, and you would like to protect the converter against an over voltage event. In that case, the over voltage protection (OVP) circuit and immediately stops the output pulses for  $t_{recovery}$  duration (400 ms typically). Then a new start-up attempt takes place to check whether the fault has disappeared or not. The OVP paragraph gives more design details on this particular section.

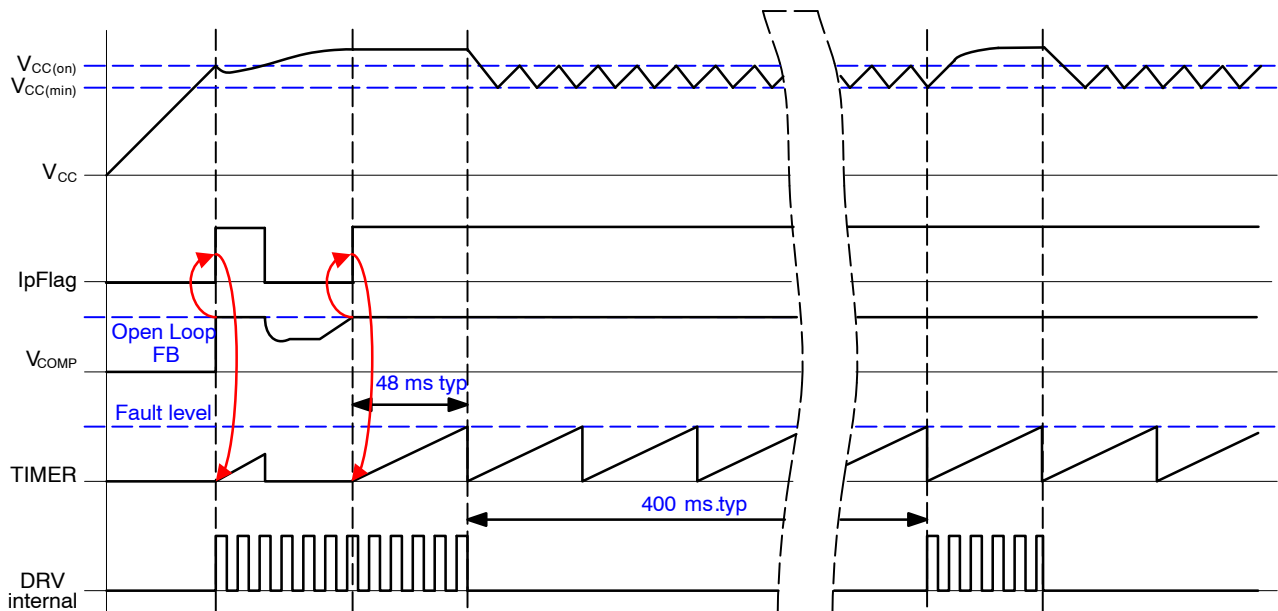
**Fault Condition – Short-circuit on V<sub>CC</sub>**

In some fault situations, a short-circuit can purposely occur between V<sub>CC</sub> and GND. In high line conditions (V<sub>HV</sub> = 370 V<sub>DC</sub>) the current delivered by the startup device will seriously increase the junction temperature. For instance, since I<sub>start1</sub> equals 4 mA (the min corresponds to the highest T<sub>j</sub>), the device would dissipate 370 · 4 = 1.48 W. To avoid this situation, the controller includes a novel circuitry made of two startup levels, I<sub>start1</sub> and I<sub>start2</sub>. At power-up, as long as V<sub>CC</sub> is below a 1.2 V level, the source delivers I<sub>start2</sub> (around 400 μA typical), then, when V<sub>CC</sub> reaches 1.2 V, the source smoothly transitions to I<sub>start1</sub> and delivers its nominal value. As a result, in case of short-circuit between V<sub>CC</sub> and GND, the power dissipation will drop to 370 · 400 μ = 148 mW. Figure 34 portrays this particular behavior.

The first startup period is calculated by the formula  $C \cdot V = I \cdot t$ , which implies a  $1 \mu \cdot 1.2 / 400 \mu = 3 \text{ ms}$  startup time for the first sequence. The second sequence is obtained by toggling the source to 8 mA with a delta V of  $V_{CC(on)} - V_{CC(TH)} = 9.0 - 1.2 = 7.8 \text{ V}$ , which finally leads to a second startup time of  $1 \mu \cdot 7.8 / 8 \text{ m} = 975 \mu\text{s}$ . The total startup time becomes  $3 \text{ m} + 0.975 \text{ m} = 3.975 \text{ ms}$ . Please note that this calculation is approximated by the presence of the knee in the vicinity of the transition.

**Fault Condition – Output Short-circuit**

As soon as V<sub>CC</sub> reaches V<sub>CC(on)</sub>, drive pulses are internally enabled. If everything is correct, the auxiliary winding increases the voltage on the V<sub>CC</sub> pin as the output voltage rises. During the start-sequence, the controller smoothly ramps up the peak drain current to maximum setting, i.e. I<sub>PK</sub>, which is reached after a typical period of 4 ms. When the output voltage is not regulated, the current coming through COMP pin is below I<sub>COMPfault</sub> level (40 μA typically), which is not only during the startup period but also anytime an overload occurs, an internal error flag is asserted, Ipflag, indicating that the system has reached its maximum current limit set point. The assertion of this flag triggers a fault counter t<sub>SCP</sub> (48 ms typically). If at counter completion, Ipflag remains asserted, all driving pulses are stopped and the part stays off in t<sub>recovery</sub> duration (about 400 ms). A new attempt to re-start occurs and will last 48 ms providing the fault is still present. If the fault still affects the output, a safe burst mode is entered, affected by a low duty-cycle operation (11%). When the fault disappears, the power supply quickly resumes operation. Figure 35 depicts this particular mode:



**Figure 35. In Case of Short-circuit or Overload, the NCP1067X Protects Itself and the Power Supply via a Low Frequency Burst Mode. The V<sub>CC</sub> is Maintained by the Current Source and Self-supplies the Controller.**





## NCP10670B, NCP10671B, NCP10672B

### Soft-start

The NCP1067X features a 4 ms soft-start which reduces the power-on stress but also contributes to lower the output overshoot. Figure 38 shows a typical operating waveform.

The NCP1067X features a novel patented structure which offers a better soft-start ramp, almost ignoring the start-up pedestal inherent to traditional current-mode supplies:

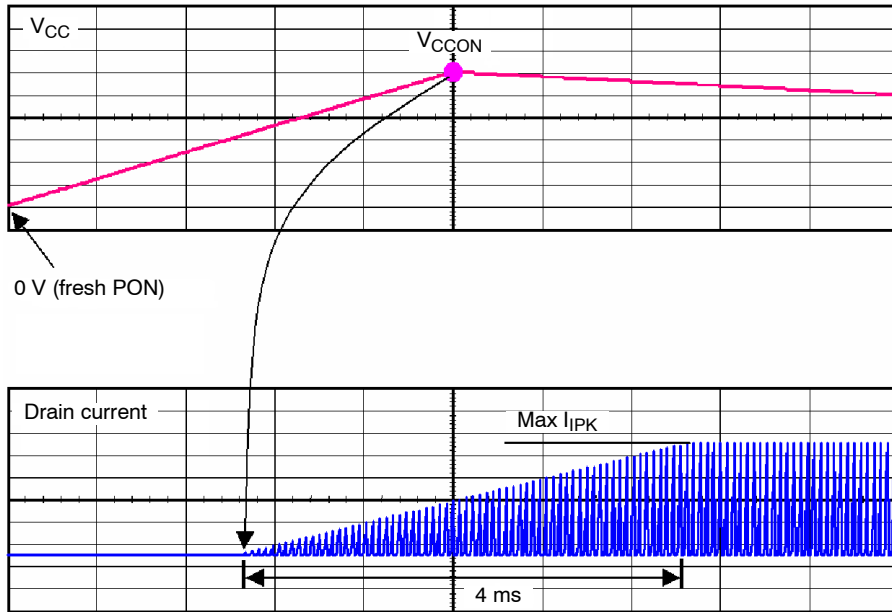


Figure 38. The 4 ms Soft-start Sequence

### Jittering

Frequency jittering is a method used to soften the EMI signature by spreading the energy in the vicinity of the main switching component. The NCP1067X offers a  $\pm 6\%$  deviation of the nominal switching frequency. The sweep

sawtooth is internally generated and modulates the clock up and down with a fixed frequency of 300 Hz. Figure 39 shows the relationship between the jitter ramp and the frequency deviation. It is not possible to externally disable the jitter.

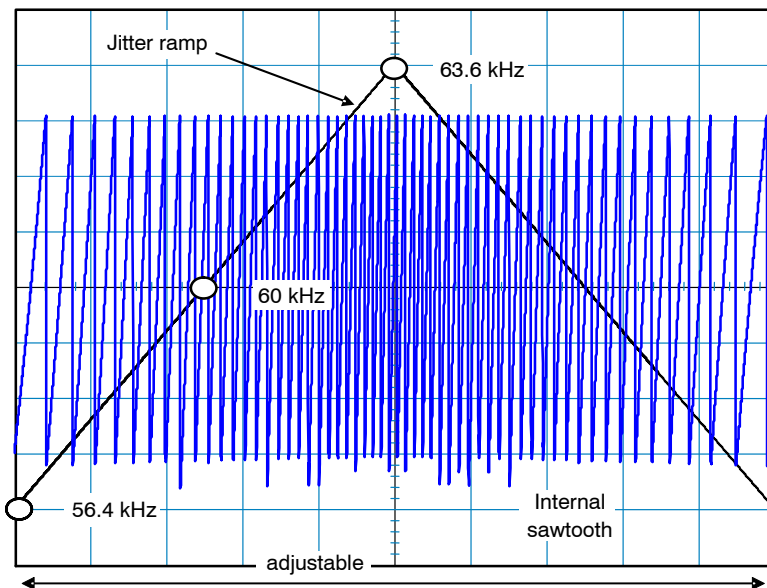


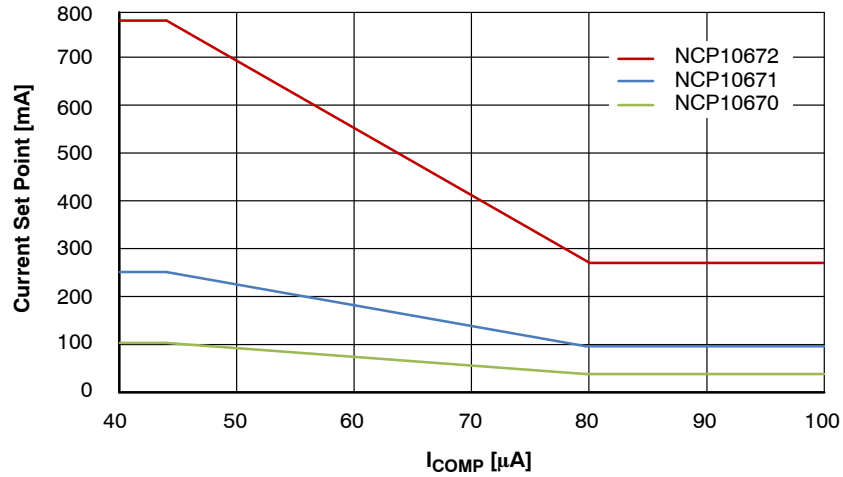
Figure 39. Modulation Effects on the Clock Signal by the Jittering Sawtooth

## NCP10670B, NCP10671B, NCP10672B

### *I<sub>pk</sub> Reduction*

The internal peak current set-point is following the COMP current information until its level reaches  $I_{\text{Freeze}}$ . Below this value, the peak current setpoint is frozen to 30% of the  $I_{\text{PK}(0)}$ . This value is reached at a COMP current level

of  $I_{\text{COMPskip}}$  (120  $\mu\text{A}$  typically). Below this point, if the output power continues to decrease, the part enters skip cycle for the best performance in no-load conditions. Figure 40 depict the adopted scheme for the part.

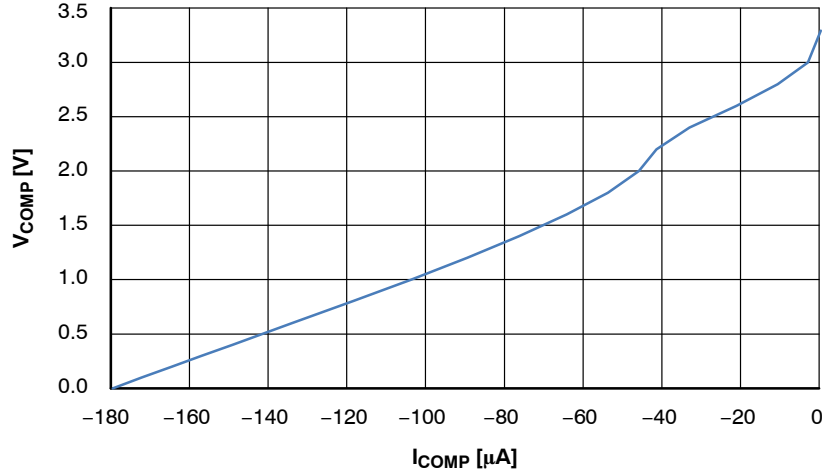


**Figure 40. I<sub>PK</sub> Set-point is Frozen at Lower Power Demand**

### *Feedback and Skip*

Figure 41 depicts the relationship between COMP pin voltage and current. The COMP pin operates linearly as the absolute value of COMP current ( $I_{\text{COMP}}$ ) is above 40  $\mu\text{A}$ . In

this linear operating range, the dynamic resistance is 17.7  $\text{k}\Omega$  typically ( $R_{\text{COMP(up)}}$ ) and the effective pull up voltage is 2.7 V typically ( $V_{\text{COMP(REF)}}$ ). When  $I_{\text{COMP}}$  is decreases, the COMP voltage will increase to 3.2 V.

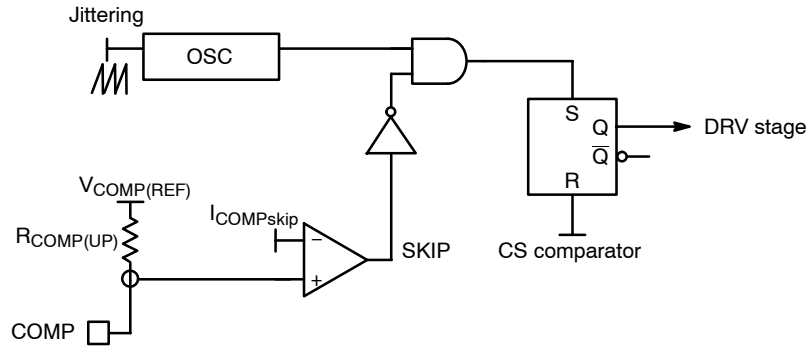


**Figure 41. COMP Pin Voltage vs. Current**

## NCP10670B, NCP10671B, NCP10672B

Figure 42 depicts the skip mode block diagram. When the COMP current information reaches  $I_{COMPskip}$ , the internal clock to set the flip-flop is blanked and the internal consumption of the controller is decreased. The hysteresis of

internal skip comparator is minimized to lower the ripple of the auxiliary voltage for  $V_{CC}$  pin and  $V_{OUT}$  of power supply during skip mode. It eases the design of  $V_{CC}$  over load range.



**Figure 42. Skip Cycle Schematic**

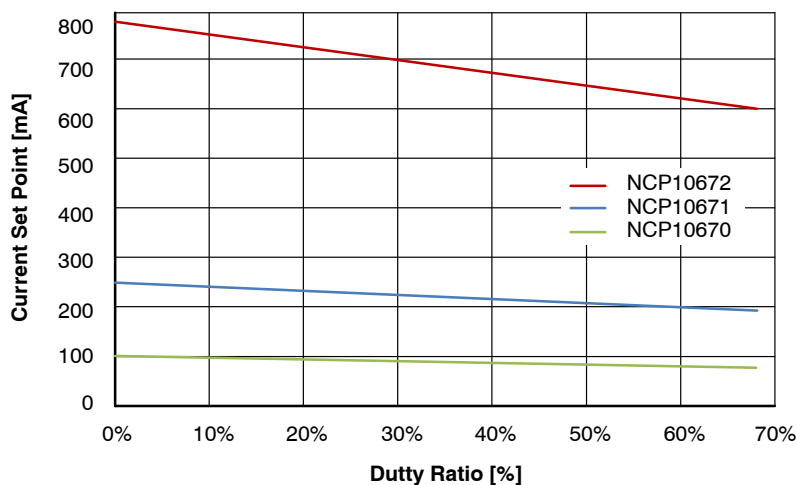
### Ramp Compensation and $I_{PK}$ Set-point

In order to allow the NCP106X to operate in CCM with a duty cycle above 50%, a fixed slope compensation is internally applied to the current-mode control.

Here we got a table of the ramp compensation, the initial current set point, and the final current set-point of different versions of switcher.

	NCP10670		NCP10671		NCP10672	
	60 kHz	100 kHz	60 kHz	100 kHz	60 kHz	100 kHz
$F_{sw}$	60 kHz	100 kHz	60 kHz	100 kHz	60 kHz	100 kHz
$S_a$	2.8 mA/μs	4.7 mA/μs	8.4 mA/μs	14 mA/μs	15.6 mA/μs	26 mA/μs
$I_{PK}(Duty = 50\%)$	83 mA		208 mA		650 mA	
$I_{PK(0)}$	100 mA		250 mA		780 mA	

Figure 43 depicts the variation of  $I_{PK}$  set-point vs. the power switcher duty ratio, which is caused by the internal ramp compensation.

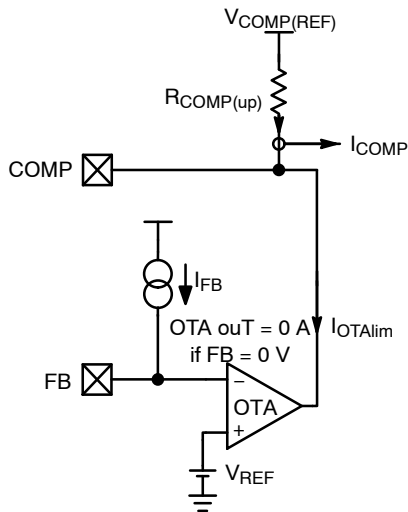


**Figure 43.  $I_{PK}$  Set-point Varies with Power Switch on Time, Which is Caused by the Ramp Compensation**

**FB pin function**

The FB pin is used in non isolated SMPS application only. Portion of the output voltage is connected into the pin. The voltage is compared with internal  $V_{REF}$  (3.3 V) using Operation Transconductance Amplifier (Figure 44). The OTAs output is connected to COMP pin. From the outside an user defined compensation network is connected to the COMP pin. The current capability of OTA is limited to  $-150 \mu A$  typically. The positive current is defined by internal  $R_{COMP(up)}$  resistor and  $V_{COMP(ref)}$  voltage. If FB path loop is broken (i.e. the FB pin is disconnected), an internal current  $I_{FB}$  ( $1 \mu A$  typ.) will pull up the FB pin and the IC stops switching to avoid uncontrolled output voltage increasing.

In isolated topology, the FB pin should be connected to GND pin. In this configuration no current flows from OTA to COMP pin (OTA is disabled) so the OTA has no influence on regulation at all.



**Figure 44. FB Pin Connection**

**Design Procedure**

The design of an SMPS around a monolithic device does not differ from that of a standard circuit using a controller and a MOSFET. However, one needs to be aware of certain characteristics specific of monolithic devices. Let us follow the steps:

- $V_{in} \text{ min} = 90 \text{ Vac or } 127 \text{ Vdc}$  once rectified, assuming a low bulk ripple
- $V_{in} \text{ max} = 265 \text{ Vac or } 375 \text{ Vdc}$
- $V_{out} = 12 \text{ V}$
- $P_{out} = 5 \text{ W}$
- Operating mode is CCM
- $\eta = 0.8$

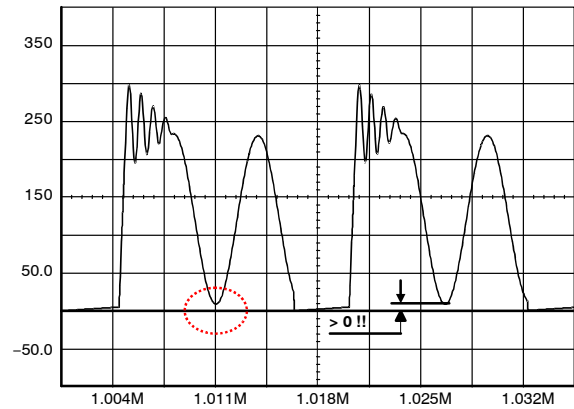
1. The lateral MOSFET body-diode shall never be forward biased, either during start-up (because of a large leakage inductance) or in normal operation as shown in Figure 45. This condition sets the maximum voltage that can be reflected during  $t_{off}$ . As a result, the Flyback voltage which is reflected on the drain at the switch opening cannot be larger than the input voltage. When selecting components, you thus must adopt a turn ratio which adheres to the following equation:

$$N (V_{out} + V_f) < V_{in, \text{min}} \tag{eq. 3}$$

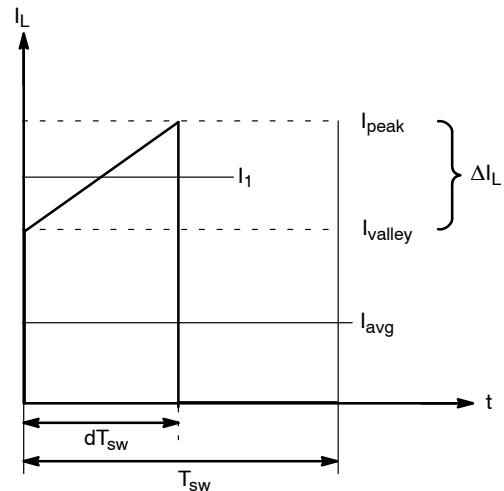
2. In our case, since we operate from a 127 V DC rail while delivering 12 V, we can select a reflected voltage of 120 V dc maximum. Therefore, the turn ratio  $N_p:N_s$  must be smaller than

$$\frac{V_{\text{reflect}}}{V_{out} + V_f} = \frac{120}{12 + 0.5} = 9.6 \tag{eq. 4}$$

or  $N_p:N_s < 9.6$ . Here we choose  $N = 8$  in this case. We will see later on how it affects the calculation.



**Figure 45. The Drain-Source Wave Shall Always be Positive**



**Figure 46. Primary Inductance Current Evolution in CCM**

3. Lateral MOSFETs have a poorly doped body–diode which naturally limits their ability to sustain the avalanche. A traditional RCD clamping network shall thus be installed to protect the MOSFET. In some low power applications, a simple capacitor can also be used since

$$V_{\text{drain,max}} = V_{\text{in}} + N (V_{\text{out}} + V_f) + I_{\text{peak}} \sqrt{\frac{L_f}{C_{\text{tot}}}} \quad (\text{eq. 5})$$

where  $L_f$  is the leakage inductance,  $C_{\text{tot}}$  the total capacitance at the drain node (which is increased by the capacitor you will wire between drain and source),  $N$  the  $N_p:N_s$  turn ratio,  $V_{\text{out}}$  the output voltage,  $V_f$  the secondary diode forward drop and finally,  $I_{\text{peak}}$  the maximum peak current. Worse case occurs when the SMPS is very close to regulation, e.g. the  $V_{\text{out}}$  target is almost reached and  $I_{\text{peak}}$  is still pushed to the maximum. For this design, we have selected our maximum voltage around 650 V (at  $V_{\text{in}} = 375$  Vdc). This voltage is given by the RCD clamp installed from the drain to the bulk voltage. We will see how to calculate it later on.

4. Calculate the maximum operating duty–cycle for this flyback converter operated in CCM:

$$d_{\text{max}} = \frac{N (V_{\text{out}} + V_f)}{N (V_{\text{out}} + V_f) + V_{\text{in,min}}} = \frac{1}{1 + \frac{V_{\text{in,min}}}{N (V_{\text{out}} + V_f)}} = 0.44 \quad (\text{eq. 6})$$

5. To obtain the primary inductance, we have the choice between two equations:

$$L = \frac{(V_{\text{in}} d)^2}{f_{\text{sw}} K P_{\text{in}}} \quad (\text{eq. 7})$$

where

$$K = \frac{\Delta I_L}{I_{\text{Lavg}}} \quad (\text{eq. 8})$$

and defines the amount of ripple we want in CCM (see Figure 46 ).

- *Small K*: deep CCM, implying a large primary inductance, a low bandwidth and a large leakage inductance.
- *Large K*: approaching DCM where the RMS losses are worse, but smaller inductance, leading to a better leakage inductance.

From eq.17, a  $K$  factor of 1 (50% ripple), gives an inductance of:

$$L = \frac{(127 \cdot 0.44)^2}{60k \cdot 1 \cdot 5)} = 10.04 \text{ mH} \quad (\text{eq. 9})$$

$$\Delta I_L = \frac{V_{\text{in}} d}{L f_{\text{SW}}} = \frac{127 \cdot 0.44}{10.04 \text{ m} \cdot 60 \text{ k}} = 92.8 \text{ mA} \quad (\text{eq. 10})$$

peak to peak

The peak current can be evaluated to be:

$$I_{\text{peak}} = \frac{I_{\text{avg}}}{d} + \frac{\Delta I_L}{2} = \frac{49.2 \text{ m}}{0.44} + \frac{92.8 \text{ m}}{2} = 158 \text{ mA} \quad (\text{eq. 11})$$

On ,  $I_L$  can also be calculated:

$$I_{\text{Lavg}} = I_{\text{peak}} - \frac{\Delta I_L}{2} = 158 \text{ m} - \frac{92.8 \text{ m}}{2} = 111.6 \text{ mA} \quad (\text{eq. 12})$$

6. Based on the above numbers, we can now evaluate the conduction losses:

$$I_{\text{d,rms}} = \sqrt{d \left( I_{\text{peak}}^2 - I_{\text{peak}} \Delta I_L + \frac{\Delta I_L^2}{3} \right)} = \sqrt{d \left( I_{\text{peak}}^2 - I_{\text{peak}} \Delta I_L + \frac{\Delta I_L^2}{3} \right)} = 57 \text{ mA} \quad (\text{eq. 13})$$

If we take the maximum  $R_{\text{ds(on)}}$  for a 125°C junction temperature, i.e. 34 Ω, then conduction losses worse case are:

$$P_{\text{cond}} = I_{\text{d,rms}}^2 R_{\text{ds (on)}} = 110 \text{ mW} \quad (\text{eq. 14})$$

7. Off–time and on–time switching losses can be estimated based on the following calculations:

$$P_{\text{off}} = \frac{I_{\text{peak}} (V_{\text{bulk}} + V_{\text{clamp}}) t_{\text{off}}}{2 T_{\text{SW}}} = \frac{0.158 \cdot (127 + 100 \cdot 2) \cdot 10 \text{ n}}{2 \cdot 16.7 \mu} = 15.5 \text{ mW} \quad (\text{eq. 15})$$

Where, assume the  $V_{\text{clamp}}$  is equal to 2 times of reflected voltage.

$$P_{\text{on}} = \frac{I_{\text{valley}} (V_{\text{bulk}} + N (V_{\text{out}} + V_f)) t_{\text{on}}}{6 T_{\text{SW}}} = \frac{0.0464 \cdot (127 + 100 \cdot 2) \cdot 20 \text{ n}}{6 \cdot 16.7 \mu} = 2.1 \text{ mW} \quad (\text{eq. 16})$$

It is noted that the overlap of voltage and current seen on MOSFET during turning on and off duration is dependent on the snubber and parasitic capacitance seen from drain pin. Therefore the  $t_{\text{off}}$  and  $t_{\text{on}}$  in eq. 15 and eq. 16 have to be modified after measuring on the bench.

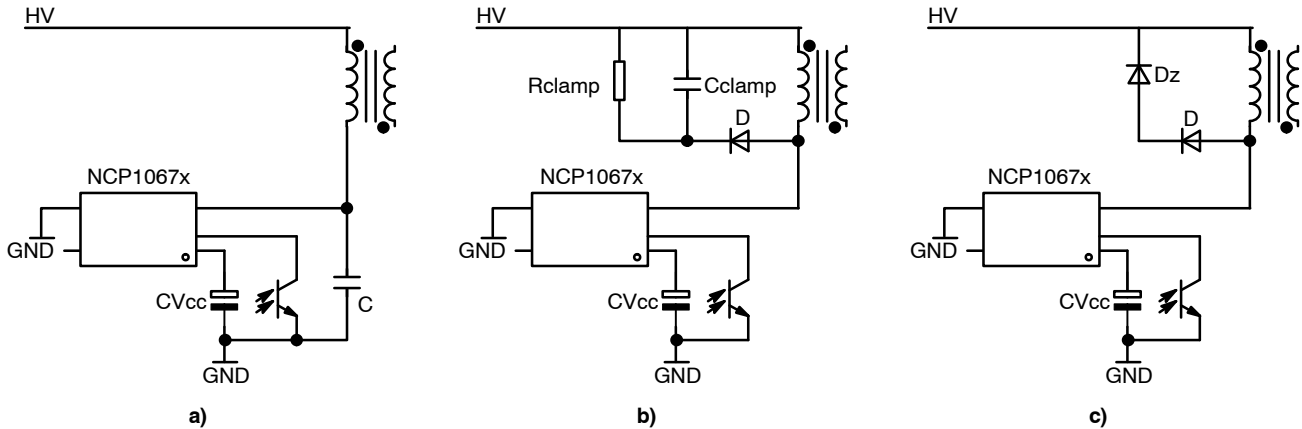
8. The theoretical total power is then  
 $117 + 15.5 + 2.1 = 127.6 \text{ mW}$   
 9. If the NCP106X operates at DSS mode, then the losses caused by DSS mode should be counted as losses of this device on the following calculation:

$$P_{\text{DSS}} = I_{\text{cc1}} \cdot V_{\text{in,max}} = 0.8 \text{ m} \cdot 375 = 300 \text{ mW} \quad (\text{eq. 17})$$

**MOSFET Protection**

As in any Flyback design, it is important to limit the drain excursion to a safe value, e.g. below the MOSFET BV<sub>DSS</sub>

which is 700 V. Figure 47 a–b–c present possible implementations:



**Figure 47. Different Options to Clamp the Leakage Spike**

Figure 47a: the simple capacitor limits the voltage according to the lateral MOSFET body–diode shall never be forward biased, either during start–up (because of a large leakage inductance) or in normal operation as shown by Figure 45. This condition sets the maximum voltage that can be reflected during  $t_{off}$ . As a result, the flyback voltage which is reflected on the drain at the switch opening cannot be larger than the input voltage. When selecting components, you must adopt a turn ratio which adheres to the following equation eq. 5. This option is only valid for low power applications, e.g. below 5 W, otherwise chances exist to destroy the MOSFET. After evaluating the leakage inductance, you can compute C with (eq. 6). Typical values are between 100 pF and up to 470 pF. Large capacitors increase capacitive losses...

Figure 47b: the most standard circuitry is called the RCD network. You can calculate  $R_{clamp}$  and  $C_{clamp}$  using the following formula:

$$R_{clamp} = \frac{2 V_{clamp} (V_{clamp} + (V_{out} + V_f) N)}{L_{leak} I_{leak}^2 F_{sw}} \quad (\text{eq. 18})$$

$$C_{clamp} = \frac{V_{clamp}}{V_{ripple} F_{sw} R_{clamp}} \quad (\text{eq. 19})$$

$V_{clamp}$  is usually selected 50 – 80 V above the reflected value  $N \times (V_{out} + V_f)$ . The diode needs to be a fast one and a MUR160 represents a good choice. One major drawback of the RCD network lies in its dependency upon the peak current. Worst case occurs when  $I_{peak}$  and  $V_{in}$  are maximum and  $V_{out}$  is close to reach the steady–state value.

Figure 47c: this option is probably the most expensive of all three but it offers the best protection degree. If you need a very precise clamping level, you must implement a zener diode or a TVS. There are little technology differences behind a standard zener diode and a TVS. However, the die

area is far bigger for a transient suppressor than that of zener. A 5 W zener diode like the 1N5388B will accept 180 W peak power if it lasts less than 8.3 ms. If the peak current in the worse case (e.g. when the PWM circuit maximum current limit works) multiplied by the nominal zener voltage exceeds these 180 W, then the diode will be destroyed when the supply experiences overloads. A transient suppressor like the P6KE200 still dissipates 5 W of continuous power but is able to accept surges up to 600 W @ 1 ms. Select the zener or TVS clamping level between 40 to 80 volts above the reflected output voltage when the supply is heavily loaded.

As a good design practice, it is recommended to implement one of this protection to make sure Drain pin voltage doesn't go above 650 V (to have some margin between Drain pin voltage and BV<sub>DSS</sub>) during most stringent operating conditions (high  $V_{in}$  and peak power).

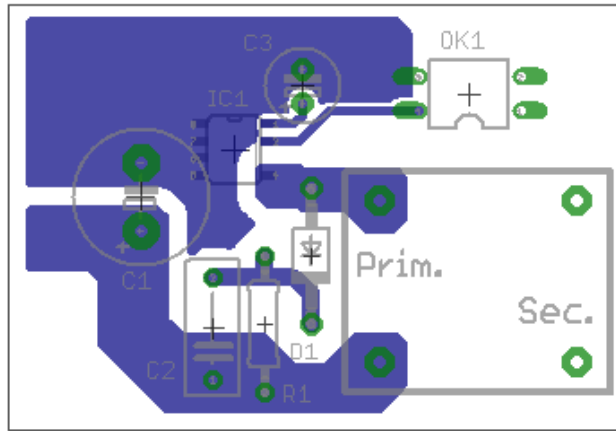
**Power Dissipation and Heatsinking**

The NCP1067X welcomes two dissipating terms, the DSS current–source (when active) and the MOSFET. Thus,  $P_{tot} = P_{DSS} + P_{MOSFET}$ . It is mandatory to properly manage the heat generated by losses. If no precaution is taken, risks exist to trigger the internal thermal shutdown (TSD). To help dissipating the heat, the PCB designer must foresee large copper areas around the package. When the package is surrounded by a surface approximately 200 mm<sup>2</sup> of 35 μm copper, the maximum power the device can thus evacuate is:

$$P_{max} = \frac{t_{jmax} - t_{ambmax}}{R_{\theta JA}} \quad (\text{eq. 20})$$

which gives around 862 mW for an ambient of 50°C and a maximum junction of 150°C. If the surface is not large enough, the  $R_{\theta JA}$  is growing and the maximum power the device can evacuate decreases. Figure 48 gives a possible layout to help drop the thermal resistance.

## NCP10670B, NCP10671B, NCP10672B



**Figure 48. A Possible PCB Arrangement to Reduce the Thermal Resistance Junction-to-Ambient**

**Bill of Material:**

- C1 Bulk capacitor, input DC voltage is connected to the capacitor
- C2, R1, D1 Clamping elements
- C3 Vcc capacitor
- OK1 Optocoupler

**ORDERING INFORMATION**

Device	Marking	Frequency	$R_{DS(on)}$	$I_{PK(0)}$	Package Type	Shipping <sup>†</sup>
NCP10670BD060R2G	P10670060	60 kHz	34	100 mA	SOIC-8 MISSING PIN 3 (Pb-Free)	2500 / Tape & Reel
NCP10670BD100R2G	P10670100	100 kHz	34	100 mA		2500 / Tape & Reel
NCP10671BD060R2G	P10671060	60 kHz	34	250 mA		2500 / Tape & Reel
NCP10671BD100R2G	P10671100	100 kHz	34	250 mA		2500 / Tape & Reel
NCP10672BD060R2G	P10672060	60 kHz	12	780 mA		2500 / Tape & Reel
NCP10672BD100R2G	P10672100	100 kHz	12	780 mA		2500 / Tape & Reel

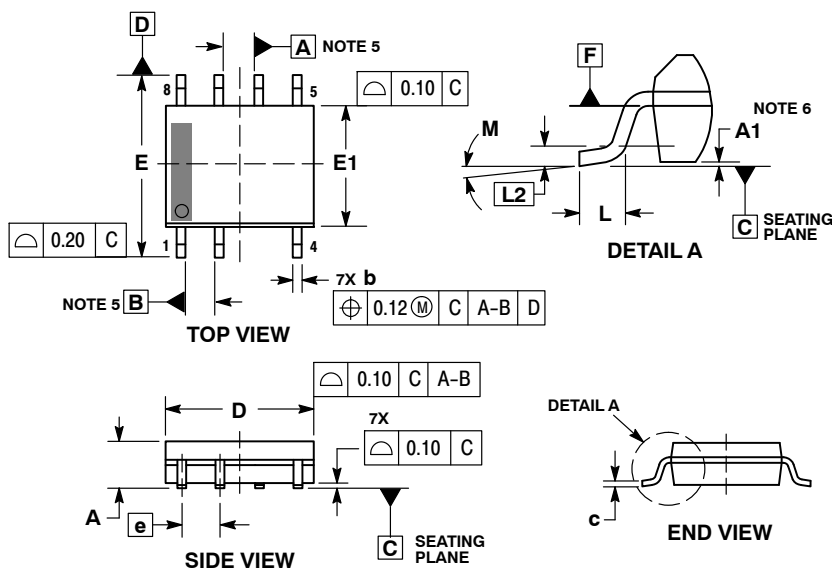
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 1:1

**SOIC8 MISSING PIN 3**  
**CASE 751EV**  
**ISSUE O**

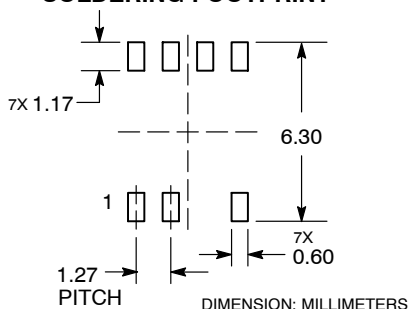
DATE 19 SEP 2017



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
  4. DIMENSIONS D & E1 DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM F.
  5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
  6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

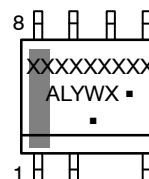
MILLIMETERS		
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
b	0.33	0.51
c	0.19	0.25
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
e	1.27 BSC	
L	0.40	1.27
L2	0.25 BSC	
M	0° 8°	

**RECOMMENDED SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC MARKING DIAGRAM\***



- XXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present. Some products may not follow the Generic Marking.

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<b>DESCRIPTION:</b>	<b>SOIC8 MISSING PIN 3</b>	<b>PAGE 1 OF 1</b>

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