

# 3-to-8 Line Decoder

## MM74HCT138

### General Description

The MM74HCT138 decoder utilizes advanced silicon-gate CMOS technology, and are well suited to memory address decoding or data routing applications. Both circuits feature high noise immunity and low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL logic.

The MM74HCT138 have 3 binary select inputs (A, B, and C). If the device is enabled these inputs determine which one of the eight normally HIGH outputs will go LOW. Two active LOW and one active HIGH enables (G1, G2A and G2B) are provided to ease the cascading decoders.

The decoders' output can drive 10 low power Schottky TTL equivalent loads and are functionally and pin equivalent to the 74LS138. All inputs are protected from damage due to static discharge by diodes to VCC and ground.

MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

### Features

- TTL Input Compatible
- Typical Propagation Delay: 20 ns
- Low Quiescent Current: 160  $\mu$ A Maximum (74HCT Series)
- Low Input Current: 1  $\mu$ A Maximum
- Fanout of 10 LS-TTL Loads
- These are Pb-Free Devices

### Connection Diagram

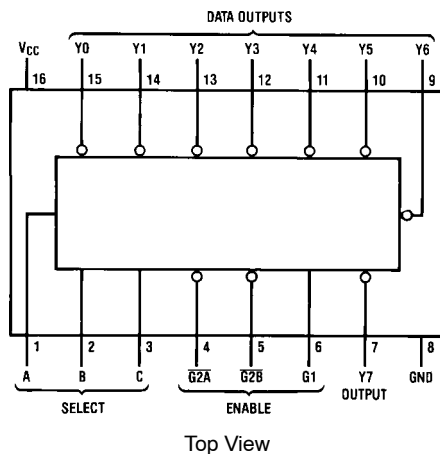
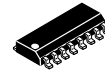
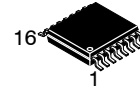


Figure 1. Pin Assignments for SOIC and TSSOP

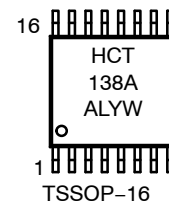
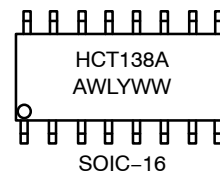


SOIC-16  
CASE 751B-05/751BG-01



TSSOP-16  
CASE 948F-01

### MARKING DIAGRAM



HCT138A = Specific Device Code  
A = Assembly Location  
WL, L = Wafer Lot  
Y = Year  
WW, W = Work Week

### ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

# MM74HCT138

## TRUTH TABLE

Inputs			Outputs											
Enable		Select												
G1	$\overline{G2}$ (Note 1)	C	B	A	Y0	Y01	Y2	Y3	Y4	Y5	Y6	Y7		
X	H	X	X	X	H	H	H	H	H	H	H	H		
L	X	X	X	X	H	H	H	H	H	H	H	H		
H	L	L	L	L	L	H	H	H	H	H	H	H		
H	L	L	L	H	H	L	H	H	H	H	H	H		
H	L	L	H	L	H	H	L	H	H	H	H	H		
H	L	L	H	H	H	H	H	L	H	H	H	H		
H	L	H	L	L	H	H	H	H	L	H	H	H		
H	L	H	L	H	H	H	H	H	H	L	H	H		
H	L	H	H	L	H	H	H	H	H	H	L	H		
H	L	H	H	H	H	H	H	H	H	H	H	L		

H = HIGH Level  
L = LOW Level  
X = Don't Care

1.  $\overline{G2} = \overline{G2A} + \overline{G2B}$

## Logic Diagram

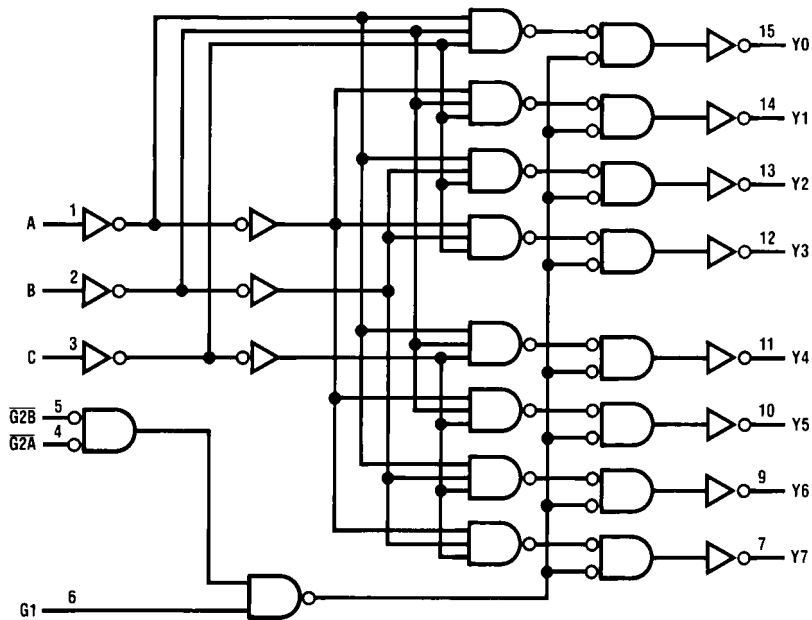


Figure 2. Logic Diagram

# MM74HCT138

## ABSOLUTE MAXIMUM RATINGS (Note 2)

Symbol	Parameter		Rating
V <sub>CC</sub>	Supply Voltage		-0.5 to +6.5 V
V <sub>IN</sub>	DC Input Voltage		-0.5 to V <sub>CC</sub> + 0.5 V
V <sub>OUT</sub>	DC Output Voltage		-0.5 to V <sub>CC</sub> + 0.5 V
I <sub>IK</sub> , I <sub>OK</sub>	Clamp Diode Current		±20 mA
I <sub>OUT</sub>	DC Output Current, per Pin		±25 mA
I <sub>CC</sub>	DC V <sub>CC</sub> or GND Current, per Pin		±50 mA
T <sub>STG</sub>	Storage Temperature Range		-65°C to +150°C
P <sub>D</sub>	Power Dissipation	S.O. Package Only	500 mW
T <sub>L</sub>	Lead Temperature (Soldering 10 Seconds)		260°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Unless otherwise specified all voltages are referenced to ground.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5.5	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input or Output Voltage	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature Range	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise or Fall Times	-	500	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 5 V ±10% (unless otherwise specified))

Symbol	Parameter	Conditions	T <sub>A</sub> = 25°C		T <sub>A</sub> = -40°C to 85°C	T <sub>A</sub> = -55°C to 125°C	Unit
			Typ	Guaranteed Limits			
V <sub>IH</sub>	Minimum HIGH Level Input Voltage		-	2.0	2.0	2.0	V
V <sub>IL</sub>	Maximum LOW Level Input Voltage		-	0.8	0.8	0.8	V
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   = 20 μA	V <sub>CC</sub>	V <sub>CC</sub> - 0.1	V <sub>CC</sub> - 0.1	V <sub>CC</sub> - 0.1	V
		I <sub>OUT</sub>   = 4.0 mA, V <sub>CC</sub> = 4.5 V	4.2	3.98	3.84	3.7	V
		I <sub>OUT</sub>   = 4.8 mA, V <sub>CC</sub> = 5.5 V	5.2	4.98	4.84	4.7	V
V <sub>OL</sub>	Maximum LOW Level Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   = 20 μA	0	0.1	0.1	0.1	V
		I <sub>OUT</sub>   = 4.0 mA, V <sub>CC</sub> = 4.5 V	0.2	0.26	0.33	0.4	V
		I <sub>OUT</sub>   = 4.8 mA, V <sub>CC</sub> = 5.5 V	0.2	0.26	0.33	0.4	V
I <sub>IN</sub>	Maximum Input Current	V <sub>IN</sub> = V <sub>CC</sub> or GND, V <sub>IH</sub> or V <sub>IL</sub>	-	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND, I <sub>OUT</sub> = 0 μA	-	8.0	80	160	μA
		V <sub>IN</sub> = 2.4 V or 0.5 V (Note 3)	-	0.3	0.4	0.5	mA

3. This is measured per input pin. All other inputs are held at V<sub>CC</sub> or ground.

# MM74HCT138

**AC ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V}$ ,  $t_r = t_f = 6\text{ ns}$ ,  $C_L = 15\text{ pF}$  (unless otherwise specified))

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Unit
$t_{PHL}$	Maximum Propagation Delay, A, B, or C to Output		20	35	ns
$t_{PLH}$	Maximum Propagation Delay, A, B, or C to Output		13	25	ns
$t_{PHL}$	Maximum Propagation Delay, G1 to Y Output		14	25	ns
$t_{PLH}$	Maximum Propagation Delay, G1 to Y Output		13	25	ns
$t_{PHL}$	Maximum Propagation Delay, $\overline{G2A}$ or $\overline{G2B}$ to Y Output		17	30	ns
$t_{PLH}$	Maximum Propagation Delay, $\overline{G2A}$ or $\overline{G2B}$ to Y Output		13	25	ns

**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $C_L = 50\text{ pF}$ ,  $t_r = t_f = 6\text{ ns}$  (unless otherwise specified))

Symbol	Parameter	Conditions	$T_A = 25^\circ\text{C}$		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	$T_A = -55^\circ\text{C to } 125^\circ\text{C}$	Unit
			Typ	Guaranteed Limits			
$t_{PHL}$	Maximum Propagation Delay A, B, or C to Output		24	40	50	60	ns
$t_{PLH}$	Maximum Propagation Delay A, B, or C to Output		18	30	38	45	ns
$t_{PHL}$	Maximum Propagation Delay G1 to Y Output		17	30	38	45	ns
$t_{PLH}$	Maximum Propagation Delay G1 to Y Output		20	30	38	45	ns
$t_{PHL}$	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Y Output		23	35	43	52	ns
$t_{PLH}$	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Y Output		18	30	38	45	ns
$t_{THL}, t_{TLH}$	Maximum Output Rise and Fall Time		–	15	19	22	ns
$C_{IN}$	Input Capacitance		–	5	10	10	pF
$C_{PD}$	Power Dissipation Capacitance	(Note 4)	55	–	–	–	pF

4.  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

## ORDERING INFORMATION

Part Number	Package	Shipping <sup>†</sup>
MM74HCT138M	SOIC-16, Case 751B-05 (Pb-Free)	48 Units / Tube
MM74HCT138MTC	TSSOP-16, Case 948F-01 (Pb-Free)	96 Units / Tube
MM74HCT138MX	SOIC-16, Case 751BG-01 (Pb-Free)	2500 Units / Tape & Reel
MM74HCT138MTCX	TSSOP-16, Case 948F-01 (Pb-Free)	2500 Units / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

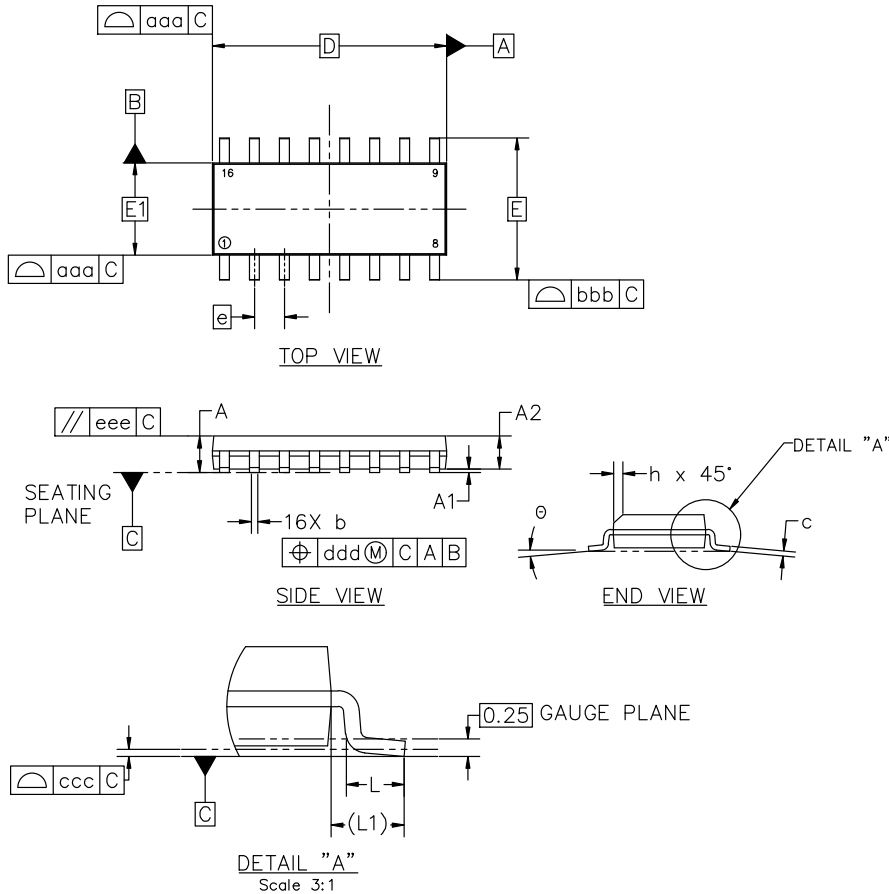


SOIC-16 9.90x3.90x1.37 1.27P  
CASE 751B  
ISSUE M

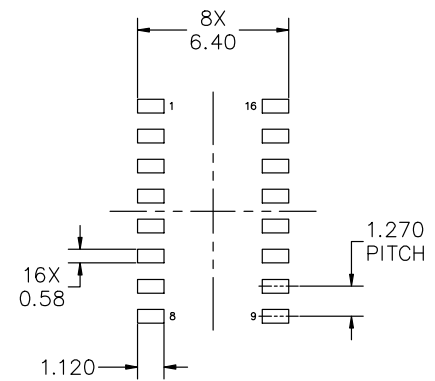
DATE 18 OCT 2024

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	---	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

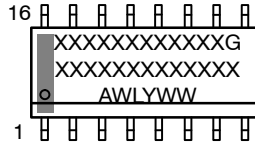
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**SOIC-16 9.90x3.90x1.37 1.27P**  
**CASE 751B**  
**ISSUE M**

DATE 18 OCT 2024

**GENERIC  
MARKING DIAGRAM\***



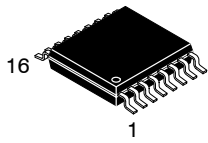
XXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

<p><b>STYLE 1:</b></p> <p>PIN 1. COLLECTOR  2. BASE  3. EMITTER  4. NO CONNECTION  5. EMITTER  6. BASE  7. COLLECTOR  8. COLLECTOR  9. BASE  10. EMITTER  11. NO CONNECTION  12. EMITTER  13. BASE  14. COLLECTOR  15. EMITTER  16. COLLECTOR</p>	<p><b>STYLE 2:</b></p> <p>PIN 1. CATHODE  2. ANODE  3. NO CONNECTION  4. CATHODE  5. CATHODE  6. NO CONNECTION  7. ANODE  8. CATHODE  9. CATHODE  10. ANODE  11. NO CONNECTION  12. CATHODE  13. CATHODE  14. NO CONNECTION  15. ANODE  16. CATHODE</p>	<p><b>STYLE 3:</b></p> <p>PIN 1. COLLECTOR, DYE #1  2. BASE, #1  3. EMITTER, #1  4. COLLECTOR, #1  5. COLLECTOR, #2  6. BASE, #2  7. EMITTER, #2  8. COLLECTOR, #2  9. COLLECTOR, #3  10. BASE, #3  11. EMITTER, #3  12. COLLECTOR, #3  13. COLLECTOR, #4  14. BASE, #4  15. EMITTER, #4  16. COLLECTOR, #4</p>	<p><b>STYLE 4:</b></p> <p>PIN 1. COLLECTOR, DYE #1  2. COLLECTOR, #1  3. COLLECTOR, #2  4. COLLECTOR, #2  5. COLLECTOR, #3  6. COLLECTOR, #3  7. COLLECTOR, #4  8. COLLECTOR, #4  9. BASE, #4  10. EMITTER, #4  11. BASE, #3  12. EMITTER, #3  13. BASE, #2  14. EMITTER, #2  15. BASE, #1  16. EMITTER, #1</p>
<p><b>STYLE 5:</b></p> <p>PIN 1. DRAIN, DYE #1  2. DRAIN, #1  3. DRAIN, #2  4. DRAIN, #2  5. DRAIN, #3  6. DRAIN, #3  7. DRAIN, #4  8. DRAIN, #4  9. GATE, #4  10. SOURCE, #4  11. GATE, #3  12. SOURCE, #3  13. GATE, #2  14. SOURCE, #2  15. GATE, #1  16. SOURCE, #1</p>	<p><b>STYLE 6:</b></p> <p>PIN 1. CATHODE  2. CATHODE  3. CATHODE  4. CATHODE  5. CATHODE  6. CATHODE  7. CATHODE  8. CATHODE  9. ANODE  10. ANODE  11. ANODE  12. ANODE  13. ANODE  14. ANODE  15. ANODE  16. ANODE</p>	<p><b>STYLE 7:</b></p> <p>PIN 1. SOURCE N-CH  2. COMMON DRAIN (OUTPUT)  3. COMMON DRAIN (OUTPUT)  4. GATE P-CH  5. COMMON DRAIN (OUTPUT)  6. COMMON DRAIN (OUTPUT)  7. COMMON DRAIN (OUTPUT)  8. SOURCE P-CH  9. SOURCE P-CH  10. COMMON DRAIN (OUTPUT)  11. COMMON DRAIN (OUTPUT)  12. COMMON DRAIN (OUTPUT)  13. GATE N-CH  14. COMMON DRAIN (OUTPUT)  15. COMMON DRAIN (OUTPUT)  16. SOURCE N-CH</p>	

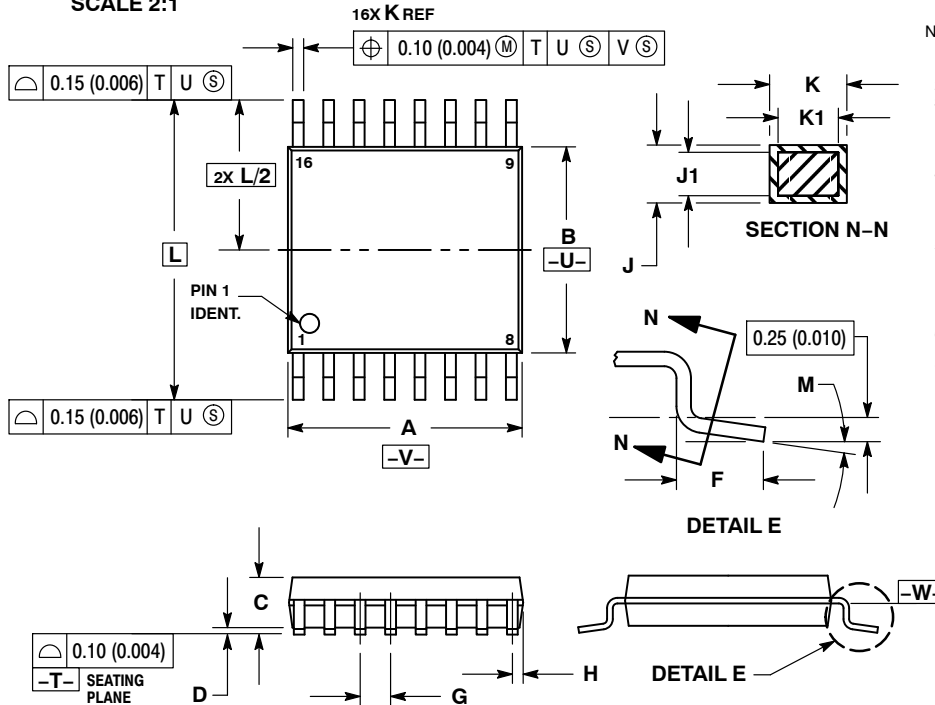
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TSSOP-16 WB  
CASE 948F  
ISSUE B

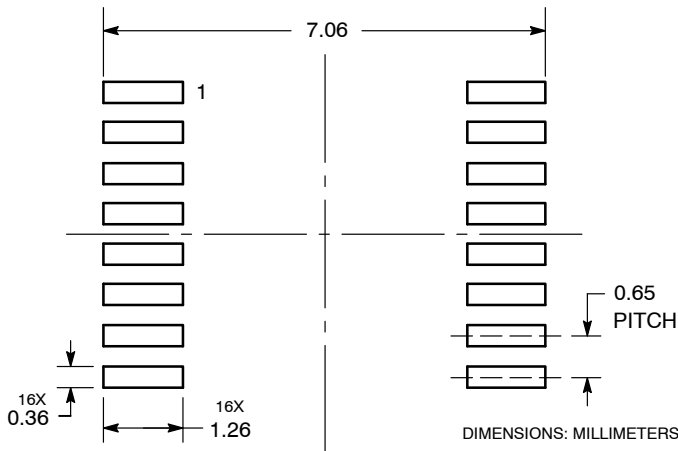
DATE 19 OCT 2006



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

RECOMMENDED  
SOLDERING FOOTPRINT\*



GENERIC  
MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- G or ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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