

# 3-State Octal D-Type Edge-Triggered Flip-Flop

## MM74HC574

The MM74HC574 high speed octal D-type flip-flops utilize advanced silicon-gate P-well CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the 3-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These devices are positive edge triggered flip-flops. Data at the D inputs, meeting the set-up and hold time requirements, are transferred to the Q outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The 74HC logic family is speed, function, and pinout compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V<sub>CC</sub> and ground.

### Features

- Typical Propagation Delay: 17 ns
- Wide Operating Voltage Range: 2 V – 6 V
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 160 μA Maximum
- Compatible with Bus-oriented Systems
- Output Drive Capability: 15 LS-TTL Loads
- This is a Pb-Free Device

### MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V <sub>CC</sub>	-0.5 to + 7.0 V	V
DC Input Voltage	V <sub>IN</sub>	-0.5 to V <sub>CC</sub> + 0.5 V	V
DC Output Voltage	V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> + 0.5 V	V
Clamp Diode Current	I <sub>IK</sub> , I <sub>OK</sub>	±20	mA
DC Output Current, per pin	I <sub>OUT</sub>	±35	mA
DC V <sub>CC</sub> or GND Current, per pin	I <sub>CC</sub>	±70	mA
Storage Temperature Range	T <sub>STG</sub>	-65 to +150	°C
Power Dissipation S.O. Package only	P <sub>D</sub>	500	mW
Lead Temperature (Soldering 10 s)	T <sub>L</sub>	260	°C

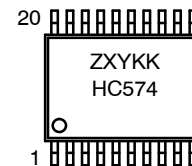
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Unless otherwise specified all voltages are referenced to ground.



TSSOP20  
MTC SUFFIX  
CASE 948AQ

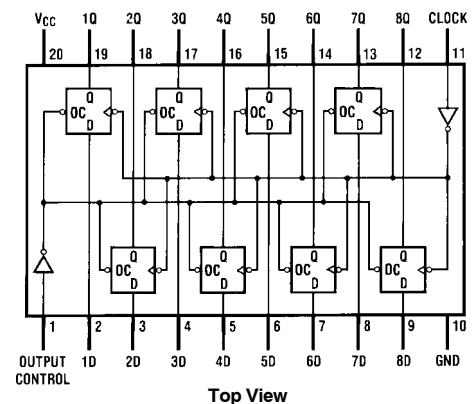
### MARKING DIAGRAM



HC574 = Specific Device Code  
Z = Assembly Plant Code  
XY = Data Code (Year & Week)  
KK = Lot Traceability Code

### CONNECTION DIAGRAM

#### Pin Assignments



### TRUTH TABLE

Output Control	Clock	Data	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

H = HIGH Level  
L = LOW Level  
X = Don't Care  
↑ = Transition from Low-to-HIGH  
Z = High Impedance State  
Q<sub>0</sub> = The level of the output before steady state input conditions were established

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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## RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristic	Min	Typ	Max	Units
$V_{CC}$	Supply Voltage	2		6	V
$V_{IN}, V_{OUT}$	DC Input or Output Voltage	0		$V_{CC}$	V
$T_A$	Operating Temperature Range	-55		+125	°C
$t_r, t_f$	Input Rise or Fall Times			1000 500 400	ns
				$V_{CC} = 2.0\text{ V}$ $V_{CC} = 4.5\text{ V}$ $V_{CC} = 6.0\text{ V}$	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS (Note 2)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ\text{C}$		$T_A = -40\text{ to }85^\circ\text{C}$		$T_A = -55\text{ to }125^\circ\text{C}$		Units
				Typ	Guaranteed Limits					
$V_{IH}$	Minimum HIGH Level Input Voltage		2.0 V		1.5	1.5	1.5		V	
			4.5 V		3.15	3.15	3.15			
			6.0 V		4.2	4.2	4.2			
$V_{IL}$	Maximum LOW Level Input Voltage		2.0 V		0.5	0.5	0.5		V	
			4.5 V		1.35	1.35	1.35			
			6.0 V		1.8	1.8	1.8			
$V_{OH}$	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20\ \mu\text{A}$	2.0 V	2.0	1.9	1.9	1.9	V		
			4.5 V	4.5	4.4	4.4	4.4			
		6.0 V	6.0	5.9	5.9	5.9				
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 6.0\text{ mA}$ $ I_{OUT}  \leq 7.8\text{ mA}$	4.5 V	4.2	3.98	3.84	3.7	V		
6.0 V	5.7		5.48	5.34	5.2					
$V_{OL}$	Maximum LOW Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20\ \mu\text{A}$	2.0 V	0	0.1	0.1	0.1	V		
			4.5 V	0	0.1	0.1	0.1			
		6.0 V	0	0.1	0.1	0.1				
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 6.0\text{ mA}$ $ I_{OUT}  \leq 7.8\text{ mA}$	4.5 V	0.2	0.26	0.33	0.4	V		
6.0 V	0.2		0.26	0.33	0.4					
$I_{IN}$	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0 V		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$		
$I_{OZ}$	Maximum 3-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND $OC = V_{IH}$	6.0 V		$\pm 0.5$	$\pm 5.0$	$\pm 10$	$\mu\text{A}$		
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\ \mu\text{A}$	6.0 V		8.0	80	160	$\mu\text{A}$		
$\Delta I_{CC}$	Quiescent Supply Current per Input Pin	$V_{CC} = 5.5\text{ V}$ $V_{IN} = 2.4\text{ V}$ or 0.4 V (Note 2)	OE	1.0	1.5	1.8	2.0	mA		
			CLK	0.6	0.8	1.0	1.1			
			DATA	0.4	0.5	0.6	0.7			

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. For a power supply of  $5\text{ V} \pm 10\%$  the worst-case output voltages ( $V_{OH}$ , and  $V_{OL}$ ) occur for HC at 4.5 V. Thus the 4.5 V values should be used when designing with this supply. Worst-case  $V_{IH}$  and  $V_{IL}$  occur at  $V_{CC} = 5.5\text{ V}$  and 4.5 V respectively. (The  $V_{IH}$  value at 5.5 V is 3.85 V.) The worst-case leakage current ( $I_{IN}$ ,  $I_{CC}$ , and  $I_{OZ}$ ) occur for CMOS at the higher voltage and so the 6.0 V values should be used.

## AC ELECTRICAL CHARACTERISTICS ( $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$ , $t_r = t_f = 6\text{ ns}$ )

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$f_{MAX}$	Maximum Operating Frequency		60	33	MHz
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, Clock to Q	$C_L = 45\text{ pF}$	17	27	ns
$t_{PZH}, t_{PZL}$	Maximum Output Enable Time	$R_L = 1\text{ k}\Omega$ , $C_L = 45\text{ pF}$	19	28	ns
$t_{PHZ}, t_{PLZ}$	Maximum Output Disable Time	$R_L = 1\text{ k}\Omega$ , $C_L = 5\text{ pF}$	14	25	ns

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## AC ELECTRICAL CHARACTERISTICS ( $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$ , $t_r = t_f = 6\text{ ns}$ )

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$t_S$	Minimum Setup Time, Data to Clock		10	12	ns
$t_H$	Minimum Hold Time, Clock to Data		-3	5	ns
$t_W$	Minimum Pulse Clock Width		8	15	ns

## AC ELECTRICAL CHARACTERISTICS ( $V_{CC} = 2.0 - 6.0\text{ V}$ , $C_L = 50\text{ pF}$ , $t_r = t_f = 6\text{ ns}$ unless otherwise specified)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ\text{C}$		$T_A = -40\text{ to }85^\circ\text{C}$	$T_A = -55\text{ to }125^\circ\text{C}$	Units
				Typ	Guaranteed Limits			
$f_{MAX}$	Maximum Operating Frequency	$C_L = 50\text{ pF}$	2.0 V 4.5 V 6.0 V		33 30 35	28 24 28	23 20 23	MHz
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay, Clock to Q	$C_L = 50\text{ pF}$ $C_L = 150\text{ pF}$	2.0 V	18	30	38	45	ns
			2.0 V	51	155	194	233	
			4.5 V 4.5 V	13 19	23 31	29 47	35 47	
6.0 V 6.0 V	12 18	20 27	25 34	30 41	ns			
$t_{PZH}$ , $t_{PLZ}$	Maximum Output Enable Time	$R_L = 1\text{ k}\Omega$ $C_L = 50\text{ pF}$ $C_L = 150\text{ pF}$	2.0 V	22	30	38	45	ns
			2.0 V	59	180	225	270	
			4.5 V 4.5 V	14 20	28 36	35 45	42 54	
6.0 V 6.0 V	12 18	24 31	30 39	36 47	ns			
$t_{PHZ}$ , $t_{PLZ}$	Maximum Output Disable Time	$R_L = 1\text{ k}\Omega$ $C_L = 50\text{ pF}$	2.0 V	15	30	38	45	ns
			4.5 V	12	25	31	38	
			6.0 V	10	21	27	32	
$t_S$	Minimum Setup Time Data to Clock		2.0 V	6	12	15	18	ns
			4.5 V		20	25	30	
			6.0 V		17	21	25	
$t_H$	Minimum Hold Time Clock to Data		2.0 V	-1	5	6	8	ns
			4.5 V		0	0	0	
			6.0 V		0	0	0	
$t_{THL}$ , $t_{TLH}$	Maximum Output Rise and Fall Time	$C_L = 50\text{ pF}$	2.0 V	6	12	15	18	ns
			4.5 V	7	12	15	18	
			6.0 V	6	10	13	15	
$t_W$	Minimum Clock Pulse Width		2.0 V	30	15	20	24	ns
			4.5 V	9	16	20	24	
			6.0 V	8	14	18	20	
$t_r$ , $t_f$	Maximum Clock Input Rise and Fall Time		2.0 V		1000	1000	1000	ns
			4.5 V		500	500	500	
			6.0 V		400	400	400	
$C_{PD}$		$OC = V_{CC}$ $OC = GND$		5 58				pF
$C_{IN}$	Maximum Input Capacitance			5	10	10	10	pF
$C_{OUT}$	Maximum Output Capacitance			15	20	20	20	pF

3.  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

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## ORDERING INFORMATION

Order Number	Package	Shipping†
MM74HC574MTCX	TSSOP-20	2500 Units / Tape & Reel
MM74HC574MTC	TSSOP-20	1825 Units / Tube

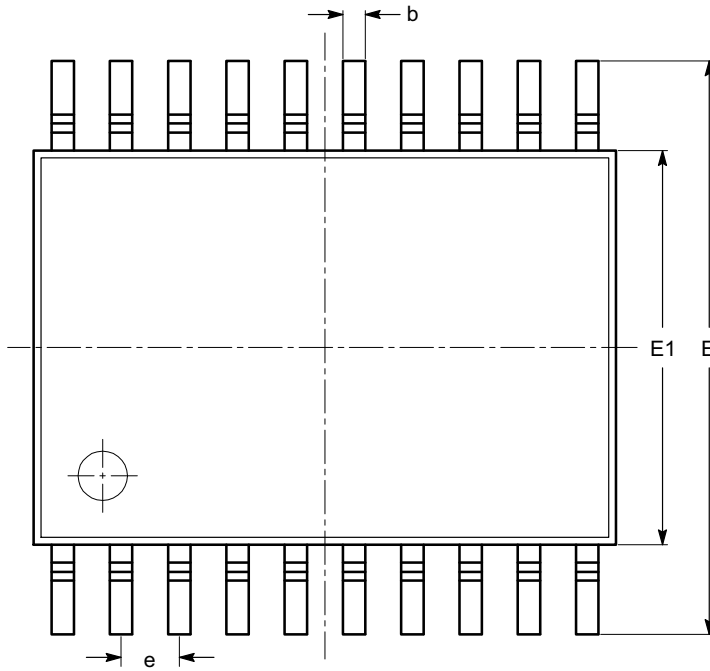
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

**MECHANICAL CASE OUTLINE**  
**PACKAGE DIMENSIONS**



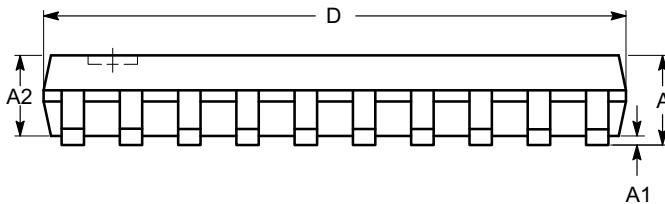
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**CASE 948AQ**  
**ISSUE A**

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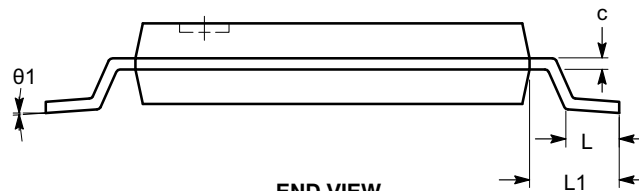


SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80		1.05
b	0.19		0.30
c	0.09		0.20
D	6.40	6.50	6.60
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
$\theta$	0°		8°

TOP VIEW



SIDE VIEW



END VIEW

**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-153.

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