MC14551B

Quad 2-Channel Analog Multiplexer/Demultiplexer

The MC14551B is a digitally−controlled analog switch. This device implements a 4PDT solid state switch with low ON impedance and very low OFF Leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

Features

- Triple Diode Protection on All Control Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Analog Voltage Range (V_{DD} − V_{EE}) = 3.0 to 18 V
  Note: V_{EE} must be ≤ V_{SS}
- Linearized Transfer Characteristics
- Low Noise − 12 nV$\sqrt{\text{Cycle}}$, f ≥ 1.0 kHz typical
- For Low R_{ON}, Use The HC4051, HC4052, or HC4053 High−Speed CMOS Devices
- Switch Function is Break Before Make
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This Device is Pb−Free and is RoHS Compliant

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage Range (Referenced to V_{EE}, $V_{SS} \geq V_{EE}$)	V_{DD}	– 0.5 to + 18.0	V
Input or Output Voltage (DC or Transient) (Referenced to V_{SS} for Control Input and V_{EE} for Switch I/O)	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Input Current (DC or Transient), per Control Pin	I_{in}	±10	mA
Switch Through Current	I_{sw}	±25	mA
Power Dissipation, per Package (Note 1)	P_D	500	mW
Ambient Temperature Range	T_A	– 55 to + 125	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C
Lead Temperature (8–Second Soldering)	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: “D/DW” Package: −7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$ for control inputs and $V_{EE} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$ for Switch I/O.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS}, V_{EE} or V_{DD}). Unused outputs must be left open.

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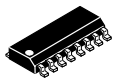
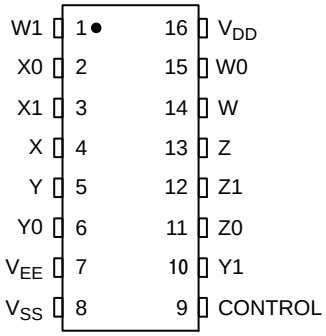
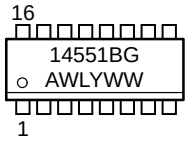


SOIC−16
D SUFFIX
CASE 751B

PIN ASSIGNMENT



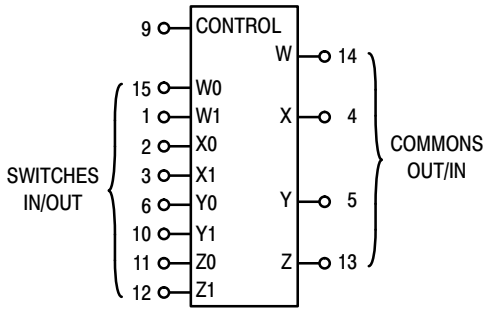
MARKING DIAGRAM



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

Control	ON
0	W0 X0 Y0 Z0
1	W1 X1 Y1 Z1

NOTE: Control Input referenced to V_{SS}, Analog Inputs and Outputs reference to V_{EE}. V_{EE} must be $\leq V_{SS}$.

ORDERING INFORMATION

Device	Package	Shipping†
MC14551BDG	SOIC−16 (Pb−Free)	48 Units / Rail
MC14551BDR2G	SOIC−16 (Pb−Free)	2500 / Tape & Reel
NLV14551BDR2G*	SOIC−16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

ELECTRICAL CHARACTERISTICS

Characteristic	V_{DD}	Test Conditions	Symbol	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	125°C Min	125°C Max	Unit
SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})											
Power Supply Voltage Range	–	$V_{DD} - 3.0 \geq V_{SS} \geq V_{EE}$	V_{DD}	3.0	18	3.0	–	18	3.0	18	V
Quiescent Current Per Package	5.0 10 15	Control Inputs: V_{in} = V_{SS} or V_{DD}, Switch I/O: $V_{EE} \leq V_{I/O} \leq V_{DD}$, and $\Delta V_{switch} \leq$ 500 mV (Note 3)	I_{DD}	– – –	5.0 10 20	– – –	0.005 0.010 0.015	5.0 10 20	– – –	150 300 600	μA
Total Supply Current (Dynamic Plus Quiescent, Per Package)	5.0 10 15	T_A = 25°C only (The channel component, $(V_{in} - V_{out})/R_{on}$, is not included.)	$I_{D(AV)}$	Typical			(0.07 μA/kHz) f + I_{DD} (0.20 μA/kHz) f + I_{DD} (0.36 μA/kHz) f + I_{DD}				μA
CONTROL INPUT (Voltages Referenced to V_{SS})											
Low−Level Input Voltage	5.0 10 15	R_{on} = per spec, I_{off} = per spec	V_{IL}	– – –	1.5 3.0 4.0	– – –	2.25 4.50 6.75	1.5 3.0 4.0	– – –	1.5 3.0 4.0	V
High−Level Input Voltage	5.0 10 15	R_{on} = per spec, I_{off} = per spec	V_{IH}	3.5 7.0 11	– – –	3.5 7.0 11	2.75 5.50 8.25	– – –	3.5 7.0 11	– – –	V
Input Leakage Current	15	V_{in} = 0 or V_{DD}	I_{in}	–	±0.1	–	±0.00001	±0.1	–	±1.0	μA
Input Capacitance	–		C_{in}	–	–	–	5.0	7.5	–	–	pF
SWITCHES IN/OUT AND COMMONS OUT/IN — W, X, Y, Z (Voltages Referenced to V_{EE})											
Recommended Peak−to−Peak Voltage Into or Out of the Switch	–	Channel On or Off	$V_{I/O}$	0	V_{DD}	0	–	V_{DD}	0	V_{DD}	V_{p-p}
Recommended Static or Dynamic Voltage Across the Switch (Note 3) (Figure 3)	–	Channel On	ΔV_{switch}	0	600	0	–	600	0	300	mV
Output Offset Voltage	–	V_{in} = 0 V, No Load	V_{OO}	–	–	–	10	–	–	–	μV
ON Resistance	5.0 10 15	$\Delta V_{switch} \leq$ 500 mV (Note 3), $V_{in} = V_{IL}$ or V_{IH} (Control), and V_{in} = 0 to V_{DD} (Switch)	R_{on}	– –	800 400 220	– – –	250 120 80	1050 500 280	– – –	1200 520 300	Ω
ΔON Resistance Between Any Two Channels in the Same Package	5.0 10 15		ΔR_{on}	– – –	70 50 45	– – –	25 10 10	70 50 45	– – –	135 95 65	Ω
Off−Channel Leakage Current (Figure 8)	15	$V_{in} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel	I_{off}	–	±100	–	±0.05	±100	–	±1000	nA
Capacitance, Switch I/O	–	Switch Off	$C_{I/O}$	–	–	–	10	–	–	–	pF
Capacitance, Common O/I	–		$C_{O/I}$	–	–	–	17	–	–	–	pF
Capacitance, Feedthrough (Channel Off)	– –	Pins Not Adjacent Pins Adjacent	$C_{I/O}$	– –	– –	– –	0.15 0.47	– –	– –	– –	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labeled “Typ” is not to be used for design purposes, but is intended as an indication of the IC’s potential performance.
3. For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

ELECTRICAL CHARACTERISTICS (C_L = 50 pF, T_A = 25°C, $V_{EE} \leq V_{SS}$)

Characteristic	Symbol	$V_{DD} - V_{EE}$ Vdc	Min	Typ (Note 4)	Max	Unit
Propagation Delay Times Switch Input to Switch Output (R_L = 10 kΩ) t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 26.5 ns t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 11 ns t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 9.0 ns	t_{PLH}, t_{PHL}	 5.0 10 15	–	 35 15 12	 90 40 30	ns
Control Input to Output (R_L = 10 kΩ) V_{EE} = V_{SS} (Figure 4)	t_{PLH}, t_{PHL}	 5.0 10 15	–	 350 140 100	 875 350 250	ns
Second Harmonic Distortion R_L = 10 kΩ, f = 1 kHz, V_{in} = 5 V_{p-p}	–	10	–	0.07	–	%
Bandwidth (Figure 5) R_L = 1 kΩ, V_{in} = 1/2 $(V_{DD} - V_{EE})_{p-p}$, 20 Log (V_{out}/V_{in}) = − 3 dB, C_L = 50 pF	BW	10	–	17	–	MHz
Off Channel Feedthrough Attenuation, Figure 5 R_L = 1 kΩ, V_{in} = 1/2 $(V_{DD} - V_{EE})_{p-p}$, f_{in} = 55 MHz	–	10	–	– 50	–	dB
Channel Separation (Figure 6) R_L = 1 kΩ, V_{in} = 1/2 $(V_{DD} - V_{EE})_{p-p}$, f_{in} = 3 MHz	–	10	–	– 50	–	dB
Crosstalk, Control Input to Common O/I, Figure 7 R1 = 1 kΩ, R_L = 10 kΩ, Control t_r = t_f = 20 ns	–	10	–	75	–	mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

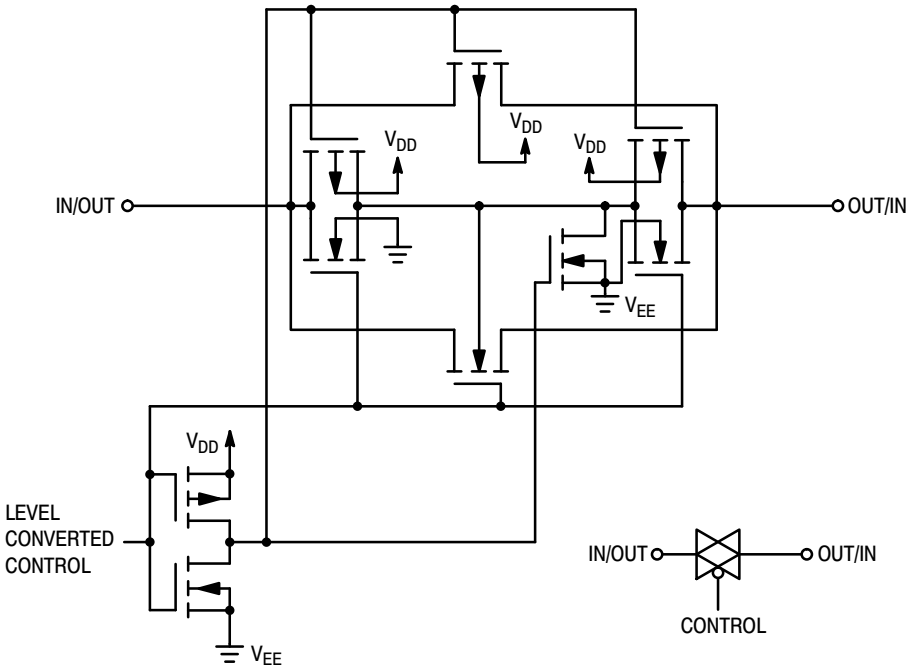


Figure 1. Switch Circuit Schematic

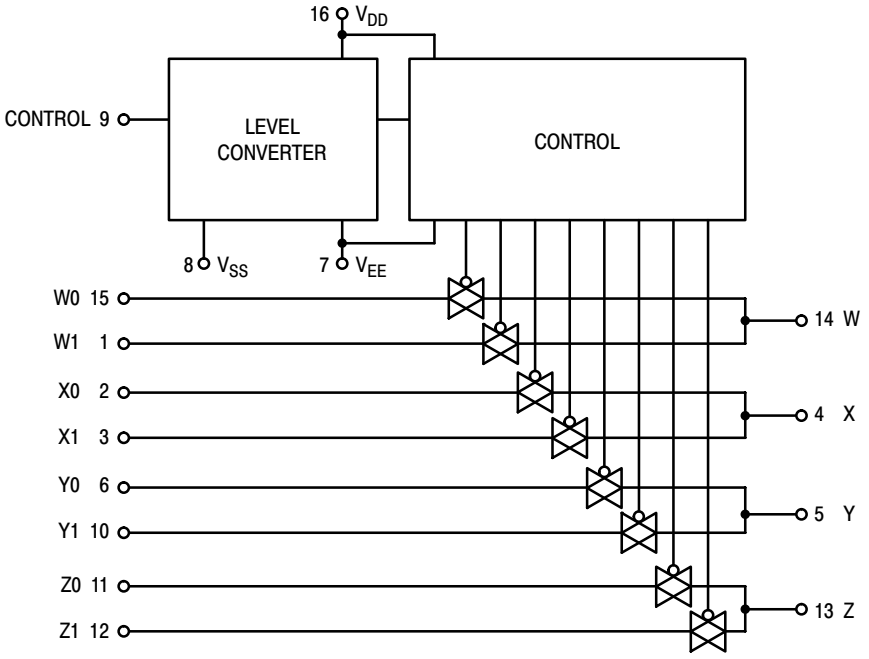


Figure 2. MC14551B Functional Diagram

TEST CIRCUITS

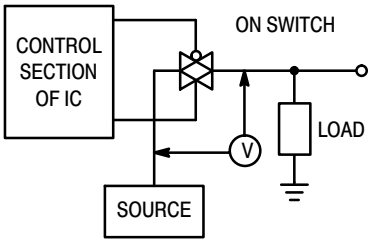


Figure 3. ΔV Across Switch

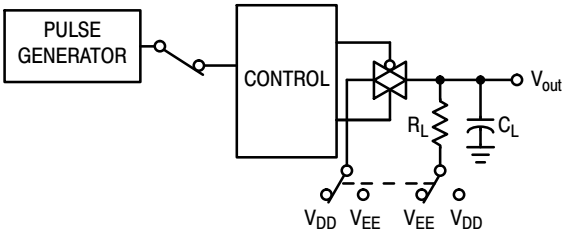


Figure 4. Propagation Delay Times, Control to Output

Control input used to turn ON or OFF the switch under test.

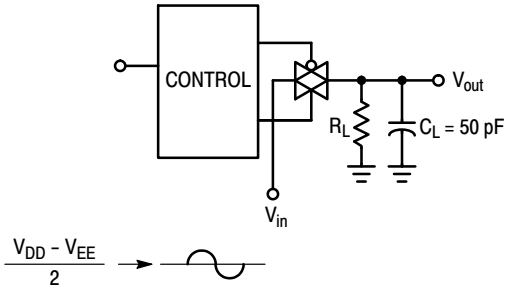


Figure 5. Bandwidth and Off−Channel Feedthrough Attenuation

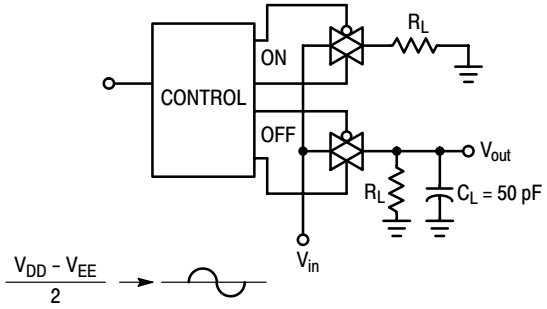


Figure 6. Channel Separation (Adjacent Channels Used for Setup)

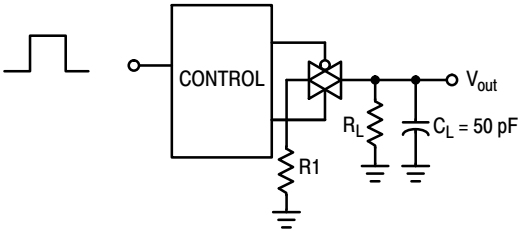


Figure 7. Crosstalk, Control Input to Common O/I

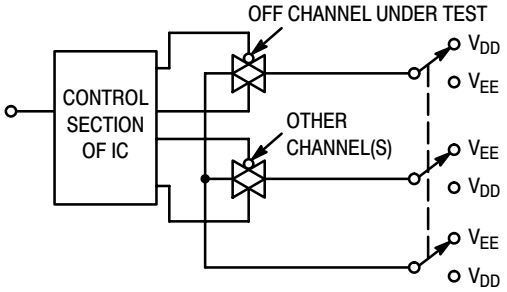


Figure 8. Off Channel Leakage

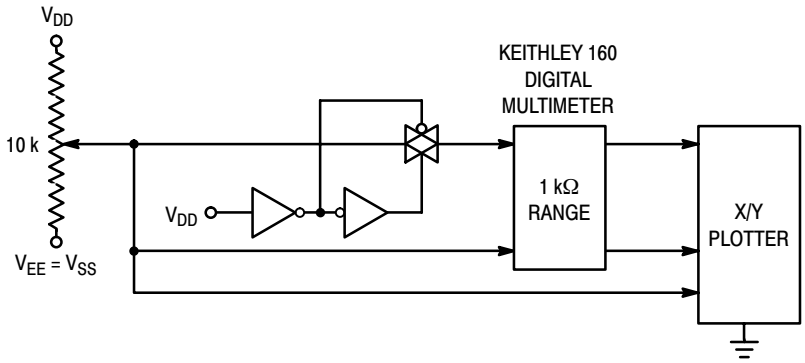


Figure 9. Channel Resistance (R_{ON}) Test Circuit

TYPICAL RESISTANCE CHARACTERISTICS

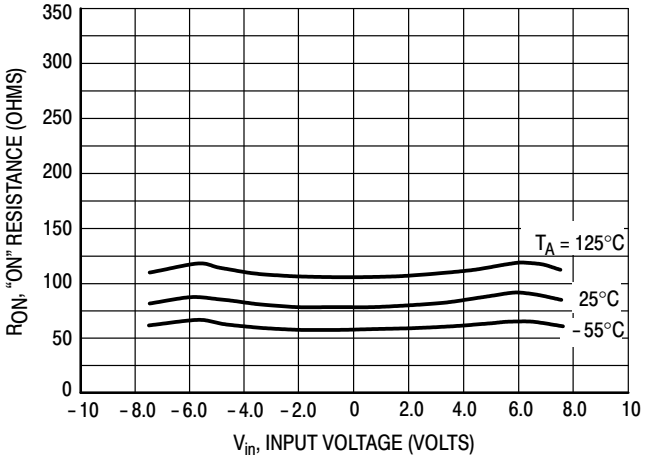


Figure 10. V_{DD} @ 7.5 V, V_{EE} @ – 7.5 V

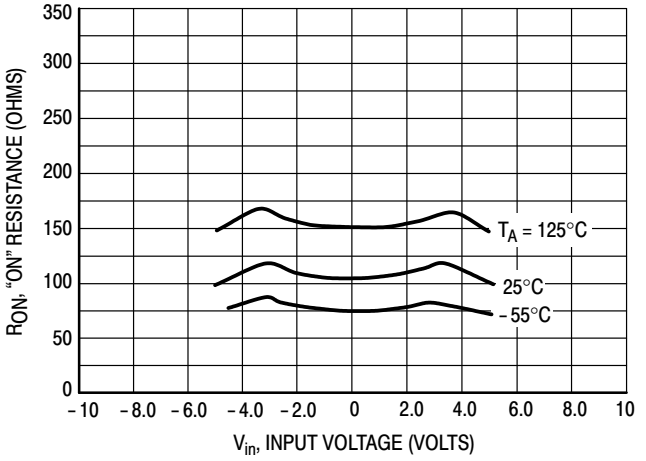


Figure 11. V_{DD} @ 5.0 V, V_{EE} @ – 5.0 V

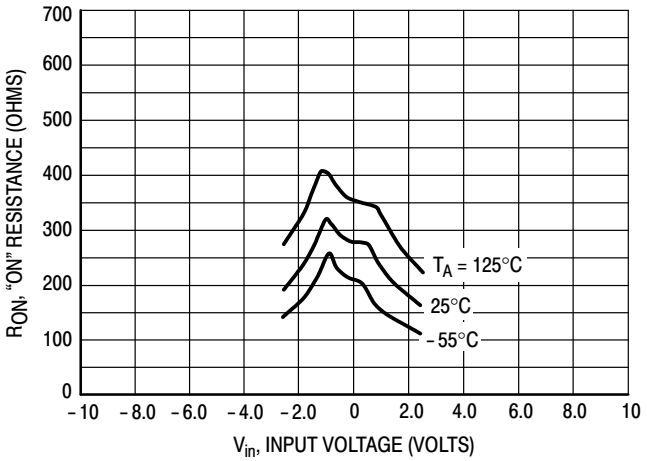


Figure 12. V_{DD} @ 2.5 V, V_{EE} @ – 2.5 V

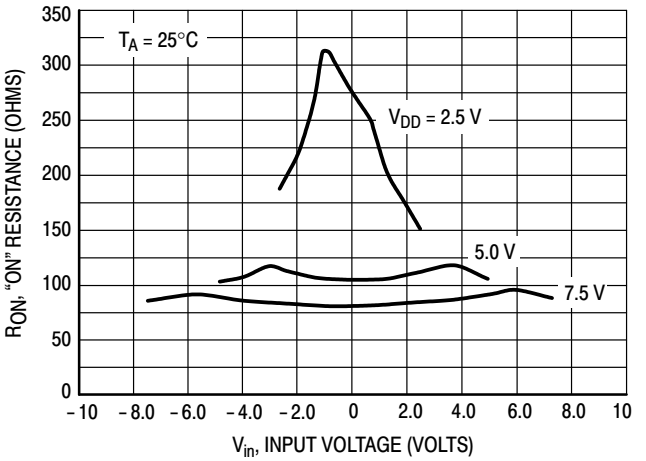


Figure 13. Comparison at 25°C, V_{DD} @ – V_{EE}

APPLICATIONS INFORMATION

Figure A illustrates use of the on−chip level converter detailed in Figure 2. The 0−to−5.0 V Digital Control signal is used to directly control a 9 V_{p-p} analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, V_{DD} = + 5.0 V = logic high at the control inputs; V_{SS} = GND = 0 V = logic low.

The maximum analog signal level is determined by V_{DD} and V_{EE}. The V_{DD} voltage determines the maximum recommended peak above V_{SS}. The V_{EE} voltage determines the maximum swing below V_{SS}. For the example, $V_{DD} - V_{SS}$ = 5.0 V maximum swing above V_{SS}; $V_{SS} - V_{EE}$ = 5.0 V maximum swing below V_{SS}. The example shows a ± 4.5 V signal which allows a 1/2 V margin at each peak. If voltage transients above V_{DD} and/or below V_{EE} are anticipated on the analog channels, external diodes (D_x) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The absolute maximum potential difference between V_{DD} and V_{EE} is 18 V. Most parameters are specified up to 15 V which is the recommended maximum difference between V_{DD} and V_{EE}.

Balanced supplies are not required. However, V_{SS} must be greater than or equal to V_{EE}. For example, V_{DD} = + 10 V, V_{SS} = + 5.0 V, and V_{EE} = – 3.0 V is acceptable. See the table below.

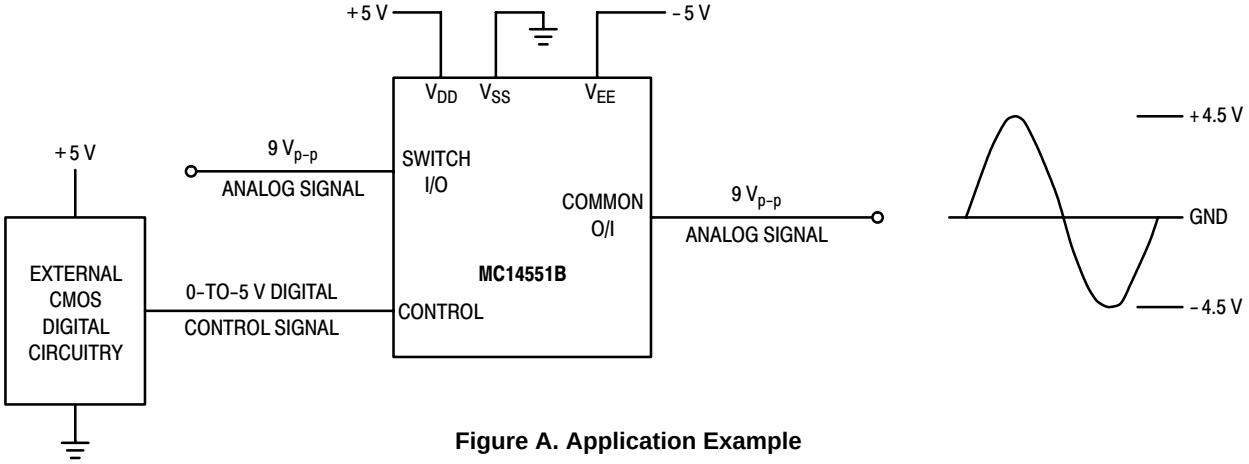


Figure A. Application Example

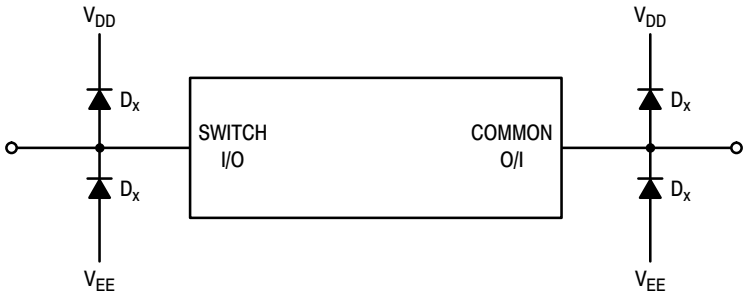
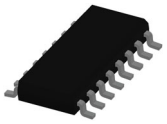


Figure B. External Schottky or Germanium Clipping Diodes

POSSIBLE SUPPLY CONNECTIONS

V_{DD} In Volts	V_{SS} In Volts	V_{EE} In Volts	Control Inputs Logic High/Logic Low In Volts	Maximum Analog Signal Range In Volts
+ 8	0	– 8	+ 8/0	+ 8 to – 8 = 16 V_{p-p}
+ 5	0	– 12	+ 5/0	+ 5 to – 12 = 17 V_{p-p}
+ 5	0	0	+ 5/0	+ 5 to 0 = 5 V_{p-p}
+ 5	0	– 5	+ 5/0	+ 5 to – 5 = 10 V_{p-p}
+ 10		– 5	+ 10/ + 5	+ 10 to – 5 = 15 V_{p-p}

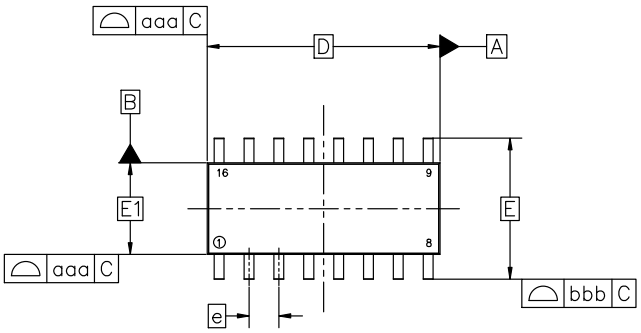
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



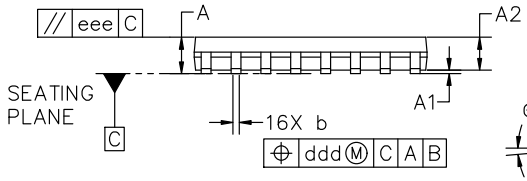
SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

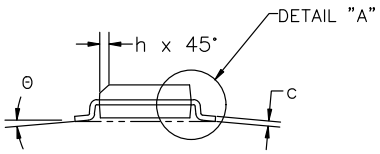
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



TOP VIEW

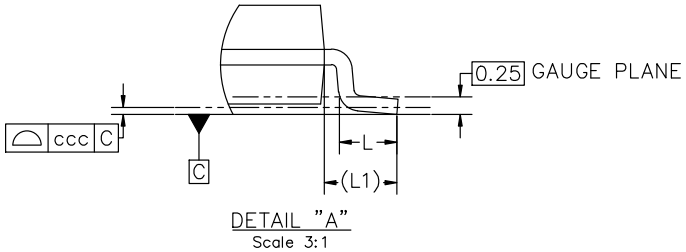


SIDE VIEW

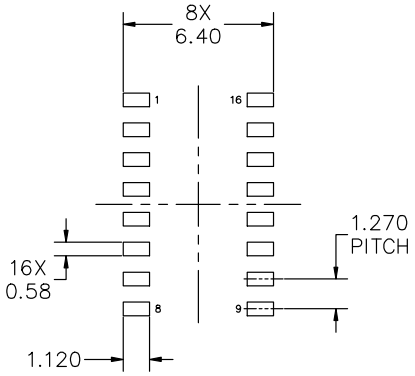


END VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.00	0.05	0.10
A2	1.35	1.50	1.65
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



DETAIL "A"
Scale 3:1



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

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SOIC−16 9.90x3.90x1.50 1.27P
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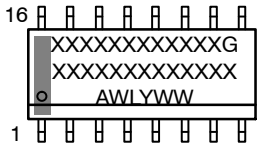
ISSUE L

DATE 29 MAY 2024

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:		STYLE 2:		STYLE 3:		STYLE 4:	
PIN 1.	COLLECTOR	PIN 1.	CATHODE	PIN 1.	COLLECTOR, DYE #1	PIN 1.	COLLECTOR, DYE #1
2.	BASE	2.	ANODE	2.	BASE, #1	2.	COLLECTOR, #1
3.	EMITTER	3.	NO CONNECTION	3.	EMITTER, #1	3.	COLLECTOR, #2
4.	NO CONNECTION	4.	CATHODE	4.	COLLECTOR, #1	4.	COLLECTOR, #2
5.	EMITTER	5.	CATHODE	5.	COLLECTOR, #2	5.	COLLECTOR, #3
6.	BASE	6.	NO CONNECTION	6.	BASE, #2	6.	COLLECTOR, #3
7.	COLLECTOR	7.	ANODE	7.	EMITTER, #2	7.	COLLECTOR, #4
8.	COLLECTOR	8.	CATHODE	8.	COLLECTOR, #2	8.	COLLECTOR, #4
9.	BASE	9.	CATHODE	9.	COLLECTOR, #3	9.	BASE, #4
10.	EMITTER	10.	ANODE	10.	BASE, #3	10.	EMITTER, #4
11.	NO CONNECTION	11.	NO CONNECTION	11.	EMITTER, #3	11.	BASE, #3
12.	EMITTER	12.	CATHODE	12.	COLLECTOR, #3	12.	EMITTER, #3
13.	BASE	13.	CATHODE	13.	COLLECTOR, #4	13.	BASE, #2
14.	COLLECTOR	14.	NO CONNECTION	14.	BASE, #4	14.	EMITTER, #2
15.	EMITTER	15.	ANODE	15.	EMITTER, #4	15.	BASE, #1
16.	COLLECTOR	16.	CATHODE	16.	COLLECTOR, #4	16.	EMITTER, #1

STYLE 5:		STYLE 6:		STYLE 7:	
PIN 1.	DRAIN, DYE #1	PIN 1.	CATHODE	PIN 1.	SOURCE N-CH
2.	DRAIN, #1	2.	CATHODE	2.	COMMON DRAIN (OUTPUT)
3.	DRAIN, #2	3.	CATHODE	3.	COMMON DRAIN (OUTPUT)
4.	DRAIN, #2	4.	CATHODE	4.	GATE P-CH
5.	DRAIN, #3	5.	CATHODE	5.	COMMON DRAIN (OUTPUT)
6.	DRAIN, #3	6.	CATHODE	6.	COMMON DRAIN (OUTPUT)
7.	DRAIN, #4	7.	CATHODE	7.	COMMON DRAIN (OUTPUT)
8.	DRAIN, #4	8.	CATHODE	8.	SOURCE P-CH
9.	GATE, #4	9.	ANODE	9.	SOURCE P-CH
10.	SOURCE, #4	10.	ANODE	10.	COMMON DRAIN (OUTPUT)
11.	GATE, #3	11.	ANODE	11.	COMMON DRAIN (OUTPUT)
12.	SOURCE, #3	12.	ANODE	12.	COMMON DRAIN (OUTPUT)
13.	GATE, #2	13.	ANODE	13.	GATE N-CH
14.	SOURCE, #2	14.	ANODE	14.	COMMON DRAIN (OUTPUT)
15.	GATE, #1	15.	ANODE	15.	COMMON DRAIN (OUTPUT)
16.	SOURCE, #1	16.	ANODE	16.	SOURCE N-CH

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