

# 3.3 V/5 V ECL Dual Differential 2:1 Multiplexer

## MC10EP56, MC100EP56

### Description

The MC10/100EP56 is a dual, fully differential 2:1 multiplexer. The differential data path makes the device ideal for multiplexing low skew clock or other skew sensitive signals. Multiple  $V_{BB}$  pins are provided.

The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu$ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

The device features both individual and common select inputs to address both data path and random logic applications.

The 100 Series contains temperature compensation.

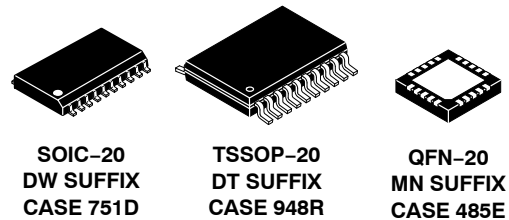
### Features

- 360 ps Typical Propagation Delays
- Maximum Frequency > 3 GHz Typical
- PECL Mode Operating Range:  $V_{CC} = 3.0$  V to 5.5 V with  $V_{EE} = 0$  V
- NECL Mode Operating Range:  $V_{CC} = 0$  V with  $V_{EE} = -3.0$  V to  $-5.5$  V
- Open Input Default State
- Safety Clamp on Inputs
- Separate and Common Select
- Q Output Will Default LOW with Inputs Open or at  $V_{EE}$
- $V_{BB}$  Outputs
- These Devices are Pb-Free and are RoHS Compliant



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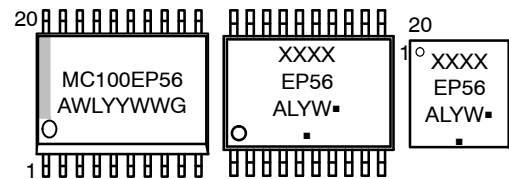


SOIC-20  
DW SUFFIX  
CASE 751D

TSSOP-20  
DT SUFFIX  
CASE 948R

QFN-20  
MN SUFFIX  
CASE 485E

### MARKING DIAGRAMS\*



XXXX = MC10 or 100  
A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G, ■ = Pb-Free Package

(Note: Microdot may be in either location)

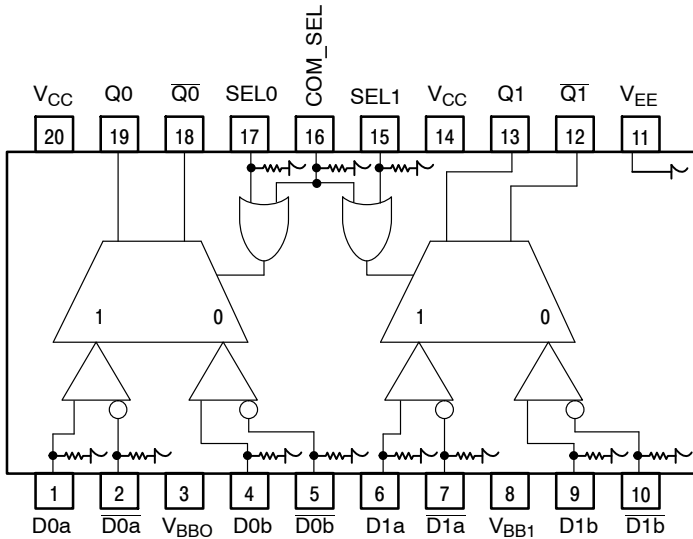
\*For additional marking information, refer to Application Note [AND8002/D](#).

### ORDERING INFORMATION

Device	Package	Shipping†
MC10EP56DTG	TSSOP-20 (Pb-Free)	75 Units / Tube
MC10EP56DTR2G	TSSOP-20 (Pb-Free)	2500 / Tape & Reel
MC10EP56MNG	QFN-20 (Pb-Free)	92 Units / Tube
MC100EP56DWG	SOIC-20 (Pb-Free)	38 Units / Tube
MC100EP56DTG	TSSOP-20 (Pb-Free)	75 Units / Tube
MC100EP56DTR2G	TSSOP-20 (Pb-Free)	2500 / Tape & Reel
MC100EP56MNG	QFN-20 (Pb-Free)	92 Units / Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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Warning: All  $V_{CC}$  and  $V_{EE}$  pins must be externally connected to Power Supply to guarantee proper operation.

**Figure 1. 20-Lead Package (Top View) and Logic Diagram**

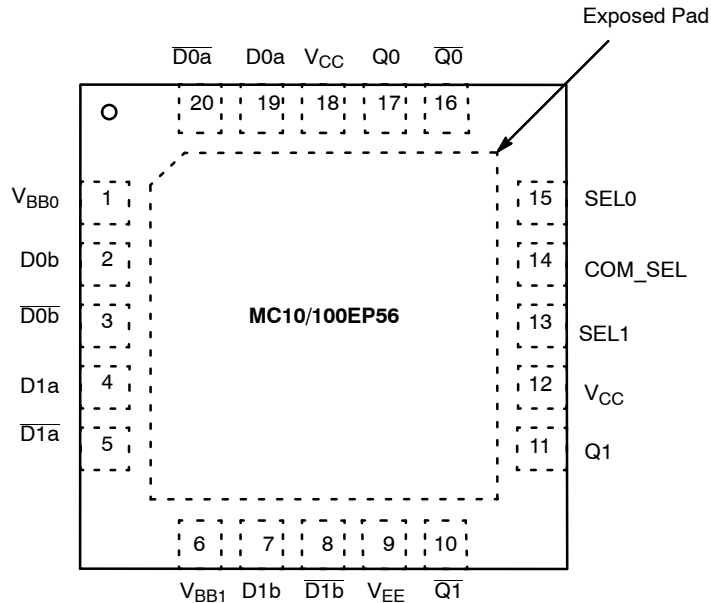
**Table 1. PIN DESCRIPTION**

PIN	FUNCTION
$D0a^* - D1a^*$	ECL Input Data a
$\overline{D0a^*} - \overline{D1a^*}$	ECL Input Data a Invert
$D0b^* - D1b^*$	ECL Input Data b
$\overline{D0b^*} - \overline{D1b^*}$	ECL Input Data b Invert
$SEL0^* - SEL1^*$	ECL Indiv. Select Input
$COM\_SEL^*$	ECL Common Select Input
$V_{BB0}, V_{BB1}$	Output Reference Voltage
$Q0 - Q1$	ECL True Outputs
$\overline{Q0} - \overline{Q1}$	ECL Inverted Outputs
$V_{CC}$	Positive Supply
$V_{EE}$	Negative Supply
EP	Exposed Pad

\* Pins will default LOW when left open.

**Table 2. TRUTH TABLE**

SEL0	SEL1	COM_SEL	$Q0, \overline{Q0}$	$Q1, \overline{Q1}$
X	X	H	a	a
L	L	L	b	b
L	H	L	b	a
H	H	L	a	a
H	L	L	a	b



NOTE: The Exposed Pad (EP) on package bottom must be attached to a heat-sinking conduit. The Exposed Pad may only be electrically connected to  $V_{EE}$ .

**Figure 1. QFN-20 Pinout (Top View)**

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**Table 3. ATTRIBUTES**

Characteristics	Value
Internal Input Pulldown Resistor	75 kΩ
Internal Input Pullup Resistor	N/A
ESD Protection Human Body Model Machine Model Charged Device Model	> 2 kV > 150 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb-Free Pkg
SOIC TSSOP QFN	Level 3 Level 3 Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	140 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note [AND8003/D](#).

**Table 4. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	PECL Mode Power Supply	V <sub>EE</sub> = 0 V		6	V
V <sub>EE</sub>	NECL Mode Power Supply	V <sub>CC</sub> = 0 V		-6	V
V <sub>I</sub>	PECL Mode Input Voltage	V <sub>EE</sub> = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub>	6	V
	NECL Mode Input Voltage	V <sub>CC</sub> = 0 V	V <sub>I</sub> ≥ V <sub>EE</sub>	-6	V
I <sub>out</sub>	Output Current	Continuous Surge		50	mA
				100	mA
I <sub>BB</sub>	V <sub>BB</sub> Sink/Source			± 0.5	mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 lfpm	20 TSSOP	140	°C/W
		500 lfpm	20 TSSOP	100	°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	Standard Board	20 TSSOP	23 to 41	°C/W
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	20 SOIC	90	°C/W
			20 SOIC	60	°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	Standard Board	20 SOIC	33 to 35	°C/W
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	QFN-20	47	°C/W
			QFN-20	33	°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	Standard Board	QFN-20	18	°C/W
T <sub>sol</sub>	Wave Solder	Pb-Free	<2 to 3 sec @ 260°C	265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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**Table 5. 10EP DC CHARACTERISTICS, PECL  $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 2)**

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	45	61	75	45	63	75	45	65	75	mA
$V_{OH}$	Output HIGH Voltage (Note 3)	2165	2290	2415	2230	2355	2480	2290	2415	2540	mV
$V_{OL}$	Output LOW Voltage (Note 3)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	2090		2415	2155		2480	2215		2540	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	1365		1690	1460		1755	1490		1815	mV
$V_{BB}$	Output Voltage Reference	1790	1890	1990	1855	1955	2055	1915	2015	2115	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4)	2.0		3.3	2.0		3.3	2.0		3.3	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	-150			-150			-150			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

2. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.3 V to -2.2 V.
3. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .
4.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 6. 10EP DC CHARACTERISTICS, PECL  $V_{CC} = 5.0\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 5)**

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	45	61	75	45	63	75	45	65	75	mA
$V_{OH}$	Output HIGH Voltage (Note 6)	3865	3990	4115	3930	4055	4180	3990	4115	4240	mV
$V_{OL}$	Output LOW Voltage (Note 6)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	3790		4115	3855		4180	3915		4240	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	3065		3390	3130		3455	3190		3515	mV
$V_{BB}$	Output Voltage Reference	3490	3590	3690	3555	3655	3755	3615	3715	3815	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 7)	2.0		5.0	2.0		5.0	2.0		5.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	-150			-150			-150			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

5. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +2.0 V to -0.5 V.
6. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .
7.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

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**Table 7. 10EP DC CHARACTERISTICS, NECL**  $V_{CC} = 0\text{ V}$ ,  $V_{EE} = -5.5\text{ V}$  to  $-3.0\text{ V}$  (Note 8)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	45	61	75	45	63	75	45	65	75	mA
$V_{OH}$	Output HIGH Voltage (Note 9)	-1135	-1010	-885	-1070	-945	-820	-1010	-885	-760	mV
$V_{OL}$	Output LOW Voltage (Note 9)	-1935	-1810	-1685	-1870	-1745	-1620	-1810	-1685	-1560	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	-1210		-885	-1145		-820	-1085		-760	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	-1935		-1610	-1870		-1545	-1810		-1485	mV
$V_{BB}$	Output Voltage Reference	-1510	-1410	-1310	-1445	-1345	-1245	-1385	-1285	-1185	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 10)	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	-150			-150			-150			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

8. Input and output parameters vary 1:1 with  $V_{CC}$ .

9. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .

10.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 8. 100EP DC CHARACTERISTICS, PECL**  $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 11)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	50	61	75	50	63	77	55	66	80	mA
$V_{OH}$	Output HIGH Voltage (Note 12)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
$V_{OL}$	Output LOW Voltage (Note 12)	1305	1480	1605	1305	1480	1605	1305	1480	1605	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	2075		2420	2075		2420	2075		2420	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	1305		1675	1305		1675	1305		1675	mV
$V_{BB}$	Output Voltage Reference	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13)	2.0		3.3	2.0		3.3	2.0		3.3	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	-150			-150			-150			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

11. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $+0.3\text{ V}$  to  $-2.2\text{ V}$ .

12. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .

13.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

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**Table 9. 100EP DC CHARACTERISTICS, PECL**  $V_{CC} = 5.0\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 14)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	50	61	75	50	63	77	55	66	80	mA
$V_{OH}$	Output HIGH Voltage (Note 15)	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
$V_{OL}$	Output LOW Voltage (Note 15)	3005	3180	3305	3005	3180	3305	3005	3180	3305	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	3775		4120	3775		4120	3775		4120	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	3005		3375	3005		3375	3005		3375	mV
$V_{BB}$	Output Voltage Reference	3475	3575	3675	3475	3575	3675	3475	3575	3675	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 16)	2.0		5.0	2.0		5.0	2.0		5.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	-150			-150			-150			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

14. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +2.0 V to -0.5 V.

15. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

16.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 10. 100EP DC CHARACTERISTICS, NECL**  $V_{CC} = 0\text{ V}$ ,  $V_{EE} = -5.5\text{ V}$  to  $-3.0\text{ V}$  (Note 17)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	50	61	75	50	63	77	55	66	80	mA
$V_{OH}$	Output HIGH Voltage (Note 18)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
$V_{OL}$	Output LOW Voltage (Note 18)	-1995	-1820	-1695	-1995	-1820	-1695	-1995	-1820	-1695	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	-1225		-880	-1225		-880	-1225		-880	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	-1995		-1625	-1995		-1625	-1995		-1625	mV
$V_{BB}$	Output Voltage Reference	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 19)	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	-150			-150			-150			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

17. Input and output parameters vary 1:1 with  $V_{CC}$ .

18. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

19.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

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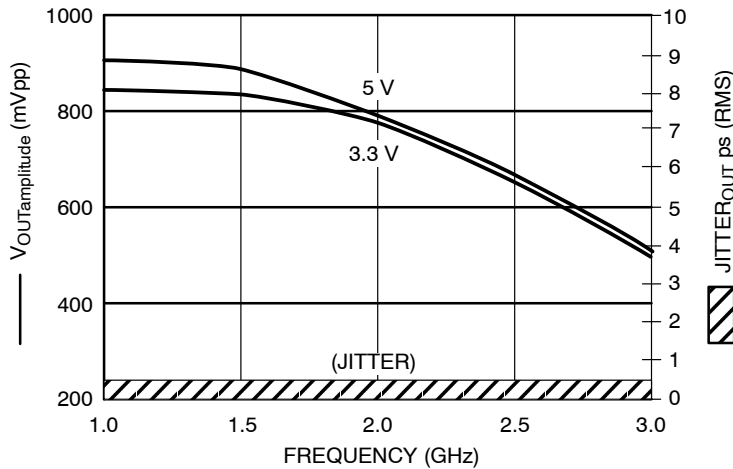
**Table 11. AC CHARACTERISTICS**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.0\text{ V to } -5.5\text{ V}$  or  $V_{CC} = 3.0\text{ V to } 5.5\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 20)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Frequency (See Figure 2 $F_{max}/JITTER$ )		> 3			> 3			> 3		GHz
$t_{PLH}$ , $t_{PHL}$	Propagation Delay to Output Differential  D to Q, $\bar{Q}$ SEL to Q, $\bar{Q}$ COM_SEL to Q, $\bar{Q}$	250 250 250	340 340 350	450 450 450	270 270 270	360 340 360	470 470 470	300 300 300	400 400 400	500 500 500	ps
$t_{SKEW}$	Within-Device Skew (Note 21) Device to Device Skew		50	100 200		50	100 200		50	100 200	ps
$t_{JITTER}$	Random Clock Jitter (See Figure 2 $F_{max}/JITTER$ )		0.2	< 1		0.2	< 1		0.2	< 1	ps
$V_{PP}$	Input Voltage Swing (Differential Configuration)	150	800	1200	150	800	1200	150	800	1200	mV
$t_r$ , $t_f$	Output Rise/Fall Times (20% - 80%)	70	120	170	80	130	180	100	150	230	ps

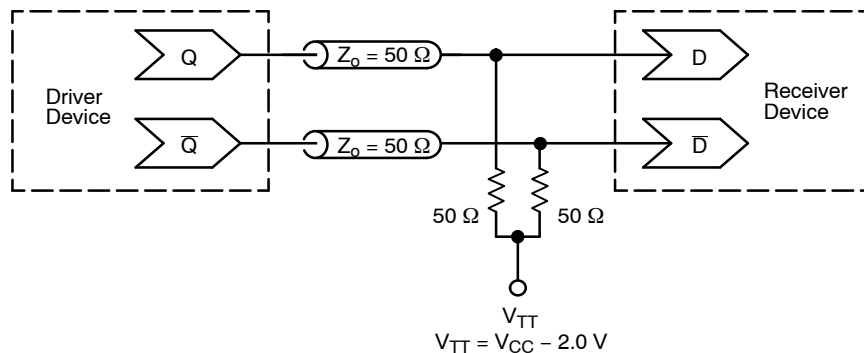
NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

20. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

21. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.



**Figure 2.  $F_{max}/Jitter$  @ 25°C**



**Figure 3. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note [AND8020/D](#) - Termination of ECL Logic Devices.)

## MC10EP56, MC100EP56

### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

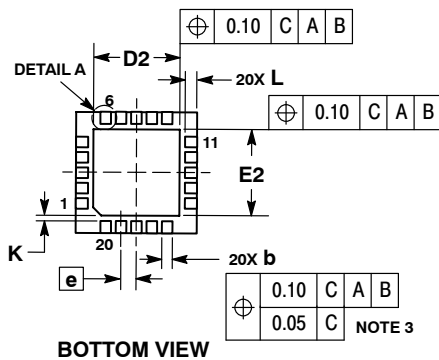
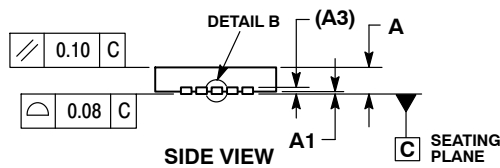
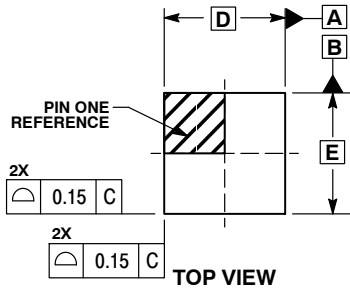
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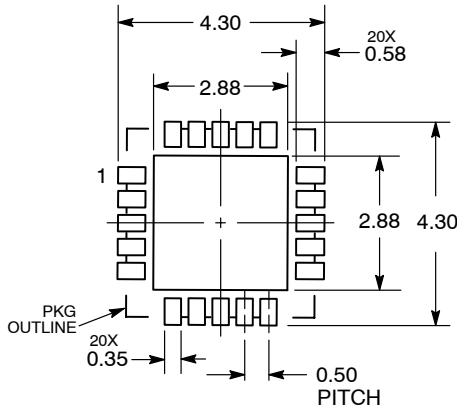
SCALE 2:1

QFN20, 4x4, 0.5P  
CASE 485E  
ISSUE C

DATE 13 FEB 2018

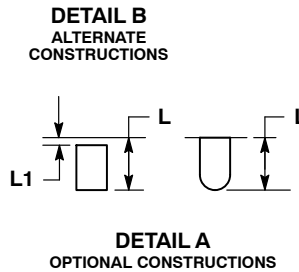
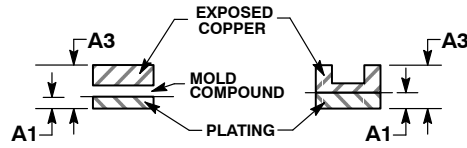


### SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

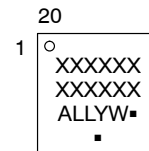


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20	REF
b	0.20	0.30
D	4.00 BSC	
D2	2.60	2.90
E	4.00 BSC	
E2	2.60	2.90
e	0.50 BSC	
K	0.20 REF	
L	0.35	0.45
L1	0.00	0.15

### GENERIC MARKING DIAGRAM\*



- XXXXXX= Specific Device Code
- A = Assembly Location
- LL = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

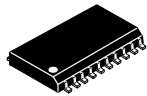
(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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<b>DESCRIPTION:</b>	<b>QFN20, 4X4, 0.5P</b>	<b>PAGE 1 OF 1</b>

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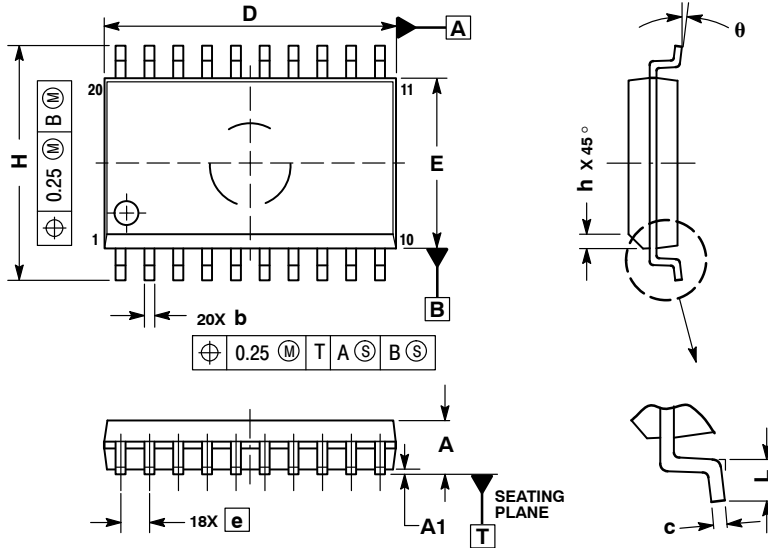
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-20 WB  
CASE 751D-05  
ISSUE H

DATE 22 APR 2015

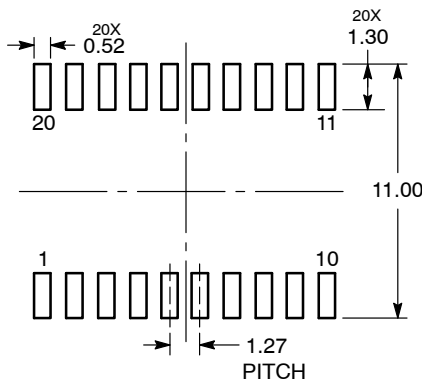


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

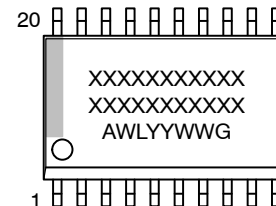
RECOMMENDED  
SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC  
MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

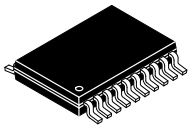
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DESCRIPTION:	SOIC-20 WB	PAGE 1 OF 1

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

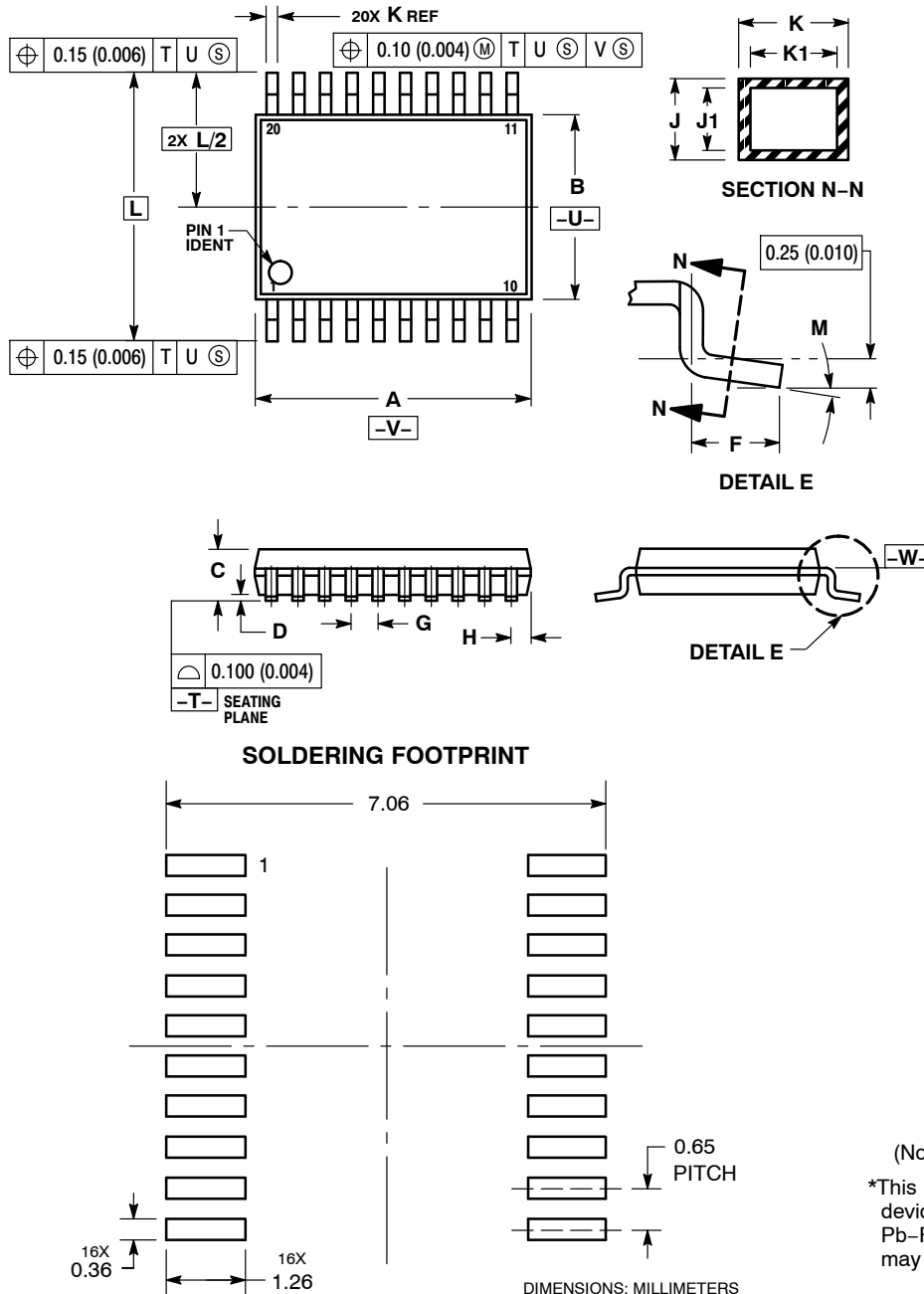
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TSSOP-20 WB  
CASE 948E  
ISSUE D

DATE 17 FEB 2016

SCALE 2:1

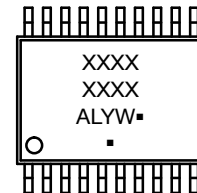


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**GENERIC MARKING DIAGRAM\***



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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