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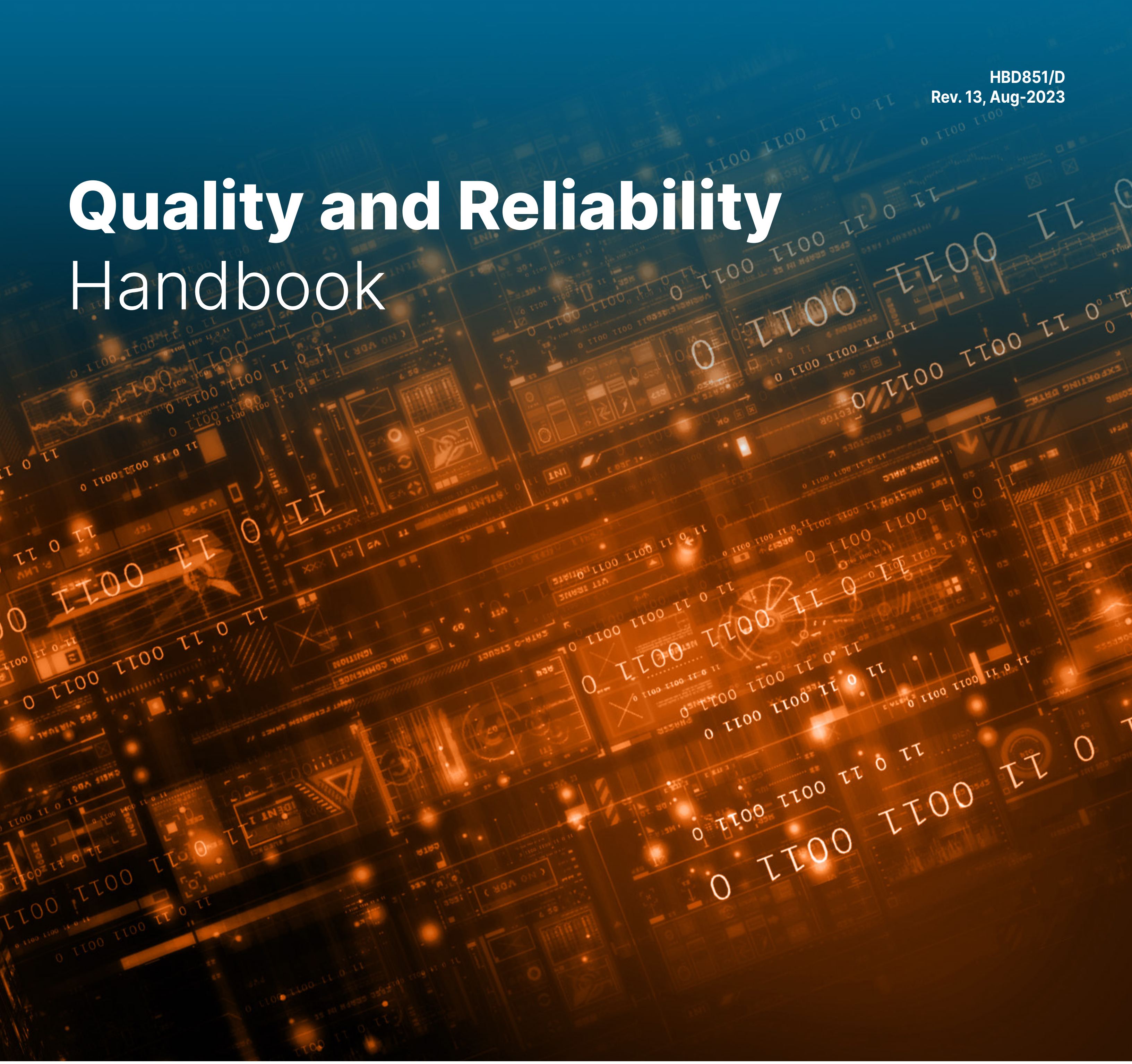

Quality and Reliability Handbook

Pushing innovation to create intelligent power and sensing technologies that solve the most challenging customer problems.

onsemi.com

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Dear Customer:

We are pleased to present you with the **onsemi** Reliability and Quality Handbook. **onsemi** is certified to ISO-9001, IATF-16949, AS9100, ISO-14001, ISO-45001, ANSI/ESD20:20, and military standards. Our medical manufacturing facility is certified to ISO-13845. We also received distinction by being classified as a 'Trusted Supplier'. Our Road to Zero Defect initiative recognizes the integrated effectiveness of building both "Reliability" and "Quality" into our services, processes, and products. We are committed to developing and maintaining a unique, world-class Quality system, which transcends all international Quality standards and truly exceeds customer expectations. This document intends to provide basic information on the reliability and quality aspects of the products supplied by **onsemi** worldwide. **onsemi** maintains a portfolio that includes a broad spectrum of products in a full array of package technologies, including but not limited to the following products:

- **Automotive Solutions:** Vehicle Electrification (SiC, High Power Modules, Drive Switch, SmartFET, Powertrain, Body Electronics, LED Lighting) & Advanced Safety (ADAS, Image Sensors & LiDAR Detectors)
- **Industrial Solutions:** Energy Infrastructure (GFCI, AFCI RSL10); Factory Automation (Intelligent Position Sensors, Machine Vision); and Charging Stations (Intelligent Power, SiC, IGBT)
- **5G & Cloud Power:** Multi-Phase & Power-Phase Controllers, Smart Power Stages, PMIC, POL, Switches, EFuse, Drivers, 48 V Topologies

onsemi is headquartered in Scottsdale, Arizona (U.S.A.) and has several international facilities with on-site parametric testing, reliability testing, and product analysis capabilities. **onsemi** has developed global marketing, sales, and field quality networks to supply its customers with quality products, information, and services.

Our Quality Statement/Policy reads, "At **onsemi**, we focus on embedding quality in every system, tool and process, with detailed attention to providing best-in-class products and solutions. This demonstrates our inherent zero-defect quality mindset, from ideation through execution and delivery, in support of consistent growth."

We believe in "safety first, quality always," as a priority of the organization's mission, and display it often to begin meetings on any topic, at any location. We also present data and information in this exact order to reinforce this concept continually.

Thank you for taking the time to read our Quality Handbook. Our customers are the reason why we place so much emphasis on quality. Hopefully, this booklet will provide you with a better understanding of our systems, procedures, and passion for providing quality products and services to you.

For additional questions, please contact 1 (800) 282-9855 or email us at continuity@onsemi.com.

Michael McCullar
Vice President, Global Quality
onsemi

Section 1 – Introduction

onsemi (Nasdaq: ON) is driving disruptive innovations to help build a better future. With a focus on automotive and industrial end-markets, the company is accelerating change in megatrends such as vehicle electrification and safety, sustainable energy grids, industrial automation, and 5G and cloud infrastructure. With a highly differentiated and innovative product portfolio, **onsemi** creates intelligent power and sensing technologies that solve the world's most complex challenges and leads the way in creating a safer, cleaner, and smarter world. **onsemi** operates a responsive, reliable, world-class supply chain and quality program, a robust compliance and ethics program, and a network of manufacturing facilities, sales offices, and design centers in key markets throughout the regions of North America, Europe, and Asia Pacific. For more information, visit www.onsemi.com.

The company's current portfolio numbers close to 60,000 products, including full Pb-Free, ROHS compliant device offerings. We ship more than 70 billion units annually to more than 2000 different customer locations. We deliver these products into the hands of our customers through a highly responsive supply chain. With our global logistics network and a strong portfolio of power semiconductor devices, **onsemi** is a preferred supplier of power solutions to engineers, purchasing professionals, distributors, and contract manufacturers in the computer, cell phone, portable devices, automotive and industrial markets.

Headquartered in Scottsdale, Arizona, we are a public company and trade on the NASDAQ under the symbol (ON). We employ approximately 34,000 people worldwide and have manufacturing facilities, sales, offices, and design centers throughout North America, Asia Pacific, and Europe. We strive to continuously meet our customers' current and anticipated semiconductor component needs. Our goal is to do this so well that "Customers come to us first!" We enact this vision each day by fulfilling our mission to eliminate any reason for the customer to buy from other suppliers by providing the highest quality components and services at competitive prices with the most reliable delivery and ease of purchase.

onsemi devices have achieved a variety of international certifications. More information about these certifications is available on our website. Customer satisfaction, customer confidence, and continuous improvement are the foundation of our success. These efforts touch every function and region of our business. Deeply ingrained in every employee is our quality resolve.

This handbook intends to review and provide information on the reliability and quality aspects of the semiconductor products supplied by **onsemi** worldwide.

In today's semiconductor marketplace, two crucial elements for a company's success are its quality and reliability systems. They are interrelated, reliability being the quality extended over the expected life of the product. For any manufacturer to remain in business, its products must meet or exceed the essential quality and reliability standards. **onsemi** has successfully established reliability and quality standards for products, processes, and services that exceed the basic standards and meet our customers' needs as a semiconductor supplier. This report uses the most stringent and demanding definitions of quality and reliability.

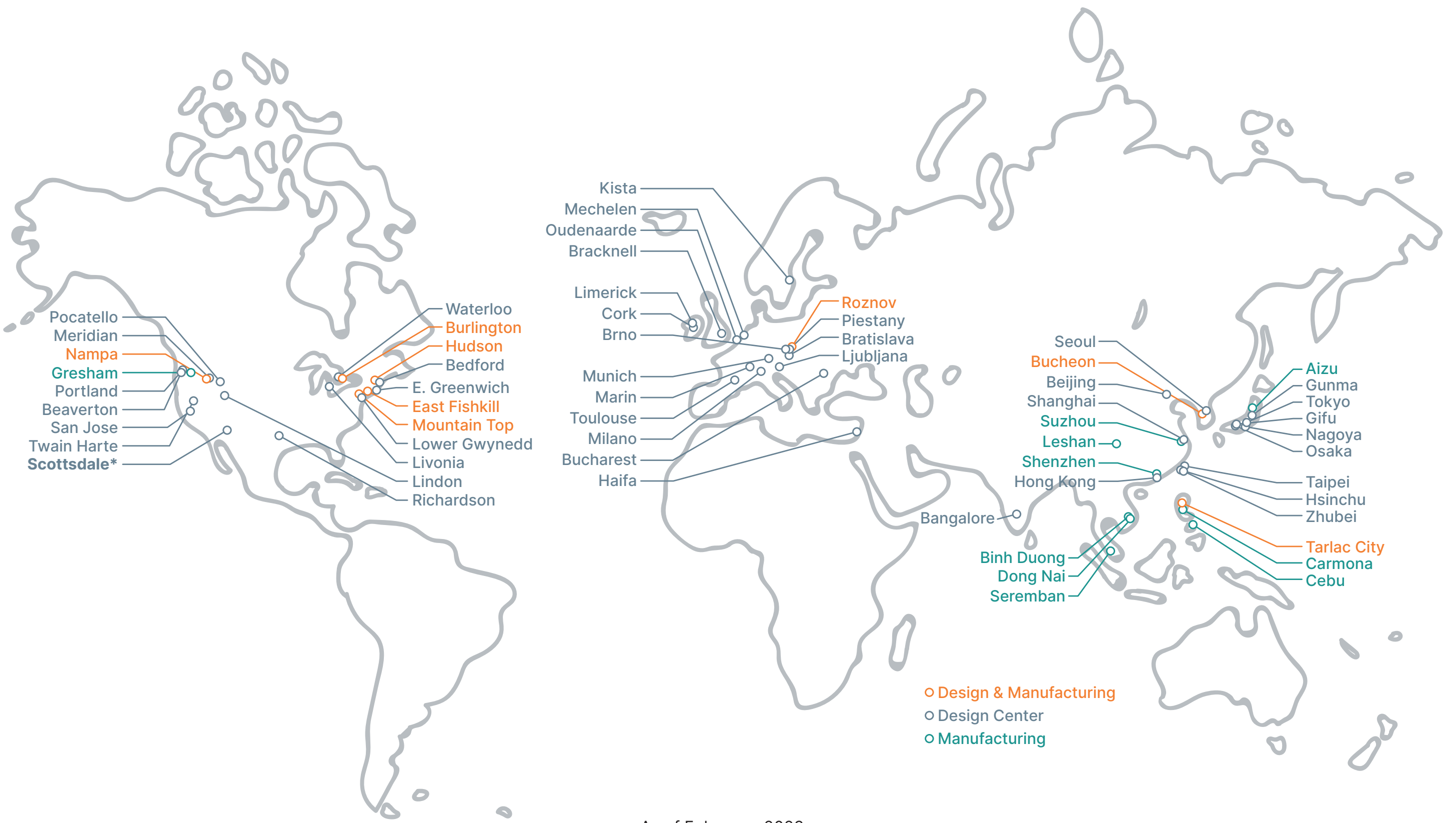
Quality may be defined as:
- Reduction of variability around a target to achieve conformance to customer requirements and expectations in a cost-effective way.
- The probability that a device (equipment, parts) will have performance characteristics within specified limits.
- Fitness for use.

Reliability is defined as:
- Quality in time and environment (temperature, voltage).
- The probability that a semiconductor device, which initially has satisfactory performance, continues to perform its intended function for a given time under actual usage environments.

At **onsemi**, we design our reliability and quality assurance program to generate ongoing data for the various product families' reliability and quality. We perform both reliability and quality monitors on the different major categories of semiconductor products. We design these monitors to test the product's design and material and identify and eliminate potential failure mechanisms to ensure reliable device performance in a real-world application. Thus, the program's primary purpose is to identify trends from the data generated and use that information to improve our products continuously. Also, our customers can use this reliability and quality data for failure rate predictions.

This handbook is a compilation of reliability test results and quality data from all semiconductor operations. The data contained are annual summaries of many detailed tests and evaluations performed in **onsemi** locations worldwide.

Detailed reliability reports for a product line or device type are available upon request and through your local **onsemi** Sales or Customer advocacy representative or from the sources indicated in this handbook



As of February, 2023

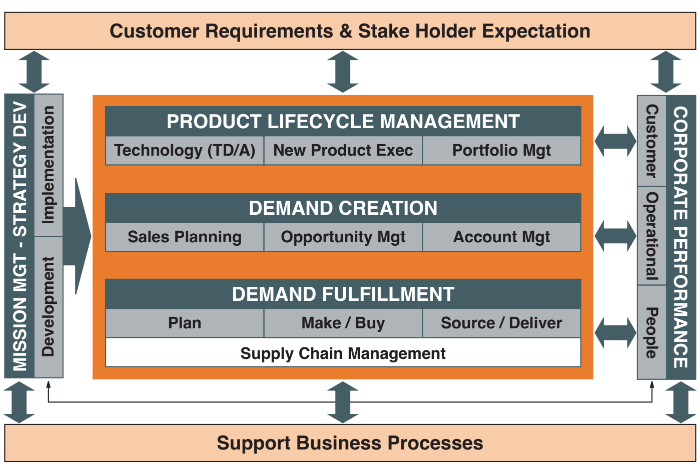
Section 2 – onsemi Quality System
(Based on our Core Business Process Model)

onsemi is registered to both ISO 9001 and IATF16949. **onsemi**'s Quality System and Business Operating System are synonymous. The company established a Core Business Process Model, shown below, that ensures we meet or exceed our customer's expectations and our business goals. We've adopted the approach of taking international standards and common customer requirements and aligning them into our existing Business Model.

Our Quality Statement/Policy reads, "At **onsemi**, we focus on embedding quality in every system, tool and process, with detailed attention to providing best-in-class products and solutions. This demonstrates our inherent zero-defect quality mindset, from ideation through execution and delivery, in support of consistent growth."

Our Core Business process model begins with the customer and ends with the customer.

Customer Business Process Model and Structure



Our core business processes are linked to our global work processes ensuring alignment between our business strategy and practices.

onsemi Certification Status

Each of our manufacturing sites, support, marketing, and design groups have been certified by Det Norske Veritas (DNV). Certificates are available on our website.

Six Sigma®

onsemi is committed to the Six Sigma philosophy in both our manufacturing and business environments.

Our Six Sigma efforts for the new millennium and beyond:

- Continue our efforts to achieve Six Sigma results in everything we do (products and services)
- Measure in parts per billion (ppb)

Customer Satisfaction

onsemi is engaged in a very competitive global marketplace. We cannot grow if we continue to focus only on our heritage and our past accomplishments. We continually strive to understand our customers' needs for service and support by focusing on customer service.

The feedback we receive on the quality of our products and services is a key driver. We strive to understand this to anticipate solutions to product and service needs that our customers have yet to recognize. We listen to our customers' ideas about how we can better serve them from a total system's perspective — from idea introduction to the successful delivery of product or service.

We gather this feedback by asking how our external customers perceive **onsemi** in terms of quality and their expectations via the Quality Survey once every two years. The objectives that accomplished through the Quality Survey are:

- Continue strengthening our business operating system by determining our customers' current business expectations.
- Provide a baseline measurement of our performance against those expectations.
- Provide feedback on our performance against customer expectations (trends).
- Track changing expectations to modify our quality system accordingly.
- Provide a basis for a consistent set of customer satisfaction metrics that check our internal quality measurements.

Therefore, each business must develop customer-driven indices – using factors established by the customer – and set aggressive improvement goals. Our Goals change over time as customers raise the bar when we meet their current expectations.

onsemi Learning and Development

onsemi has instituted education and training directly linked to the strategic company goals identified by the Executive Staff. All corporate-driven training delivered is targeted toward those areas. The training focus is reviewed annually in alignment with the corporate strategy to keep current with business needs. When the focus is determined, supporting training and education events are identified, designed, developed, and sourced to meet the need. This dynamic process includes inputs from the organization, the employees, and external market factors.

The organizational capability is assessed at the functional level, matched with the workforce's current skills, and gaps are filled accordingly. This job/skill match process allows alignment of business goals and job skill requirements.

The Lean Six Sigma Green and Black Belt training and SPC programs are examples of the many training programs developed by **onsemi**.

Section 3 – Introduction to Reliability & Quality Methods

For semiconductors, the often critical nature of the equipment using them leaves no room for failure. By their very nature, properly designed semiconductor devices should outlast the intended equipment's life expectancy, and careful processing ensures that each device meets the specifications to which it is designed.

The result of proper design and careful planning is a quality product.

The reliability and quality methods discussed in this handbook contribute to the attainment of Six Sigma performance in all of our operations.

Reliability Stress Tests

The following are brief descriptions of the tests commonly used in the reliability assessment. Not all of the tests listed are performed on each product. Other tests may be performed when appropriate. The information herein is typical of the testing performed. Variations to the following can be found throughout this document based on the specific device's limitations being tested.

AUTOCLAVE

Autoclave is a highly accelerated and destructive environmental test that measures device resistance to moisture penetration and the resultant effects of galvanic corrosion. Alternative test to Unbiased HAST.

Typical Test Conditions: T_A = 121°C, rh = 100%, p = 1 Atmosphere (15 psig), t = 24 to 240 hours.

Common Failure Modes: Parametric shifts, high leakage and catastrophic failure.

Common Failure Mechanisms: Die corrosion or contaminants such as foreign material on or within the package materials or poor package sealing.

UNBIASED HIGHLY ACCELERATED STRESS TEST

Unbiased Highly Accelerated Stress is the same as HAST (below) with no bias. UHAST accelerates the exact failure mechanisms as Autoclave.

Typical Test Conditions: T_A = 130°C, rh = 85% to 95%, p =2 Atmospheres, Bias = 80-100% of Data Book maximum rating, T = 96 to 240 hrs.

Common Failure Modes: Parametric shifts, high leakage, and catastrophic failure.

Common Failure Mechanisms: Die corrosion or contaminants such as foreign material on or within the package materials or poor package sealing.

HIGHLY ACCELERATED STRESS TEST

Highly Accelerated Stress Test uses a pressurized environment to produce extremely severe temperature, humidity, and bias conditions. HAST accelerates the same failure mechanisms as High Humidity High Temperature Bias and Temperature Humidity Bias.

Typical Test Conditions: T_A = 110-130°C, rh = 85% to 95%, p = 2 Atmospheres, Bias = 80% to 100% of Data Book maximum rating, t = 96 to 246 hours.

Common Failure Modes: Parametric shifts, high leakage, and catastrophic failure.

Common Failure Mechanisms: Die corrosion or contaminants such as foreign material on or within the package materials or poor package sealing.

HIGH HUMIDITY HIGH TEMPERATURE BIAS/TEMPERATURE HUMIDITY BIAS

This environmental test measures the moisture resistance of plastic encapsulated devices. A bias is applied to create an electrolytic cell necessary to accelerate corrosion of the die metallization. With time, this is a catastrophically destructive test. Alternative test to HAST.

Typical Test Conditions: T_A = 85°C to 95°C, rh = 85% to 95%, Bias = 80% to 100% of Data Book maximum rating, t = 96 to 1008 hours.

Common Failure Modes: Parametric shifts, high leakage, and catastrophic failure.

Common Failure Mechanisms: Die corrosion or contaminants such as foreign material on or within the package materials or poor package sealing.

HIGH TEMPERATURE GATE BIAS

This test is designed to electrically stress the gate oxide under a bias condition at high temperatures.

Typical Test Conditions: T_A = 150°C, Bias = 100% of Data Book maximum Vgs rating, t = 168 to 1008 hours.

Common Failure Modes: Parametric shifts in gate leakage and gate threshold voltage.

Common Failure Mechanisms: Random oxide defects and ionic contamination.

HIGH TEMPERATURE REVERSE BIAS /HIGH TEMPERATURE OPERATION LIFE

The purpose of these tests is to align mobile ions using temperature and voltage stress to form a high-current leakage path between two or more junctions.

Typical Test Conditions: T_A = 85°C to 175°C, Bias = 80% to 100% of Data Book maximum rating, t = 168 to 1008 hours.

Common Failure Modes: Parametric shifts in leakage and gain.

Common Failure Mechanisms: Ionic contamination on the surface or under the metallization of the die.

HIGH TEMPERATURE STORAGE LIFE

High temperature storage life testing is performed to accelerate failure mechanisms that are thermally activated by applying extreme temperatures.

Typical Test Conditions: T_A = 125°C to 200°C, no bias, t = 24 to 1008 hours.

Common Failure Modes: Parametric shifts in leakage, Vf, VCEs, RDSon and gain.

Common Failure Mechanisms: Bulk die and diffusion defects.

INTERMITTENT OPERATING LIFE

The purpose of this test is to accelerate the stresses on all bonds and interfaces between the chip and mounting face of the device that simulates repeated turn on and off of equipment, checking the integrity of both wire and die bonds using thermal stressing.

Typical Test Conditions: T_A = 25°C, Pd = Data Book maximum rating, T_{on} = T_{off} = 2-5 min (package dependent), DTJ of 125°C, t = 1000 to 15000 cycles.

Common Failure Modes: Parametric shifts and catastrophic failure.

Common Failure Mechanisms: Foreign material, crack and bulk die defects, metallization, wire, and diebond defects.

SOLDERABILITY

The purpose of this test is to measure the ability of device leads/terminals to be soldered after an extended period of storage or shelf life.

Typical Test Conditions: J-STD-002

Common Failure Modes: Pin holes, dewetting, non-wetting.

Common Failure Mechanisms: Poor plating, contaminated leads.

SOLDER HEAT

This test measures a device's ability to withstand the temperatures seen in wave soldering operations. Electrical testing is the endpoint criterion for this stress.

Typical Test Conditions: Solder Temperature = 260°C, t = 10 seconds.

Common Failure Modes: Parameter shifts, mechanical failure.

TEMPERATURE CYCLING (AIR-TO-AIR)

The purpose of this test is to evaluate the ability of the device to withstand both exposures to extreme temperatures and transitions between temperature extremes. This testing also exposes the excessive thermal mismatch between materials.

Typical Test Conditions: T_A = -65°C to 150°C, cycle = 100 to 1000.

Common Failure Modes: Parametric shifts and catastrophic failure.

Common Failure Mechanisms: Wire bond, cracked or lifted die, and package failure.

Reliability Data Analysis

Reliability is the probability a semiconductor device will perform its specified function for a specified time period under specified environmental conditions. In general, reliability is the maintenance of acceptable quality performance over time and environmental conditions. A key characteristic of reliability is the hazard rate h(t). The hazard rate roughly represents the rate devices fail as a function of time. The most widely used probability distribution used for analyzing semiconductor device reliability data is the exponential distribution. The hazard rate function for the exponential distribution l (this is usually called the failure rate) is not a function of time and is very simple to estimate. The point estimate of the failure rate is obtained by dividing the number of observed failures by the total number of device-hours from the stress test. Device-hours is defined as the product of the number of devices that are stress tested and the duration of the stress test. This is called the point estimate because it is based on a sample of devices from the population of all devices with similar characteristics. It does not account for the uncertainty caused by estimating the failure rate from a sample. For modern semiconductor devices, the failure rates are extremely low, and the failure rate is presented in units of FIT, where FIT is the number of failures per billion device-hours. These calculations are appropriate when the exact failure times are known. More complicated censoring situations can be analyzed using techniques presented elsewhere (e.g., Meeker and Escobar, “Statistical Methods for Reliability Data,” (1998)).

To account for the uncertainty due to calculating the failure rate based on a sample, one must apply confidence limits to the point estimate. The relevant confidence interval for device reliability calculations is the one-sided upper confidence interval of the failure rate. The one-sided upper confidence interval estimates the failure rate that is unlikely to be exceeded by any given point estimate at a given confidence level. The appropriate sampling distribution for the failure rate of the exponential distribution is the chi-square distribution $\chi 2$. If one were to calculate the failure rate of many independent samples drawn from the same exponential population, then the distribution of the point estimates of the failure rate would follow a $\chi 2$ distribution. The one-sided upper confidence estimate of the exponential failure rate where the life test is time-censored is given by:

$$\lambda_{1\text{-sided}} = \frac{\chi^2(\alpha, 2r+2)}{2nt} 10^9$$

where:

$\lambda_{1\text{-sided}}$ = one-sided upper confidence level failure rate estimate in FIT

χ^2 = the inverse cumulative distribution function for the chi-square distribution

α = (100 — confidence level)/100

r = number of failures observed during the stress test

n = number of devices in stress test sample

t = stress test duration in hours

Table 1 provides the inverse cumulative distribution function values for the chi-square distribution for the 60% and 90% confidence levels.

Table 1. Chi-Square Inversion Cumulative Distribution Function

60% Confidence Level		90% Confidence Level	
No. Fails	χ^2 Quantity	No. Fails	χ^2 Quantity
0	1.833	0	4.605
1	4.045	1	7.779
2	6.211	2	10.645
3	8.351	3	13.362
4	10.473	4	15.987
5	12.584	5	18.549
6	14.685	6	21.064
7	16.780	7	23.542
8	18.868	8	25.989
9	20.951	9	28.412
10	23.031	10	30.813
11	25.106	11	33.196
12	27.179	12	35.563

Due to continuous process improvements and advances in device and package technologies, the failure rate of semiconductor devices is extremely low. To assess these devices’ reliability accurately, reliability engineers routinely use accelerated stress test conditions during reliability testing. Carefully chosen test conditions accelerate the failure mechanisms expected to occur under normal use conditions without introducing spurious failure mechanisms. Accelerated stress testing provides estimates of device reliability performance under use conditions and identifies opportunities for improving the device’s reliability performance. Failure mechanisms found during stress testing are traced to the root cause and eliminated whenever possible.

The most commonly used stress accelerator is temperature. In most cases, elevated temperature increases the rate at which a given failure mechanism progresses. Using lower temperatures accelerates a few failure mechanisms. The simplest thermal acceleration model is the Arrhenius equation, where:

$$\text{Rate} = A_o e^{\frac{E_a}{kT}}$$

Rate = rate of progress for a given failure mechanism

A_o = pre-exponential factor that is a characteristic of the given failure mechanism s^{-1}

Ea = Thermal activation energy of the failure mechanism in eV

k = Boltzman constant, $8.617 \cdot 10^{-5}$ eV/K

T = device junction temperature in degrees Kelvin

Using the Arrhenius equation, one can relate the failure rate at one stress condition to the failure rate at a different condition. The acceleration factor A_f is defined in the following manner:

$$A_f = \frac{\text{Rate (Condition 1)}}{\text{Rate (Condition 2)}}$$

where:

Rate (Condition 1) = rate of progress for a given failure mechanism at Condition 1 (i.e., T_1)

Rate (Condition 2) = rate of progress for a given failure mechanism at Condition 2 (i.e., T_2)

The thermal acceleration factor becomes:

where:

$$A_f = e^{\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)}$$

T_1 and T_2 = device junction temperatures at stress conditions 1 and 2, respectively.

See Figure 1 for an example of how the acceleration factor is used to transform the stress testing time into the equivalent time at a typical use junction temperature.

ACTIVATION ENERGY

onsemi uses the industry-standard estimates for activation energies documented in JEDEC Publication JEP122, “Failure Mechanisms and Models for Siliconsemi Devices.” The following table summarizes the most commonly used activation energies.

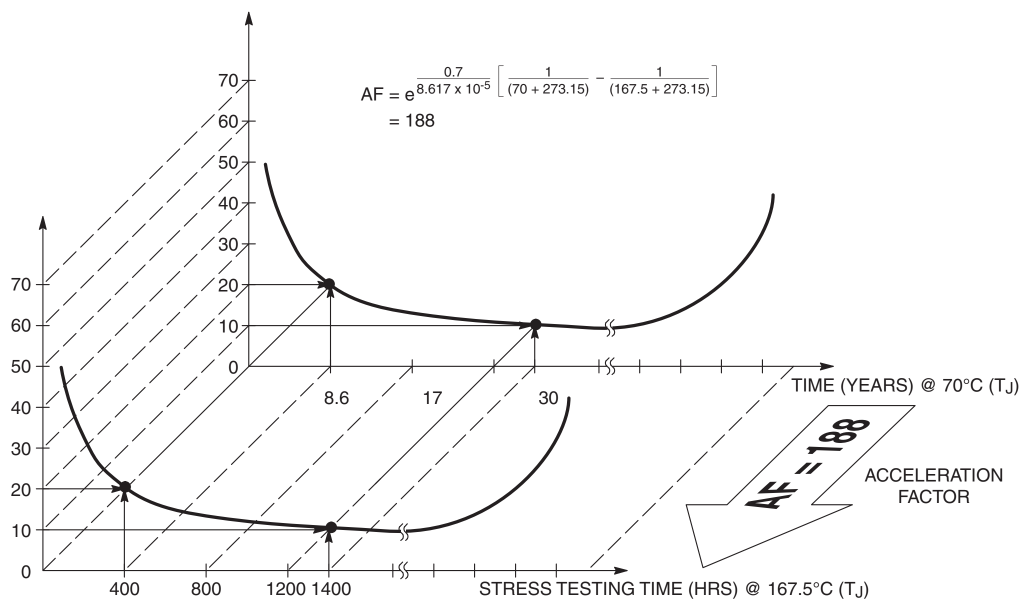


Figure 1. Example of Temperature Acceleration Factor

(0.7 eV Activation Energy)

Table 2. Activation Energy

Device Association	Failure Mechanism	Accelerating Failures	Typical Activation Energy (eV)
Silicon Surface Oxide	Surface Inversion Mobile Ions Charge Accumulation Surface Charge Spreading	T, V	1.0 1.0 1.0 0.7
Gate Oxide	Dielectric Breakdown Thin Oxide (< 40 nm) Thick Oxide (≥ 40 nm)	E, T	 0.3 0.7
Metallization	Electromigration Pure Al AlSi (≤ 1.5%) AlSi (1.5%) AlCu (0.5%) AlCuSi (1% Si, 2% Cu) AlCu over TiW (>1% Cu)	J, T	 0.48 0.50 0.72 0.70 0.70 0.71
	Corrosion General With Chlorine With Phosphorus	H, E/V, T, V	 0.8 0.7 0.53
Assembly Process	Intermetallics Bromine-induced Halide-induced Chloride-induced	T	 1.0 0.5 0.8
	Wire Bond Die Attach	T, ΔT T, ΔT	0.75 0.30

T = Temperature, ΔT = Temperature Cycling, V = Voltage, E = Electric Field, J — Current Density, H = Humidity

THERMAL RESISTANCE

Circuit performance and long-term circuit reliability are affected by die temperature. Typically, keeping the junction temperatures low improves both.

Electrical power dissipated in any semiconductor device is a source of heat. This heat source increases the temperature of the die about some reference point, usually the ambient temperature of 25°C in still air. The temperature increase depends on the amount of power dissipated in the circuit and the net thermal resistance between the heat source and the reference point.

The junction temperature depends on the packaging and mounting system's ability to remove heat generated in the circuit from the junction region to the ambient environment. The basic formula for converting power dissipation to estimated junction temperature is:

$$T_J = T_A + P_D (\bar{\theta}_{JC} + \bar{\theta}_{CA})$$

or:

$$T_J = T_A + P_D (\bar{\theta}_{JA})$$

where:

T_J = maximum junction temperature
T_A = maximum ambient temperature
P_D = calculated maximum power dissipation, including effects of external loads when applicable
$\bar{\theta}_{JC}$ = average thermal resistance, junction-to-case
$\bar{\theta}_{CA}$ = average thermal resistance, case-to-ambient
$\bar{\theta}_{JA}$ = average thermal resistance, junction-to-ambient

The user can vary only two terms on the right side of equation (1), the ambient temperature and the device case-to-ambient thermal resistance, θ_{CA}. (To some extent, the device power dissipation can also be controlled, but under recommended use, the supply voltage and loading dictate a fixed power dissipation.) Both system airflow and the package mounting technique affect the θ_{CA} thermal resistance term. θ_{JC} is essentially independent of airflow and external mounting methods but is sensitive to package material, die bonding method, and die area.

For applications where the case is held at essentially a fixed temperature by mounting on a large or temperature-controlled heat sink, the estimated junction temperature is calculated by:

$$T_J = T_C + P_D (JC) (\bar{\theta}_{JC})$$

where T_C = maximum case temperature and the other parameters are as previously defined.

AIR FLOW

Airflow over the packages (due to a decrease in θ_{CA}) reduces the package's thermal resistance, therefore, permitting a corresponding increase in power dissipation without exceeding the maximum permissible operating junction temperature. For thermal resistance values for specific packages, see the **onsemi** data sheet or application note for the appropriate device family or contact your local **onsemi** sales office.

Section 4 – Customer Product/Process Change Notification

onsemi is committed to delivering superior quality products to our valued customers and providing cost-effective solutions. This commitment to continuous improvement in quality and value requires us to change our product portfolio periodically. The change management "process," described below, is compliant with all international quality system standards such as ISO 9001, IATF16949, AS9100, Mil-PRF-38535, J-STD-046, J-STD-048, and mutually agreed Customer Specific Requirements.

Along with our commitment to quality and value, **onsemi** manages necessary product changes with a rigorous evaluation and characterization methodology to make them fully "transparent" to our valued customers from an electrical, physical, and thermal performance standpoint.

Change Management Overview

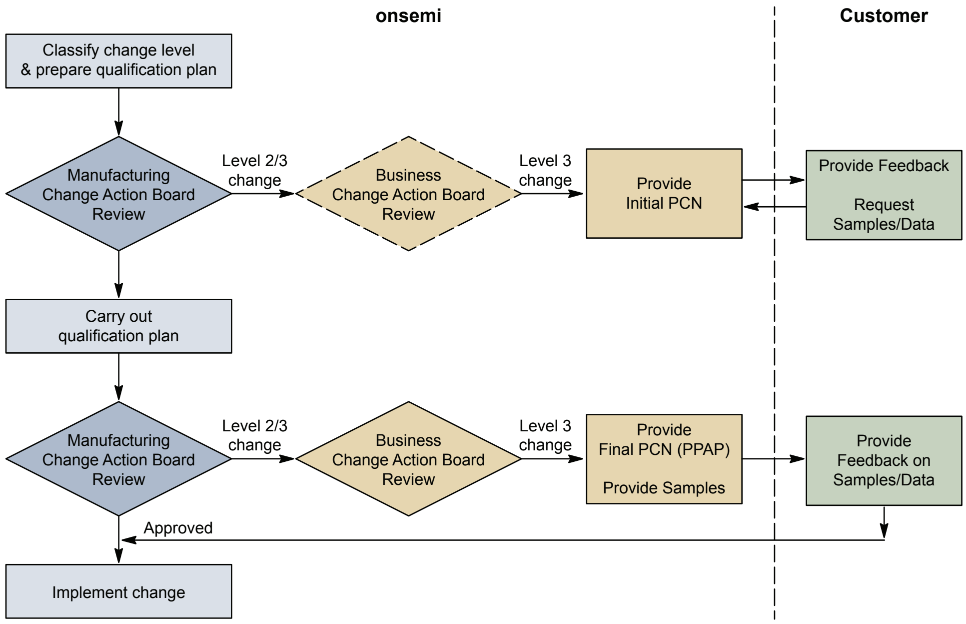
All proposed changes are classified into one of three classes and are determined by the proposed change's nature and scope. The classification level indicates the level of qualification testing and customer notification required. The corporate Business Change Action Board (BU CAB), an independent body chartered to represent the customer's best interests with representatives from Quality & Reliability, the Business Units, Engineering and Manufacturing, assigns the classification level. Before submittal for Business Change Action Board review, the local manufacturing engineering reviews and approves any potential changes first in the Manufacturing Change Action Board (Mfg CAB). This two-tiered requirement for review and approval provides a thorough analysis of all changes for proper evaluation and risk mitigation.

Level 1 changes include any minor change to the materials, process method, process equipment, or design, which does not affect the visual appearance, external dimensions, tolerances, or the finished product's performance. Level 1 changes do not require reliability testing or customer notification but require product characterization before implementation.

Level 2 changes include any substantial change to the materials, process method, process equipment, or design, which does not affect the finished product's external dimensions and tolerances or performance. Level 2 changes may affect the visual appearance if the difference is purely cosmetic in nature and does not impact customer usage of the product. Level 2 changes require product characterization and reliability testing but do not require customer notification before implementation.

Level 3 changes include any substantial change to the materials, process method, process equipment, or design, affecting the visual appearance, external dimensions, tolerances, or performance of the finished product. It is also called 'major changes' in standard J-STD-046. Level 3 changes also include transferring existing wafer fabrication or assembly processes to a new manufacturing site. Level 3 changes require both product characterization and reliability testing and communication to customers.

The Change Management Policy of **onsemi** is to inform customers about Level 3 product and process changes in as many as three stages of communication.



Initial Product/Process Change Notification (IPCN) – This "Initial Notification" is the first formal notification distributed to customers. The IPCN is optional and gets typically distributed 30 days before the publication of the final PCN. The IPCN contains the qualification plan that must be completed before implementation, which allows our valued customers to request any additional testing they might require to approve the change. The qualification plan's content depends on the nature and scope of the change but must comply with applicable JEDEC and AEC standards in all cases.

Final Product/Process Change Notification (FPCN) – This 'Final Notification' completes the notification process. The FPCN must be distributed at least 90 days before the change's effective date or implemented earlier when approved by the customer. The FPCN must contain successful results of all characterization and reliability testing documented in the qualification plan. Before issuing the FPCN, the characterization and reliability data is again reviewed and approved by both the internal Manufacturing and Business Change Action Boards. The 90-day advance notification provides our valued customers with a final opportunity to communicate any additional requirements to accept the change before implementation if necessary. The PCN notification process and format are compliant with J-STD-046.

Product Discontinuance (PD) – A special type of Notification when the product/process goes to end-of-life. The Product Discontinuance notice is distributed to customers at least 6 months in advance for the last purchase (Last Time Buy) and 6 months for the last shipments. The Product Discontinuance process is compliant with J-STD-048.

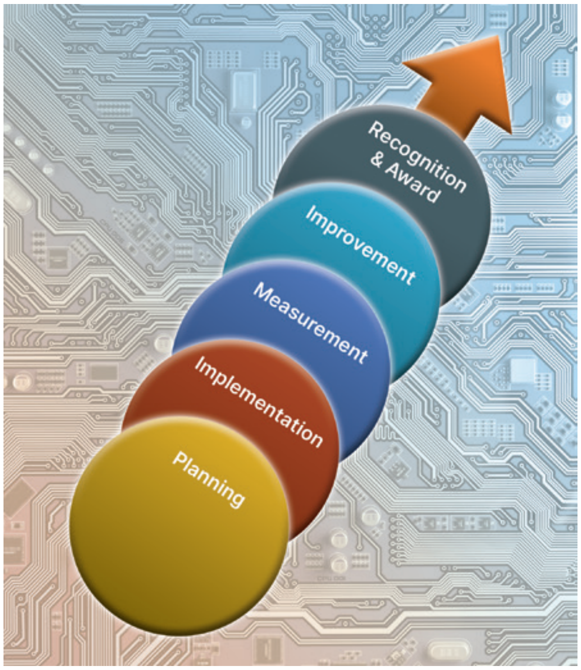
Process Change Management Portal – The customer receives an email notification with hyperlinks to the PCN document and a customized list of the affected part numbers. The customer should acknowledge receipt of the PCN within 30 days of delivery of the Notification. Opening the hyperlink to the PCN document in the Email Notification performs as an acknowledgment of receipt. Lack of acknowledgment of the Notification within 30 days constitutes acceptance of the change. Published notifications for standard products are publicly accessible by everyone on the external **onsemi** website. Company-specific (customized) notifications can be retrieved from the **onsemi** website but require a login.

Section 5 – Supplier Quality Process

onsemi follows a five-step Supplier Development process to improve the quality of goods and services delivered by our suppliers, including Planning, Implementation, Measurement, Improvement, and Recognition and Award.

We establish general expectations of doing business with **onsemi** during the planning phase and make our supplier selection based on their Quality System, Technical Capability, Value Added Services, Cost, and Capacity. Suppliers are requested to perform a Quality System self-evaluation to VDA6.3 requirements.

After selecting a potential supplier, the supplier must pass our qualification process before making any production shipments; this is the Implementation step of our Supplier Development Process. To pass our qualification requirements, suppliers must provide samples and data demonstrating that their product conforms to our specifications and their ability to manufacture the product consistently. This process includes a review of First Article Inspection data, Process Control and Measurement System Analysis data, and an on-site audit by **onsemi** (for new suppliers). Any significant process changes made by the supplier go through the same qualification process described above managed through our CAB process.



Once qualified, a supplier enters into the Measurement stage. We verify the material we use in production in one of three ways before use in production. The three methods are Inspection, Audits combined with measurement of acceptable performance, and receipt and review of SPC data. If material has been received that does not conform to our specified requirements, we utilize our automated corrective action tracking system to ensure suppliers respond to the problem using an 8D corrective action. Every quarter we measure our supplier's performance in the areas of Quality, Cost, Delivery, Service, and Technology. We share this data with our suppliers both via email and during Business Review Meetings. We also have an ongoing supplier assessment process (to VDA6.3 requirements) prioritized based on their certification status and ongoing performance as measured by our rating system.

In the Improvement stage, we establish goals with our suppliers using our Supplier Goal Plan (SGP) Process. It enables us to define our suppliers' priorities clearly, provides a follow-up method, and verifies suppliers are meeting our goals. We review the SGP with suppliers during Business Review meetings.

The final step in our Supplier Development Process is Recognition and Award. **onsemi** understands the value of recognizing and awarding suppliers for their hard work and dedication. We set a standard for all our suppliers to achieve by recognizing our best suppliers for their superb performance.

Section 6 – Failure Analysis

Overview

Failure analysis is a process that entails vast analytical methods and techniques to solve the reliability and quality issues that may occur in either the manufacturing or application of our products. The process can be a rather complicated endeavor due to the many aspects of the ever-advancing semiconductor and packaging technologies and the numerous engineering disciplines involved. The failure analyst must be proficient in design, process, assembly, test, and applications, which equates to electrical, physics, chemical, and mechanical engineering.

Failure analysis laboratories are available globally at most **onsemi** manufacturing sites. We use these analytical tools for good unit analysis, process characterization, destructive physical analysis, construction analysis, and even competitive benchmarking studies. Tool development for failure analysis is advancing at a similar rate as that of manufacturing. For the labs to stay current with technology, the analyst must continually develop the associated tools and techniques. As the die features are shrinking and become covered with multiple layers of interconnects, failure analysis requirements need to be anticipated as early as the design cycle. By incorporating these specialized test structures and functional test coverage, problems can more easily be diagnosed. In addition to tools, trained personnel, techniques, and procedures, the labs should employ an adequate database and tracking system to assist in expeditious problem-solving.

onsemi equips the labs in a diverse range of instrumentation and engineering expertise to solve problems in all aspects of semiconductor and packaging analysis. Failure analysis's success arises from a superior instrumentation set and its people and their approach to problem-solving. While the failure analysis lab may identify a failure mechanism, the road to the root cause is just begun. Depending on the manufacturing process complexity, root cause analysis may entail extensive experimentation and designed experiments to identify the root cause and verify potential corrective action effectiveness. The complete process of problem-solving entails multiple labs and techniques. These analytical professionals and the subject matter experts, such as design or manufacturing, work in unison to solve the problem.

Generic Process Steps

Section 9 – Customer Returns on page 17, outlines the entire sequence of the problem-solving events. The following steps outline the basic procedures that the failure analysis lab subjects to a typical field return.

Required Information

A minimum set of background information significantly impacts the overall quality and cycle time of the problem-solving process – the more information, the better. The minimum set and some questions are as follows:

1. Failure history and failure rate at the customer site in either this application or other products. Is this a new product, or have any changes occurred in this time frame?
2. Length of time in the application, including the conditions upon failure. Did any other components fail at the same time, and if so, how did they fail? Can a schematic be sent? Are there any devices of this same date code still available?
3. What is the application's failure mode, and how can it be related to this device? How do you perceive that the device is failing (short, open, stuck logic levels)?
4. How was the device handled before receipt at onsemi? Were precautions taken in removing and handling (ESD/thermal) the devices to ensure that electrical or physical damage does not occur and the package's testability is maintained?

Receipt of Request

When the failure analysis lab receives the product, the devices have generally been confirmed as failures through the use of automatic test equipment to achieve rapid failure verification by our customer support group. At this point, the background documentation, electrical results, and historical failure data are reviewed to outline the appropriate course of analytical action. An external visual inspection is carried out, documenting the package's physical condition and markings.

Diagnostic Testing

The labs subject the devices to a benign "pin-to-pin" test that quickly identifies parametric anomalies compared to known good units. Depending on the failure mode, the labs may subject the device to a more extensive bench test with stress conditions applied to match the customer's application or stimulate the mechanism.

Data Analytics

As a technology company, **onsemi** employs advanced data driven analytics to assist in our device analysis process. Our vast storage, decades of device data, advanced analytic techniques, and experienced analysts allow for accurate data mining and the quick assessment of many issues. By employing data analytics early in the process, we significantly reduced our overall response time and increased the accuracy of device analysis.

Non-destructive Testing

Failure analysis in itself is reverse engineering and, in this vein, destructive to the returned product. Because the labs partially destroyed the package to expose the die, they first carry out non-destructive techniques to observe the package or assembly-related mechanisms. The most common techniques used are acoustic microscopy and radiographic (XRAY) inspections to look for internal assembly or molding anomalies.

Storage Bakes or Stress

Depending on the failure mode, the analyst may subject the device to a series of vacuum or storage bakes to observe parametric or functional shifts. If the original failure mode were not confirmed, the labs would carry out stress testing (high-temperature bias, for instance) to observe possible longer-term reliability concerns.

Decapsulation or Package Preparation

The general course of action at this point is to reveal the die surface. In the case of a plastic encapsulated component, this would entail a chemical decapsulation. There are, however, many methods utilized for decapsulation or package preparation, dependent on the package, failure mode, and potential failure mechanism.

Internal Inspection

The labs would then carry out an internal optical inspection to check for any obvious assembly anomalies or wafer fabrication issues. Possible re-testing is recommended at this point to ensure that the failure mode has not changed.

Internal Diagnostic Testing

In many cases, the internal inspection does not reveal an obvious failure mechanism. At this point, depending on the technology and level of testability, the lab would utilize one or more of the techniques available to isolate the failure site. It could entail extensive probing or a technique, such as thermography or photoemission, to highlight potential anomalies. The majority of these techniques attempt to observe the failure site's properties, as in thermal dissipation or photon emission. The labs may use navigational tools, a laser cutter, or a Focused Ion Beam (FIB) to assist in device and circuit isolation from a probing standpoint.

Deprocessing

Deprocessing is an iterative process of removing a layer of the die, which may entail both wet chemistry and dry plasma etching techniques to reveal the underlying structures. The proper techniques are critical during these steps due to the process's destructive nature and the potential loss of vital information.

Analysis of Failure Site

Once a potential site has been determined or revealed, the labs may conduct further documentation and analysis. Additional analytical techniques are employed depending on whether the morphology or material composition is required.

Report Conclusion

Upon completion of the analysis, the labs generate a written report documenting the work. The report should state the relationship of the physical anomaly to the failure mode. It should also include sufficient documentation for root cause analysis by the manufacturing site if warranted.

Summary

The cost of failure analysis is high due to the extensive instrumentation, highly technical staff, continual training and development, and associated analysis expenses (chemicals, fixtures). The background documentation (see Required Information on the previous page) must be completed upon receipt to enable these resources' most efficient utilization. An open communication channel between **onsemi** and our customers exists to ensure a timely resolution of the problem on either end.

Section 7 – Reliability Data Summary

onsemi performs extensive reliability stress testing on devices that span the full breadth of our product portfolio. **onsemi** collects Reliability Data in the Reliability Audit Program and during the standard product qualification and re-qualification process. The data is updated periodically to include the most recent test results and quarterly. The reliability data links on the **onsemi** website provide the current data.

Section 8 – External Manufacturing Quality

onsemi utilizes packaging and testing subcontractors, foundry, external wafer fabrication manufacturers, and joint venture partners to support our customers' increasing requirements for high-quality, low-cost semiconductors. Our global subcontractor, foundry, and joint venture partners perform some or all areas of semiconductor manufacturing, including design, wafer fabrication, wafer probe, assembly, test, calibration, product analysis, and reliability testing. The selection and engagement of a new manufacturing design, subcontractor, foundry, or lab requires an extensive review and audit to ensure the supplier meets the quality, business, and technical requirements of **onsemi**. The review may include, but not limited to, the Supplier's quality certifications, quality management systems, sub-supplier quality control, corporate social responsibility, environmental controls, business continuity plans, new product development, product qualification, product manufacturing control, change control, machine capability and maintenance, process documentation and control, training and certification of personnel, and FMEA's.

Quality systems vary from subcontractor to subcontractor and foundry to foundry; however, **onsemi** requires each supplier to manufacture our products with the same high-quality standards as our internal factories. The new product introduction and process change control requirements and specifications are the same for internal **onsemi** factories and the selected external manufacturing suppliers. Additionally, we extend many of our internal factories' quality system practices to our external partners.

We continuously monitor, control, and re-evaluate the effectiveness of all suppliers through the following process:

1. Supplier scorecards.
2. Periodic subcontractor and foundry audits to review progress to critical metrics, including customer quality and delivery.
3. Joint corrective action plans to drive the resolution of identified issues and continuous improvements.
4. High-risk suppliers, targeted for continuous improvement and supplier focus using aggressive improvement plans and goals, are continuously evaluated until closure.
5. Detailed project management methodology to drive projects to timely completion.
6. Partnership with each subcontractor and foundry to pursue outside certification to drive their quality system improvements.

Section 9 – Customer Returns

onsemi's Global Customer Return or Incident process is focused on formal Problem Solving and Responsiveness. We use the 8D Problem Solving Methodology to determine Containment, Root Cause, and Corrective/Preventive Actions.

The Eight Disciplines are:

D1 – Establish the Team — Establish a cross-functional team of people with the process/product knowledge to solve the problem.

D2 – Describe the Problem — Specify the who, what, where, why, how, and how many of the customer's problem in quantifiable terms.

D3 – Implement and Verify Containment — Define and Implement containment actions to isolate the effect of the customers' problem until the implementation of corrective actions.

D4 – Define and Verify Root Cause — Identify all potential causes that could explain why the problem occurred and how it escaped our testing. Isolate and verify root cause by testing each potential cause against the problem description.

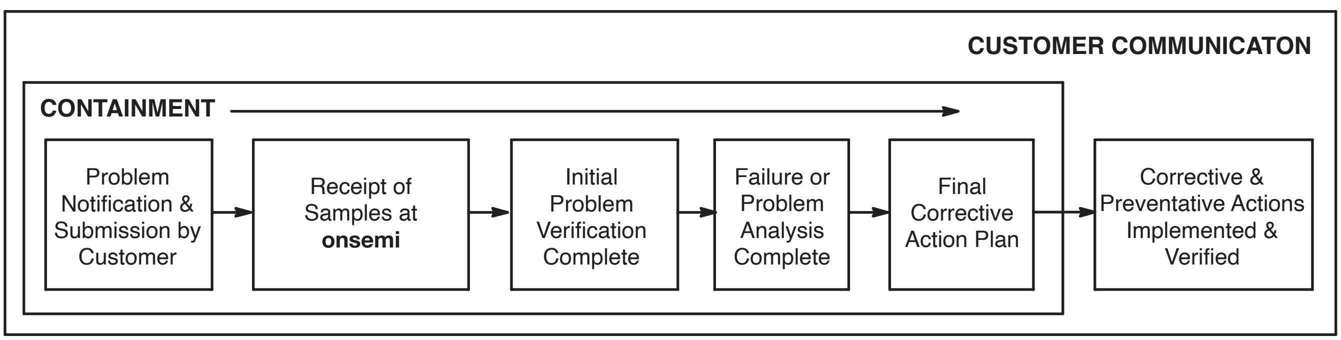
D5 – Choose and Verify Permanent Corrective Action — Identify all potential corrective actions for the Occur and Escape Root Causes. Verify actions that correct the root cause.

D6 – Implement Permanent Corrective Action — Provide action plans for implementation of the verified corrective actions. Follow up on any outstanding actions.

D7 – Prevent Recurrence — Implement actions to address the "system" failure. Update control plans, FMEA specifications, process specifications. Fan-Out Corrective Actions to appropriate manufacturing sites and other Technologies.

D8 – Congratulate the Team — We communicate to the customer throughout the process.

Customer Incident Process Map



Our Customer Incident information system tracks Customer Incidents. Monthly customer incident metrics are compiled and distributed corporate-wide. Responsiveness metrics drive continuous improvement in the Cycle Time arena. Failure Mechanism Pareto Charts are used to drive continuous improvement in the Product and Administrative Quality arenas. We review these metrics in our monthly Business Unit & Manufacturing Operations Reviews.

Section 10 – New Product Development

onsemi uses a phase/gate approach (aka Advanced Product Quality Planning – APQP) for New Product Development, as shown below. The major project milestones and phase-gates provide points where the project undergoes a formal review of all deliverables required for that phase. The NPD process includes the following design and development phases (gates):

- Concept (Concept Commit gate),
- Plan (Plan Commit gate),
- Develop (Develop Complete gate),
- Qualify (Qualify Complete gate),
- Launch (Launch Complete gate).

The Sustain and Retire are phases of the Product Life Cycle but extend beyond and are not part of NPD.

The **Concept Phase** is the starting point for new product ideas (proposals) and their associated business opportunity. During the Concept Phase, the primary activity is to analyze the NPD opportunity from both a technical feasibility and a business viability perspective.

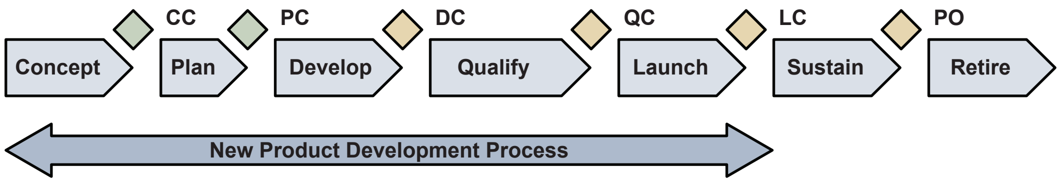
The **Plan Phase** validates the assumptions made during the Concept Phase on scope, schedule, and cost. Identified discrepancies with customer expectations must be resolved by the end of this phase. This phase includes creating the Project Plan, the Verification and Validation (Qualification) plans, and the Product Technical Specification. For automotive projects, a Design Failure-Mode-Effects-Analysis (DFMEA) is initiated according to the AIAG standard to identify, document, assess, and manage the project risks. Additionally, for automotive, the Production Part Approval Process (PPAP) level is determined.

The **Develop Phase** encapsulates the execution of the main design and development activities for the new product per the product requirements and the project plan, including silicon design, layout, test, hardware or software design and development, or package development as identified in the project plan. Design and development verification and validations are performed following planned arrangements to ensure that the design and development outputs meet the design and development input requirements.

During the **Qualify Phase**, the design and development validation gets completed, including Reliability tests (see section 3), product approval, and ensuring product readiness for Manufacturing, Supply Chain, Sales, and Marketing. PPAP is completed in this phase for automotive products.

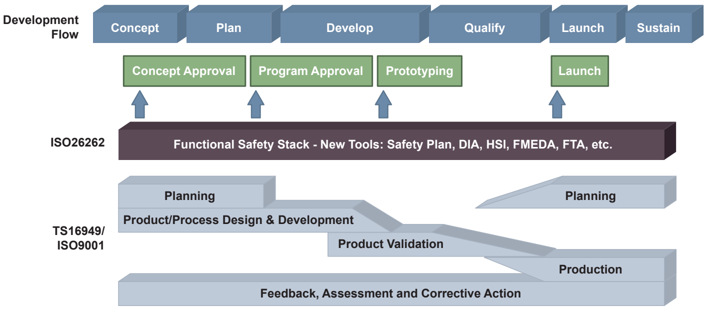
The **Launch Phase** demonstrates that the product can be delivered in high volume with acceptable conditions for both **onsemi** (cost and manufacturability) and the customer (quality, reliability, and volume).

Product Discontinuance occurs in the **Retire Phase** of the product life cycle; the **Customer Process Change Notification** section above describes the **Product Discontinuance** notice procedure.



Section 11 – ISO 26262 Automotive Functional Safety

ISO 26262 is an adaptation of IEC 61508 for the automotive industry. Since its inception in November 2011, ISO 26262 has become state of the art and is now widely used to develop automotive safety-related integrated circuits. The second version of the standard released in 2018 for which **onsemi** was an active member contains many improvements, including a dedicated part for the Semiconductor industry.

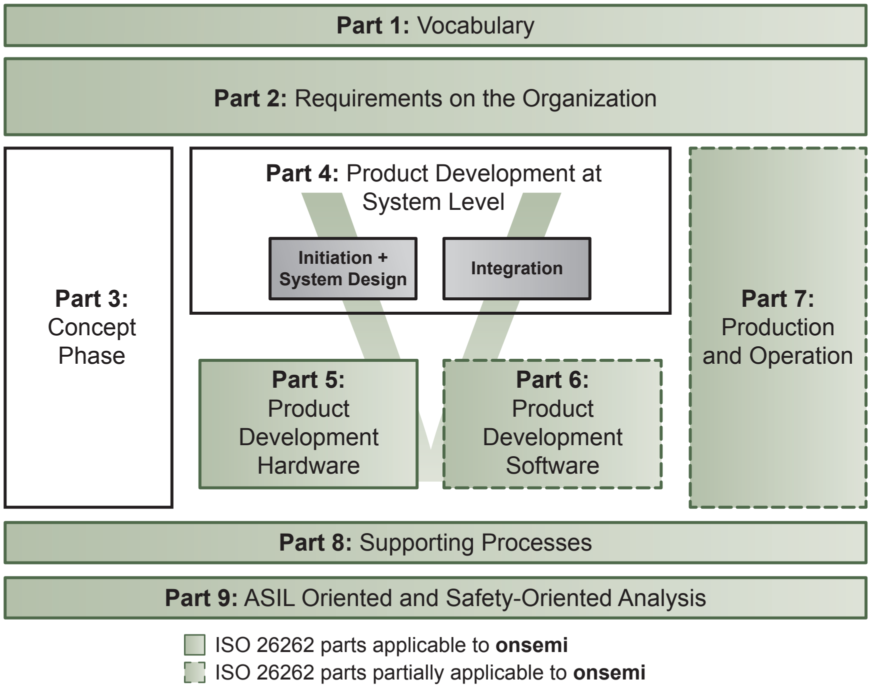


onsemi created a specific organization to enhance its safety culture and integrate the ISO 26262 requirements into our existing Quality Management System (QMS) based on IATF 16949. Consequently, the company added Safety activities into each development phase defined in the NPD process. Part 5 (Product Development Hardware), Part 8 (Supporting Processes), and Part 9 (ASIL oriented and safety-oriented analysis) define the main requirements brought by ISO 26262 compared to the regular QMS. They describe the hardware product development flow and the tools needed to develop safe products. These requirements, for example, are related to the specification of the hardware safety requirements, the definition of the safety mechanisms, and the execution of the safety analysis [e.g., Failure Modes Effects and Diagnostic Analysis (MEDA), Fault Tree Analysis (FTA)]. The creation of a dedicated team supports functional safety development across the company.

In addition to integrating safety activities into our NPD process, we can trace a functional safety product from each step of its lifecycle from the concept phase until the final deployment in the field. Thus, **onsemi** can immediately identify safety-related parts among field returns.

Another vital requirement from ISO 26262 is to perform an independent assessment for each functional safety development. To meet this requirement, **onsemi** established a dedicated organization fully independent from the business units and provided a level of independence up to I3 (i.e., ASIL D).

onsemi continues to be an active member of the ISO 26262 working group, and our experience contributes to many other functional safety initiatives such as the IEEE P2851 project.



Section 12 – Storage and Preservation

onsemi adheres to the proper storage and preservation of semiconductors to prevent damage or deterioration and ensure on-time delivery of superior quality products to our valued customers. The standard storage and preservation guidelines are listed below and are followed by all **onsemi** manufacturing sites, including subcontractors and distribution centers.

We monitor the storage duration throughout our Supply Chain and within Finance information systems. They are tracked monthly to drive on-time delivery.

Table 3. Storage and Preservation*

onsemi Product	Storage Condition	Storage Life
Finished Wafer, Probe Wafer	Temperature 18-28°C Humidity 30-65% RH	36 months after final wafer fab finish date
Die in Tray or Pocket Tape	Temperature 18-28°C, Humidity 30-65% RH	24 months after die singulation/sawing date
Die in Surf Tape, Wafers in Foil/Tape	Temperature 18-28°C, N2 storage or in vacuum moisture bag with desiccant and humidity card	3 months after tape date After 3 months quality of products needs to be validated
Finished/ Packaged Goods in tray. Tube or sealed in dry bag (MSL2 rated and above)	Temperature 8-30°C Humidity 30-70% RH	24 months after assembly date
Finished/packaged Goods in Tray, Tube or sealed in dry bag (MSL1 rated)	Temperature 8-30°C Humidity 30-70% RH	24 months after assembly date
Finished/Packaged Ceramics in Tray or Tube	Temperature 8-30°C Humidity 30-70% RH	36 months after assembly date

* Regular temperature monitoring is needed to ensure no sudden changes in temperature can result in moisture condensation during storage.

Section 13 – Product ID and Traceability

onsemi identifies products throughout every step of the product manufacturing process, and where traceability is a requirement, controls the unique identification of the product, and maintains records per our corporate record procedures.

All Products manufactured by **onsemi** are assigned a unique lot number by the manufacturing execution system (MES) in each factory. As the MES transacts the lots, they are reported into the **onsemi** corporate inventory management system (IRAB). These transactions are managed by interfaces designed to ensure the MES and inventory systems are synchronized as lots move between factories and distribution centers to ensure our inventory management system is the central repository for all inventory data.

Lot Genealogy (Lot G) is one of the supplemental systems built upon IRAB with the specific goal of providing lot number traceability. As lots are processed throughout our global supply chain, the Lot G data are updated so that the history of an existing lot number can be traced back to its factory of origin. The historical parametric data associated with the production of a lot is archived in the MES for the factory that produces the lot in compliance with the corporate data retention policy.

Other methods can be used to research local lot information or to reconstruct a sequence of events such as:

- Customer incident data from ONIT
- MES data searches
- Hyperion reports
- Web Lot G
- Shop orders
- TRAK inventory search

Manufacturing operations ensure that a system can trace a product from the factory order number back to the manufacturing lot number and from the manufacturing lot numbers back to incoming material batch numbers to ensure that all manufacturing lots using material from the same material batch may be traced and located.

If product identification is lost or the product is mixed, it Is considered non-conforming and dispositioned per 12MRM70603A. Manufacturing is capable of identifying and tracing lots and bill of material items.

Historical Data

Each MES maintains its own archiving procedures for historical data, which complies with the corporate data retention policy.

Section 14 – Record Retention Policy

onsemi complies with the record retention requirements of local country/government statutes and other business needs. Records are retained in strict compliance with an established record retention policy and demonstrate compliance to regulatory, certification, and agreed customer requirements.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS
Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

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