FDZ192NZ

Power MOSFET, N-Channel, Trench®, 1.5 V Specified Thin WLCSP

20 V, 5.3 A, 39 mΩ

General Description

Designed on advanced 1.5 V PowerTrench® process with state of the art "fine pitch" WLCSP packaging process, the FDZ192NZ minimizes both PCB space and $r_{DS(on)}$. This advanced WLCSP MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, ultra−low profile packaging, low gate charge, and low $r_{DS(on)}$.

Features

- Max $r_{DS(on)}$ = 39 mΩ at V_{GS} = 4.5 V, I_D = 2.0 A
- Max $r_{DS(on)}$ = 43 mΩ at V_{GS} = 2.5 V, I_D = 2.0 A
- Max $r_{DS(on)}$ = 49 mΩ at V_{GS} = 1.8 V, I_D = 1.0 A
- Max $r_{DS(on)}$ = 55 mΩ at V_{GS} = 1.5 V, I_D = 1.0 A
- Occupies only 1.5 mm^2 of PCB Area. Less than 50% of the Area of 2 x 2 BGA
- Ultra−thin Package: Less than 0.65 mm Height when Mounted to PCB
- HBM ESD Protection Level > 2200 V (Note 3)
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Battery Management
- Load Switch
- Battery Protection

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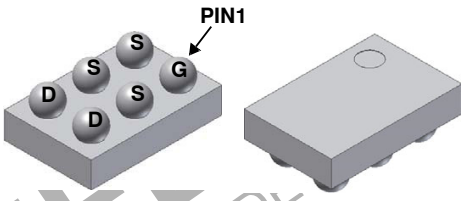
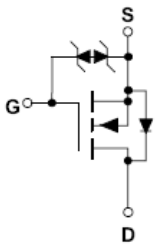
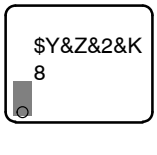


WLCSP6 1.5x1x0.6
CASE 567PW

SCHEMATIC



MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&2	= Numeric Date Code
&K	= Lot Code
8	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Part Number	Device Marking	Package	Shipping†
FDZ192NZ	8	WLCSP6 1.5x1x0.6 (Pb-Free / Halogen Free)	5000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	20	V
V_{GS}	Gate to Source Voltage	±8	V
I_D	Drain Current Continuous, T_A = 25°C (Note 1a)	5.3	A
	Drain Current Pulsed	15	
P_D	Power Dissipation, T_A = 25°C (Note 1a)	1.9	W
	Power Dissipation, T_A = 25°C (Note 1b)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	65	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	133	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C		10		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8 V, V_{DS} = 0 V			±10	μA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	0.4	0.7	1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C		−3		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 4.5 V, I_D = 2.0 A		26	39	mΩ
		V_{GS} = 2.5 V, I_D = 2.0 A		29	43	
		V_{GS} = 1.8 V, I_D = 1.0 A		33	49	
		V_{GS} = 1.5 V, I_D = 1.0 A		38	55	
		V_{GS} = 4.5 V, I_D = 2.0 A, T_J = 125°C		31	47	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 5.3 A		36		s
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz		915	1220	pF
C_{oss}	Output Capacitance			145	195	pF
C_{rss}	Reverse Transfer Capacitance			100	150	pF

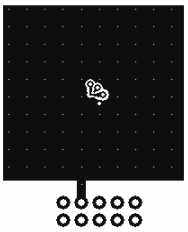
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
Switching Characteristics							
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 10 V, I_D = 5.3 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω			6.5	13	ns
t_r	Rise Time				4	10	ns
$t_{d(off)}$	Turn−Off Delay Time				50	80	ns
t_f	Fall Time				20	32	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 4.5 V	V_{DD} = 10 V, I_D = 5.3 A		12	17	nC
Q_{gs}	Gate to Source Charge				1.3		nC
Q_{gd}	Gate to Drain “Miller” Charge				2.3		nC
Drain−Source Diode Characteristics							
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.1 A (Note 2)			0.6	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 5.3 A, di/dt = 100 A/μs			18	32	ns
Q_{rr}	Reverse Recovery Charge				4.6	10	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.



a.) 65°C/W when mounted on a 1 in^2 pad of 2 oz copper

b.) 133°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. The diode connected between the gate and source servers only as protection against ESD. No gate overvoltage rating is implied.

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

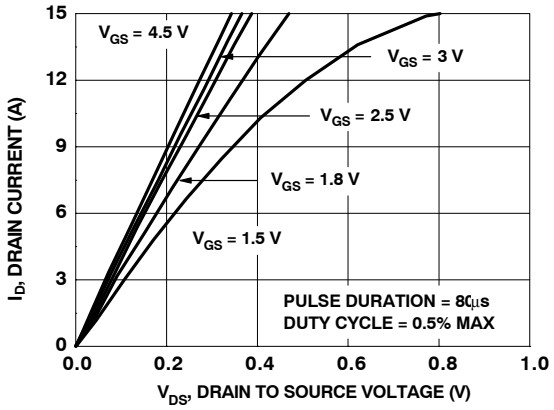


Figure 1. On−Region Characteristics

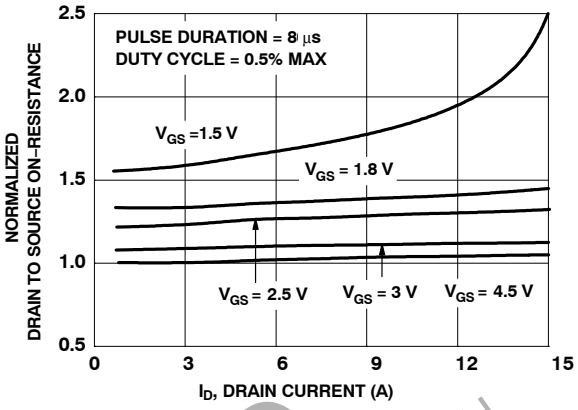


Figure 2. Normalized On−Resistance vs Drain Current and Gate Voltage

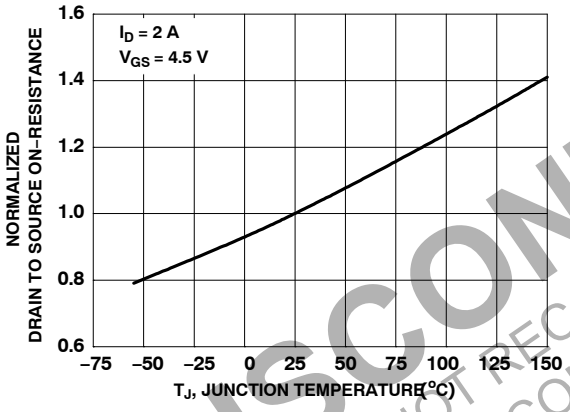


Figure 3. Normalized On−Resistance vs Junction Temperature

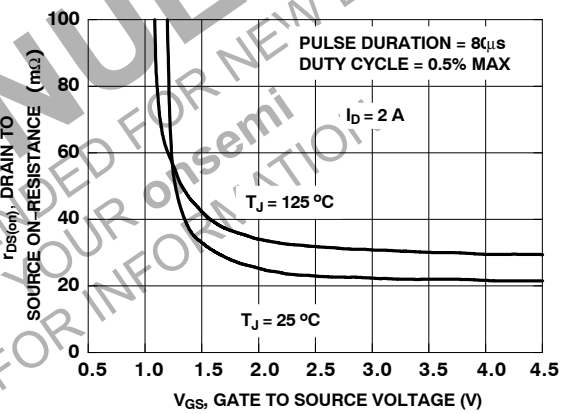


Figure 4. On−Resistance vs Gate to Source Voltage

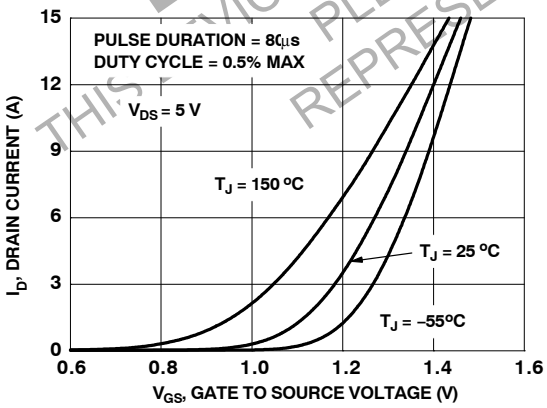


Figure 5. Transfer Characteristics

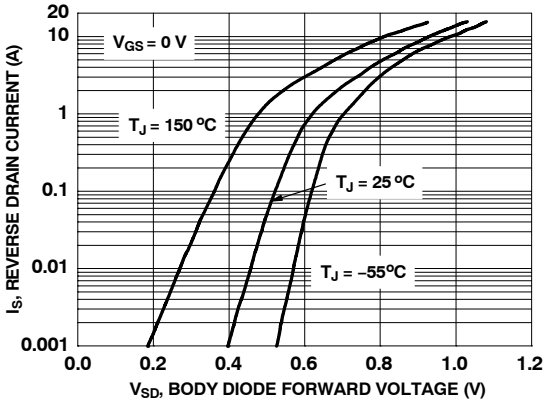


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

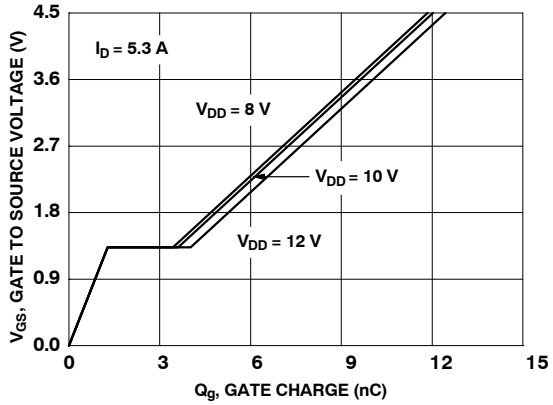


Figure 7. Gate Charge Characteristics

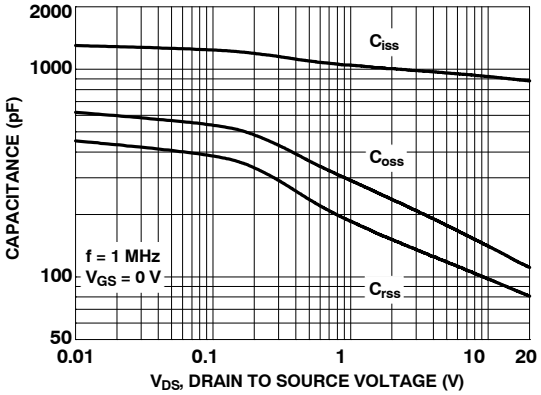


Figure 8. Capacitance vs Drain to Source Voltage

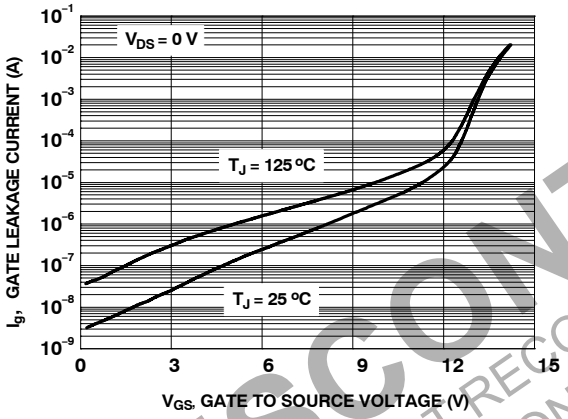


Figure 9. Gate Leakage Current vs Gate to Source Voltage

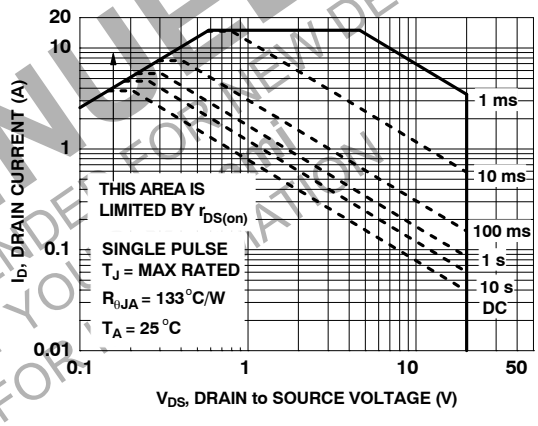


Figure 10. Forward Bias Safe Operating Area

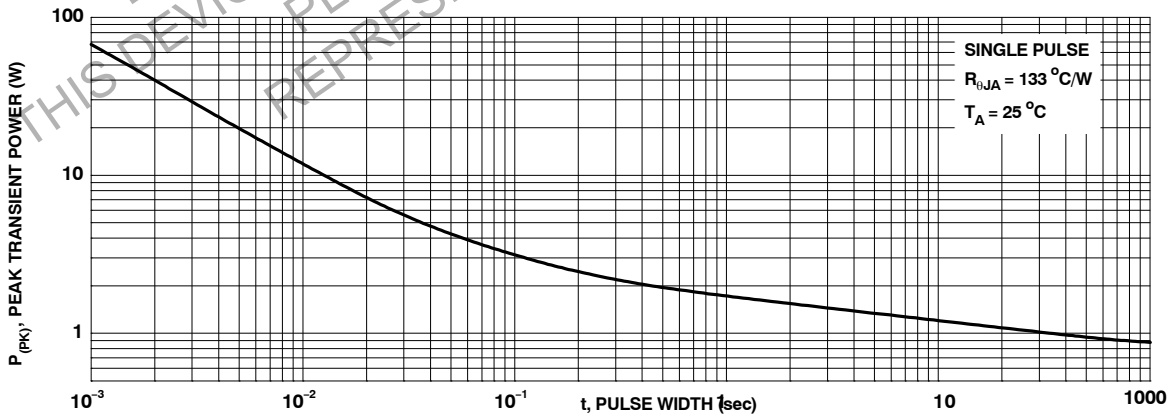


Figure 11. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

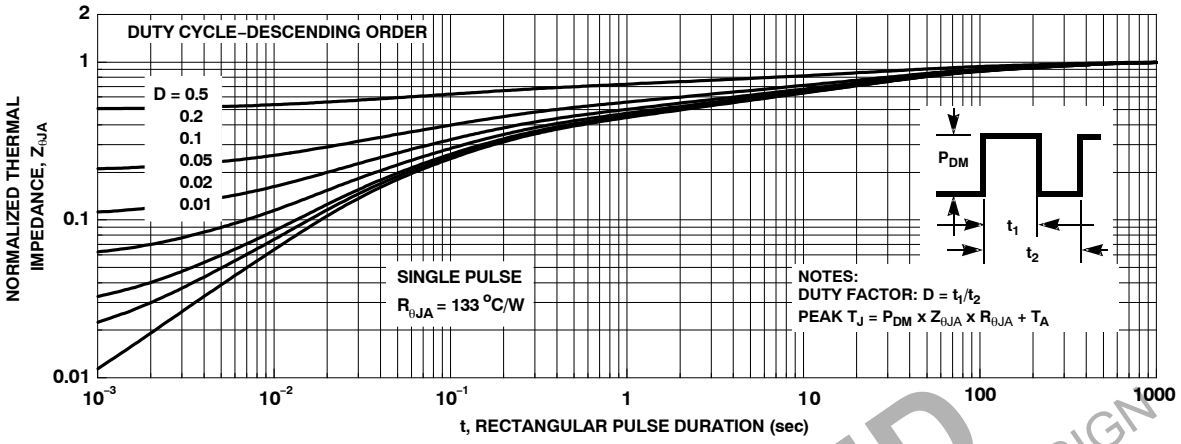


Figure 12. Junction−to−Ambient Transient Thermal Response Curve

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

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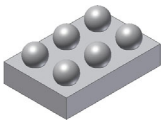

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CASE 567PW
ISSUE A

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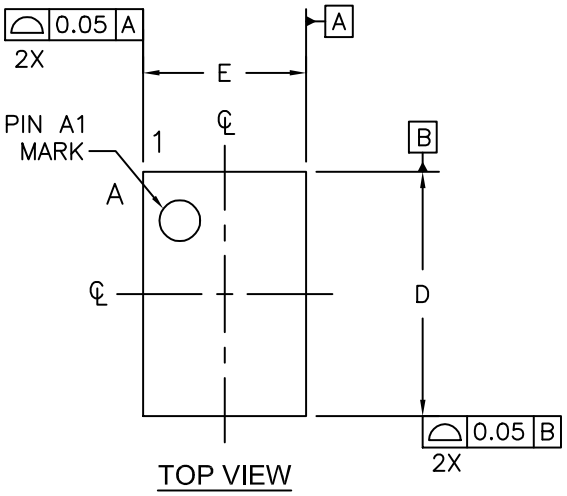
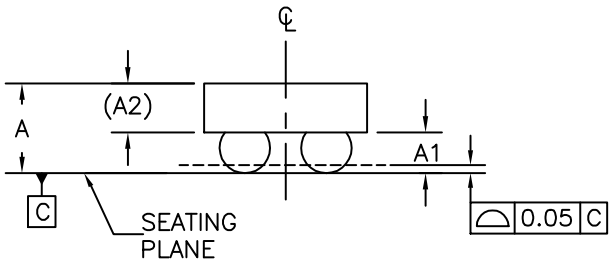
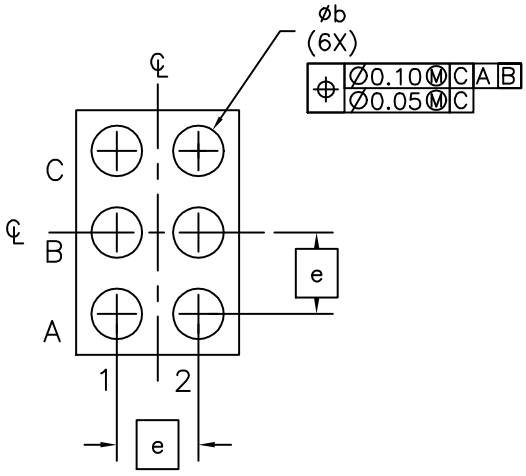


TOP VIEW



FRONT VIEW

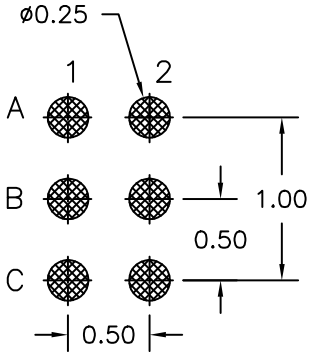


BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) NO JEDEC REGISTRATION REFERENCE AS OF OCTOBER 2005.
C) DRAWING CONFORMS TO ASME Y14.5M-2009

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	-	-	0.60
A1	0.22	0.25	0.28
A2	0.30 REF		
b	0.24	0.31	0.39
D	1.45	1.50	1.55
E	0.95	1.00	1.05
e	0.50 BSC		



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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