

# MOSFET – N-Channel, POWERTRENCH®

100 V, 3.2 A, 108 mΩ

## FDT86106LZ

### General Description

This N-Channel logic Level MOSFETs are produced using onsemi's advanced POWERTRENCH process that has been special tailored to minimize the on-state resistance and yet maintain superior switching performance. G-S zener has been added to enhance ESD voltage level.

### Features

- Max  $r_{DS(on)}$  = 108 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 3.2\text{ A}$
- Max  $r_{DS(on)}$  = 153 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 2.7\text{ A}$
- High Performance Trench Technology for Extremely Low  $r_{DS(on)}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- HBM ESD Protection Level > 3 kV Typical (Note 4)
- 100% UIL Tested
- This Device is Pb-Free, Halide Free and is RoHS Compliant

### Applications

- DC – DC Conversion

### MOSFET MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

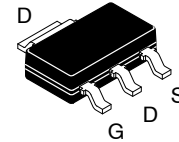
Symbol	Parameter	Rated	Unit	
$V_{DS}$	Drain-Source Voltage	100	V	
$V_{GS}$	Gate-Source Voltage	±20	V	
$I_D$	Drain Current	- Continuous $T_A = 25^\circ\text{C}$ (Note 1a.)	3.2	A
		- Pulsed	12	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	12	mJ	
$P_D$	Power Dissipation	$T_A = 25^\circ\text{C}$ (Note 1a.)	2.2	W
		$T_A = 25^\circ\text{C}$ (Note 1b.)	1.0	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

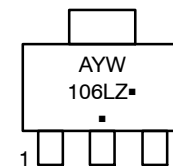
Symbol	Parameter	Rated	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	12	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a.)	55	°C/W

$V_{DSS}$	$R_{DS(ON)}$ MAX	$I_D$ MAX
100 V	108 mΩ @ 10 V	3.2 A
	153 mΩ @ 4.5 V	



SOT-223  
CASE 318H

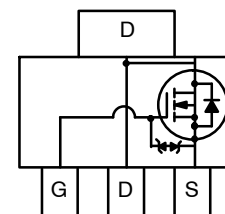
### MARKING DIAGRAM



- A = Specific Device Code
- Y = Date Code
- W = Work Week
- 106LZ = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

### PINOUT



### ORDERING INFORMATION

Device	Package	Shipping†
FDT86106LZ	106LZ	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

# FDT86106LZ

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V	100	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	–	71	–	mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V	–	–	1	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V	–	–	±10	μA

## ON CHARACTERISTICS (Note 2)

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	1.0	1.5	2.2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25°C	–	–5	–	mV/°C
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.2 A V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 2.7 A, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.2 A, T <sub>J</sub> = 125°C	–	80 100 140	108 153 189	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 3.2 A	–	8	–	S

## DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V, f = 1 MHz	–	234	315	pF
C <sub>oss</sub>	Output Capacitance		–	46	65	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		–	3.1	5	pF

## SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 3.2 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω	–	3.8	10	ns
t <sub>r</sub>	Rise Time		–	1.3	10	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		–	10	20	ns
t <sub>f</sub>	Fall Time		–	1.5	10	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V, V <sub>DD</sub> = 50 V, I <sub>D</sub> = 3.2 A	–	4.3	7	nC
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to 5 V, V <sub>DD</sub> = 50 V, I <sub>D</sub> = 3.2 A	–	2.4	4	nC
Q <sub>gs</sub>	Gate to Source Gate Charge	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 3.2 A	–	0.7	–	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge		–	0.9	–	nC

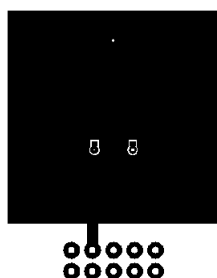
## DRAIN-SOURCE DIODE CHARACTERISTICS

V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 3.2 A (Note 2) V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1 A (Note 2)	–	0.86 0.77	1.3 1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 3.2 A, di/dt = 100 A/s	–	31	49	ns
Q <sub>rr</sub>	Reverse Recovery Charge		–	21	34	nC

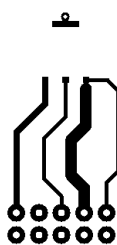
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

### NOTES:

- R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design while R<sub>θJA</sub> is determined by the user's board design.



a. 55°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b. 118°C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.
- Starting T<sub>J</sub> = 25°C, L = 1 mH, I<sub>AS</sub> = 5 A, V<sub>DD</sub> = 90 V, V<sub>GS</sub> = 10 V.
- The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

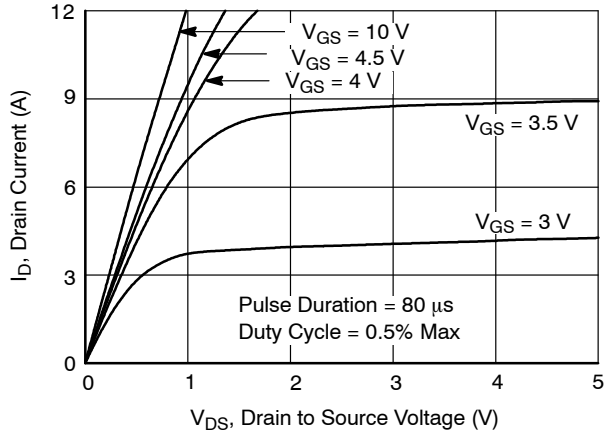


Figure 1. On-Region Characteristics

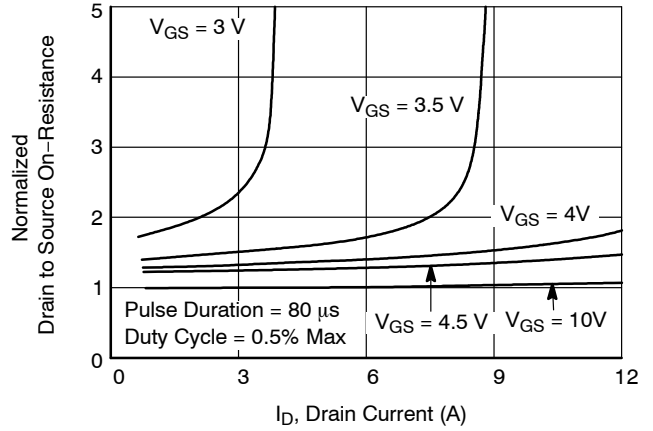


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

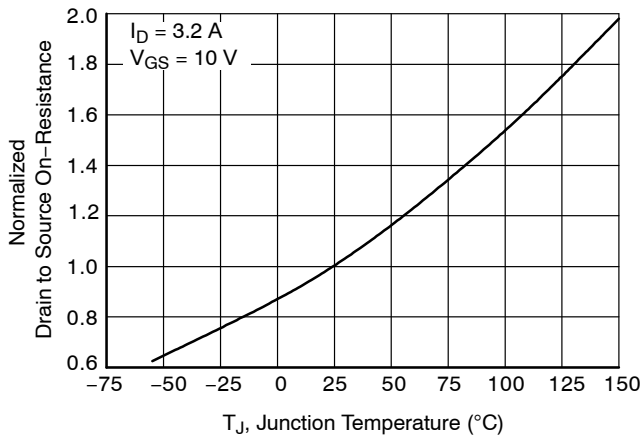


Figure 3. Normalized On-Resistance vs. Junction Temperature

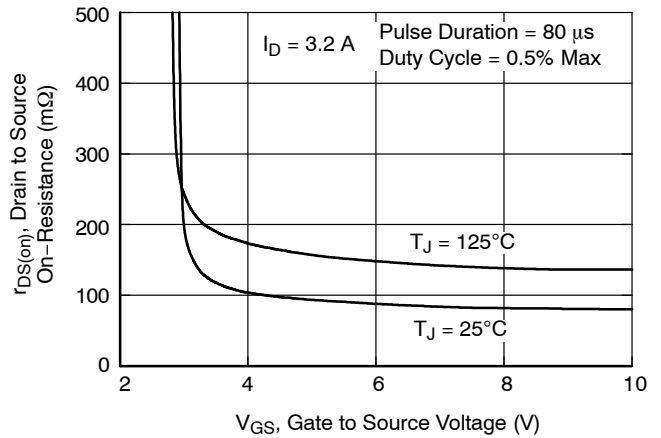


Figure 4. On-Resistance vs. Gate to Source Voltage

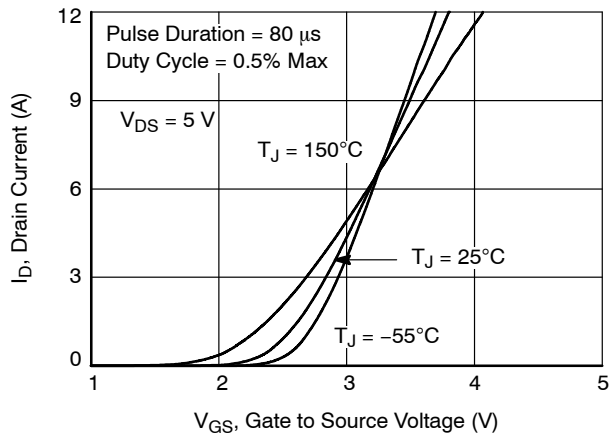


Figure 5. Transfer Characteristics

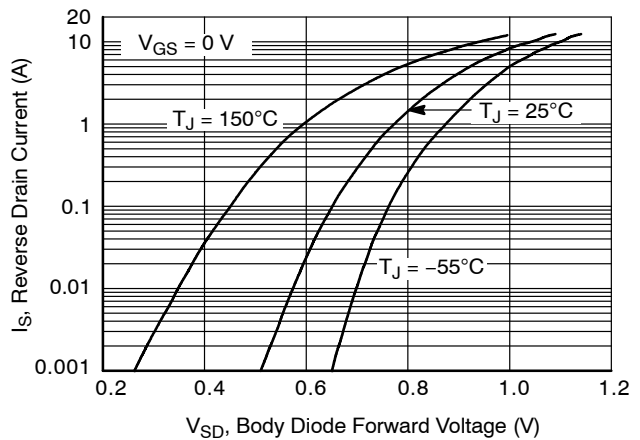


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)

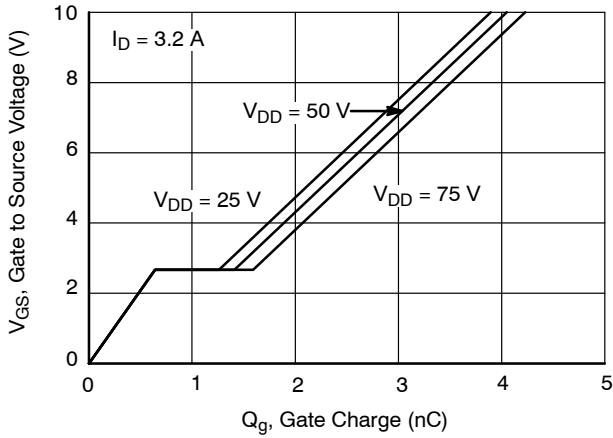


Figure 7. Gate Charge Characteristics

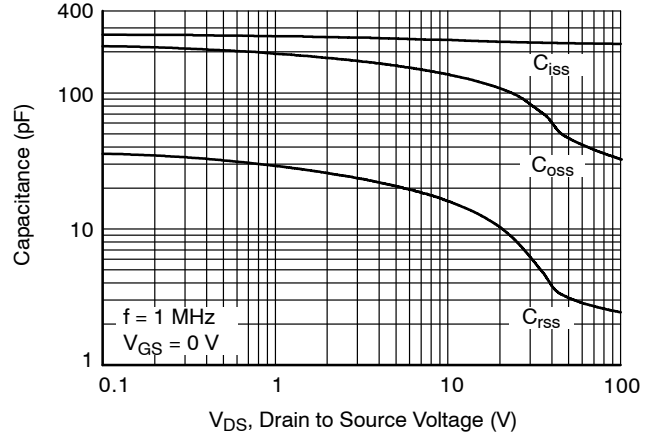


Figure 8. Capacitance vs. Drain to Source Voltage

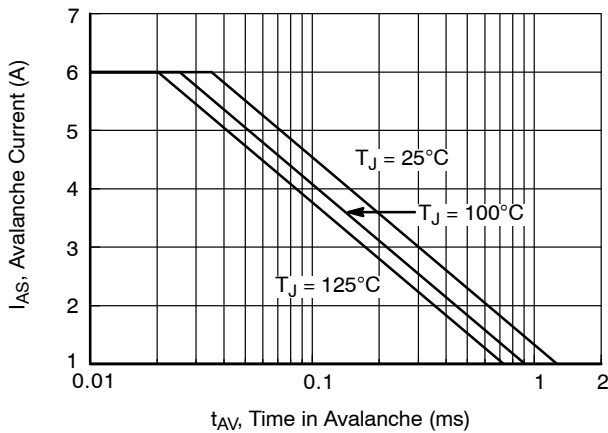


Figure 9. Unclamped Inductive Switching Capability

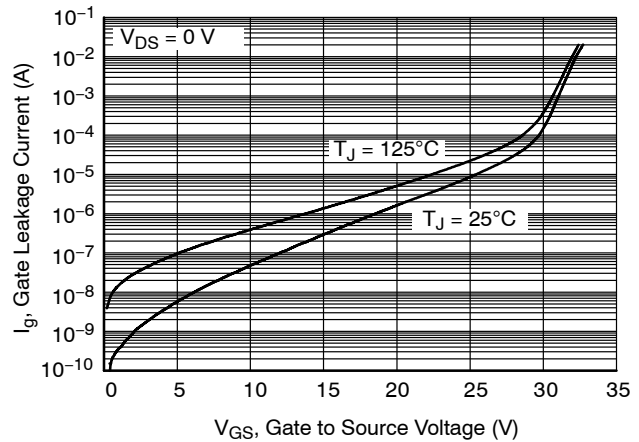


Figure 10. Gate Leakage Current vs. Gate to Source Voltage

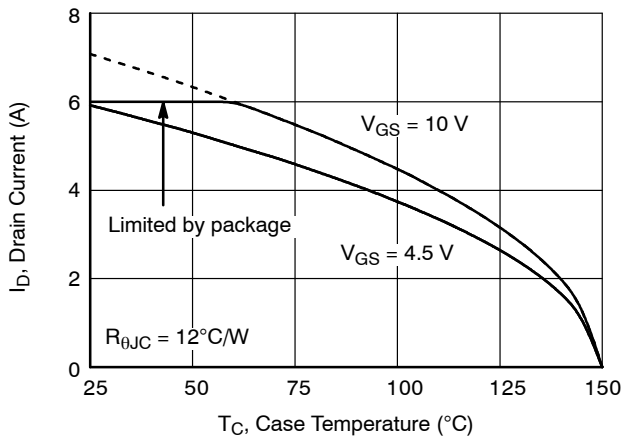


Figure 11. Maximum Continuous Drain Current vs. Case temperature

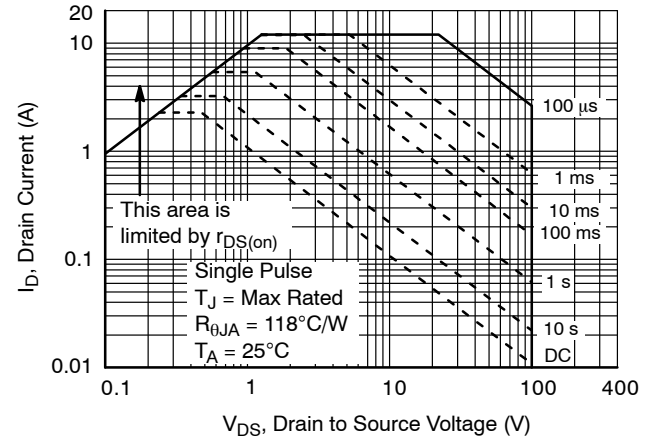


Figure 12. Forward Bias Safe Operating Area

# FDT86106LZ

## TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

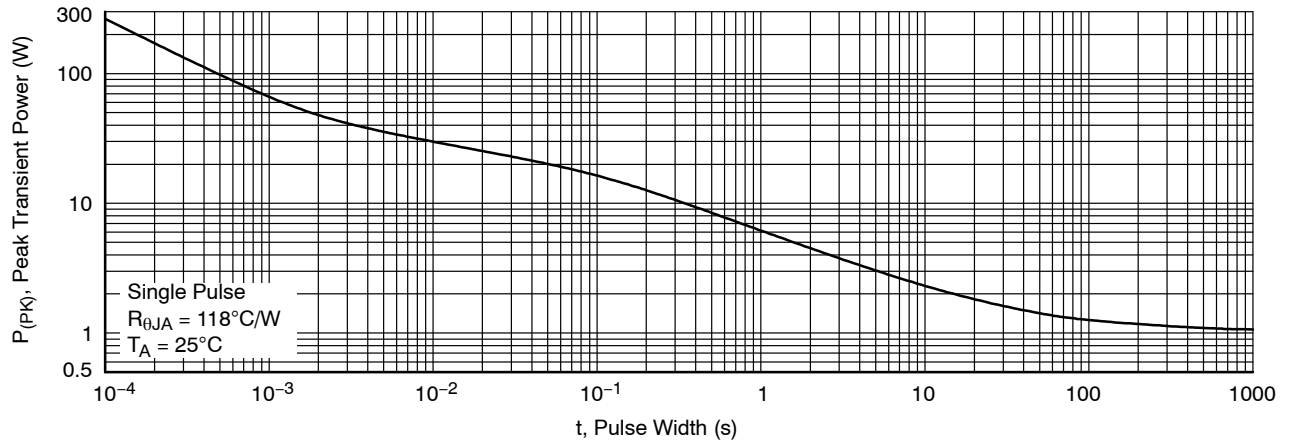


Figure 13. Single Pulse Maximum Power Dissipation

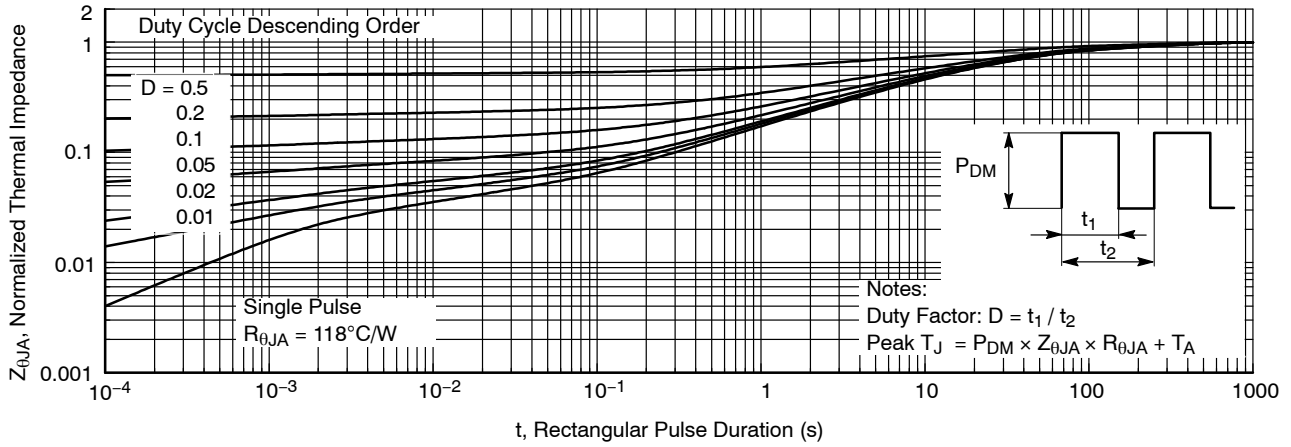
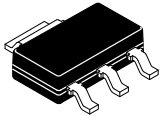


Figure 14. Junction-to-Ambient Transient Thermal Response Curve



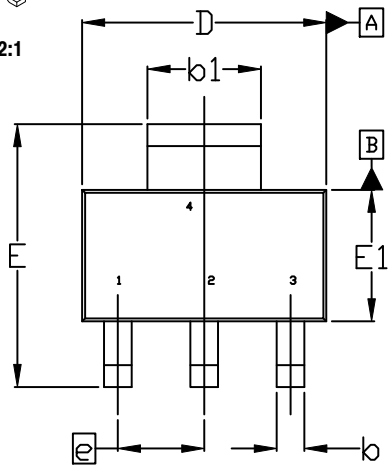
SCALE 2:1

SOT-223  
CASE 318H  
ISSUE B

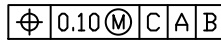
DATE 13 MAY 2020

NOTES:

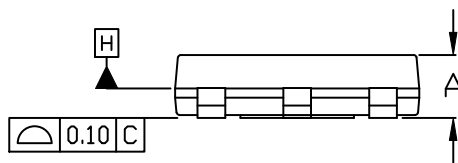
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E1 ARE DETERMINED AT DATUM H. DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. SHALL NOT EXCEED 0.23mm PER SIDE.
4. LEAD DIMENSIONS b AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.08mm PER SIDE.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.



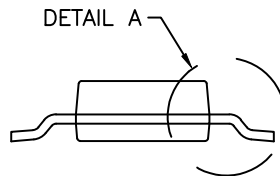
TOP VIEW



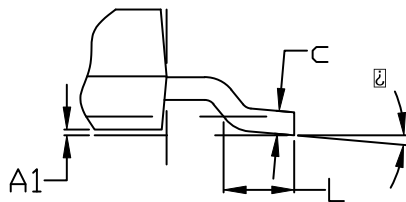
NOTE 7



SIDE VIEW

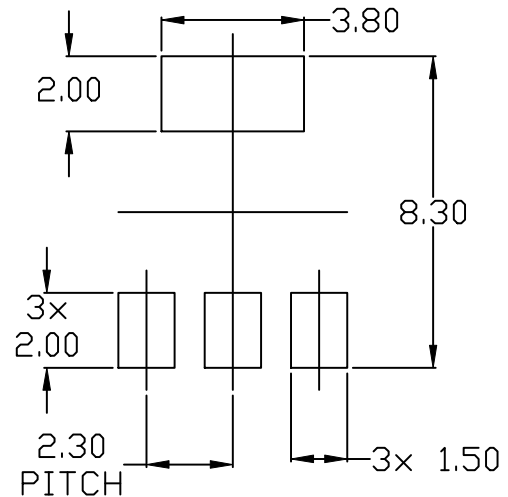


END VIEW



DETAIL A

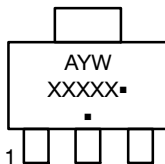
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.80
A1	0.02	0.06	0.11
b	0.60	0.74	0.88
b1	2.90	3.00	3.10
c	0.24	---	0.35
D	6.30	6.50	6.70
E	6.70	7.00	7.30
E1	3.30	3.50	3.70
e	2.30 BSC		
L	0.25	---	---
$\text{C}$	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

\* For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SLDERRM/D.

GENERIC MARKING DIAGRAM\*



- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98ASH70634A	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOT-223	PAGE 1 OF 1

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

---

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)