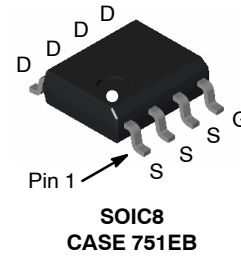


MOSFET – N-Channel, POWERTRENCH®

30 V, 15 A, 7.0 mΩ

FDS8817NZ, FDS8817NZ-G



General Description

This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process that has been especially tailored to minimize the on-state resistance.

This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

Features

- Max $r_{DS(on)}$ = 7 mΩ at $V_{GS} = 10$ V, $I_D = 15$ A
- Max $r_{DS(on)}$ = 10 mΩ at $V_{GS} = 4.5$ V, $I_D = 12.6$ A
- HBM ESD Protection Level of 3.8 kV Typical*
- High Performance Trench Technology for Extremely Low $r_{DS(on)}$
- High Power and Current Handling Capability
- These Devices are Pb-Free and are RoHS Compliant

Specifications

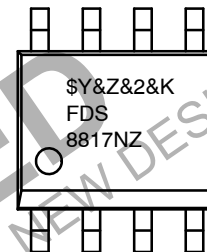
MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current	Continuous (Note 1a)	15
		Pulsed	60
E_{AS}	Single Pulse Avalanche Energy (Note 2)	181	mJ
P_D	Power Dissipation	(Note 1a)	2.5
		(Note 1b)	1.0
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

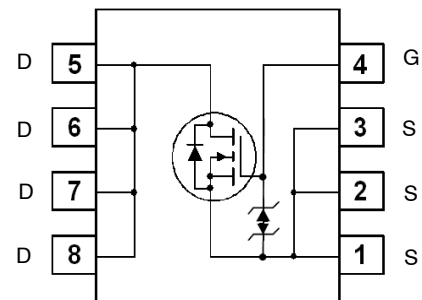
*The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

MARKING DIAGRAM



\$Y = onsemi Logo
&Z = Assembly Plant Code
&2 = Numeric Date Code
&k = Lot Code
FDS8817NZ = Specific Device Code

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	25	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	125	

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a. 50°C/W when mounted on a 1 in² pad of 2 oz copper



b. 125°C/W when mounted on a minimum pad

2. Starting $T_J = 25^\circ\text{C}$; $L = 3\text{ mH}$, $I_{AS} = 11\text{ A}$, $V_{DD} = 30\text{ V}$, $V_{GS} = 10\text{ V}$.

DISCONTINUED
 THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
 PLEASE CONTACT YOUR onsemi
 REPRESENTATIVE FOR INFORMATION

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}$, $V_{GS} = 0 \text{ V}$	30			V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C		20		$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V}$, $V_{GS} = 0 \text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0 \text{ V}$			± 10	μA

ON CHARACTERISTICS (Note 3)

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250 \mu\text{A}$	1	1.8	3	V
$\Delta V_{GS(th)} / \Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C		-6		$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}$, $I_D = 15 \text{ A}$		5.4	7	$\text{m}\Omega$
		$V_{GS} = 4.5 \text{ V}$, $I_D = 12.6 \text{ A}$		7.0	10	
		$V_{GS} = 10 \text{ V}$, $I_D = 15 \text{ A}$, $T_J = 125^\circ\text{C}$		7.5	11	
g_{FS}	Forward Transconductance	$V_{DS} = 5 \text{ V}$, $I_D = 15 \text{ A}$		54		S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 15 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$		1805	2400	pF
C_{oss}	Output Capacitance			335	445	
C_{rss}	Reverse Transfer Capacitance			200	300	
R_g	Gate Resistance	$f = 1 \text{ MHz}$		1.4		Ω

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15 \text{ V}$, $I_D = 15 \text{ A}$, $V_{GS} = 10 \text{ V}$, $R_{GEN} = 6 \Omega$		11	22	ns
t_r	Rise Time			13	26	
$t_{d(off)}$	Turn-Off Delay Time			25	40	
t_f	Fall Time			7	14	
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ V}$ to 10 V , $V_{DD} = 15 \text{ V}$, $I_D = 15 \text{ A}$		32	45	nC
		$V_{GS} = 0 \text{ V}$ to 5 V , $V_{DD} = 15 \text{ V}$, $I_D = 15 \text{ A}$		17	24	
Q_{gs}	Gate to Source Charge	$V_{DD} = 15 \text{ V}$, $I_D = 15 \text{ A}$		6		nC
Q_{gd}	Gate to Drain "Miller" Charge			7		nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}$, $I_S = 2.1 \text{ A}$ (Note 3)		0.8	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 15 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$		24	36	ns
Q_{rr}	Reverse Recovery Charge				15	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

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TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

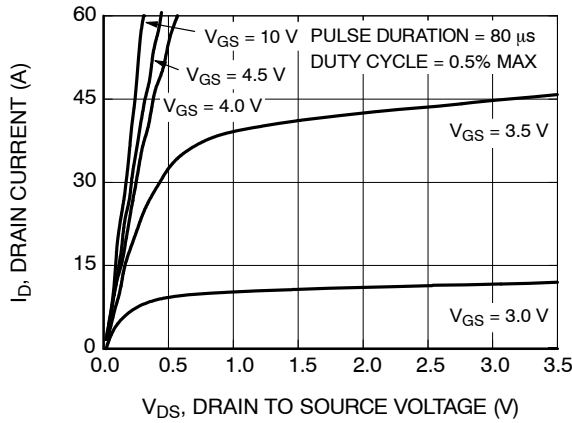


Figure 1. On Region Characteristics

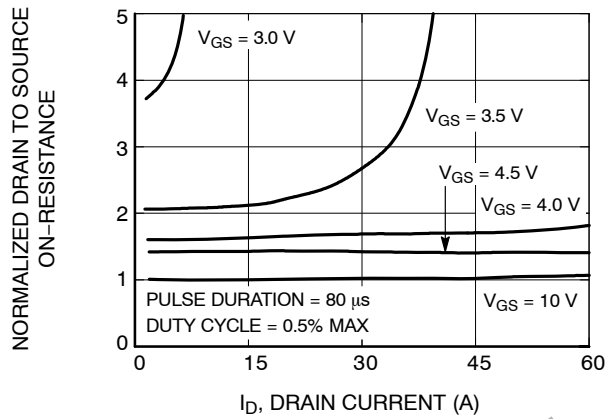


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

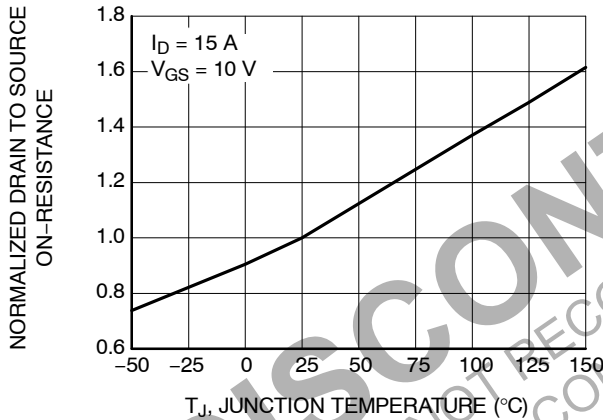


Figure 3. Normalized On Resistance vs. Junction Temperature

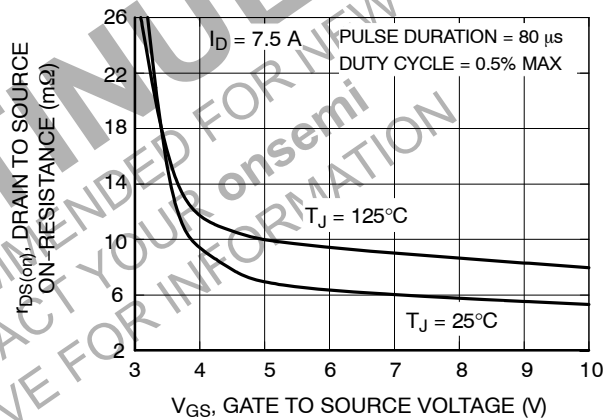


Figure 4. On-Resistance vs. Gate to Source Voltage

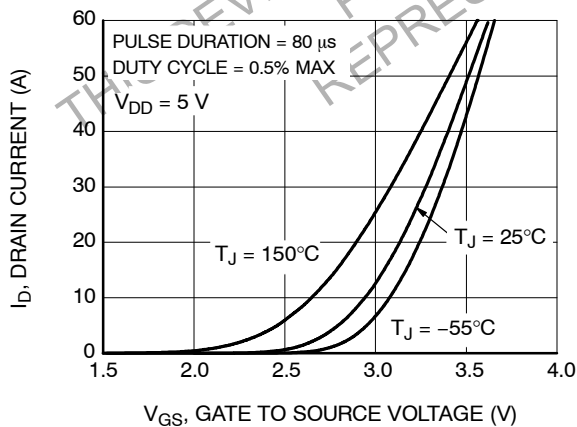


Figure 5. Transfer Characteristics

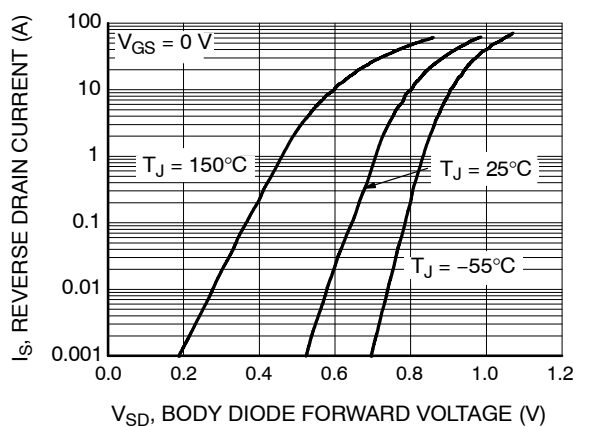


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

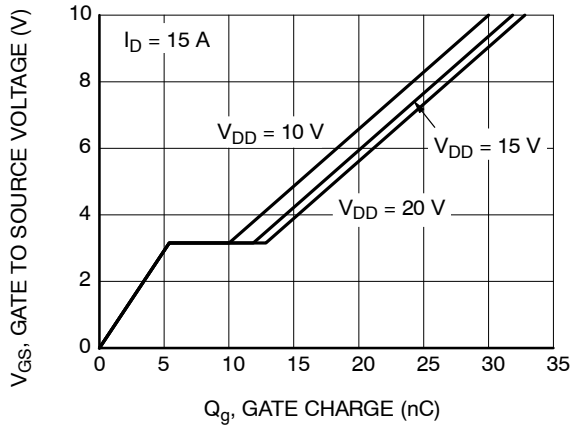


Figure 7. Gate Charge Characteristics

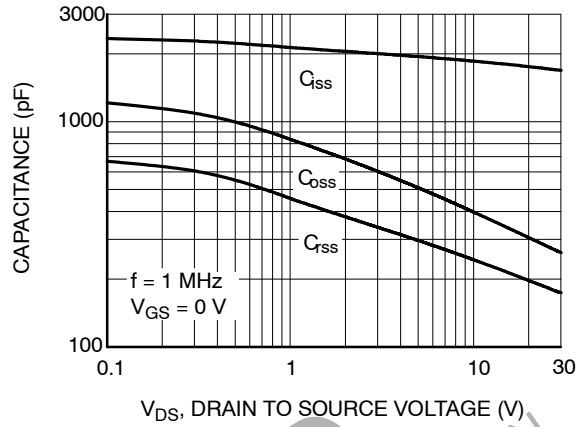


Figure 8. Capacitance vs. Drain to Source Voltage

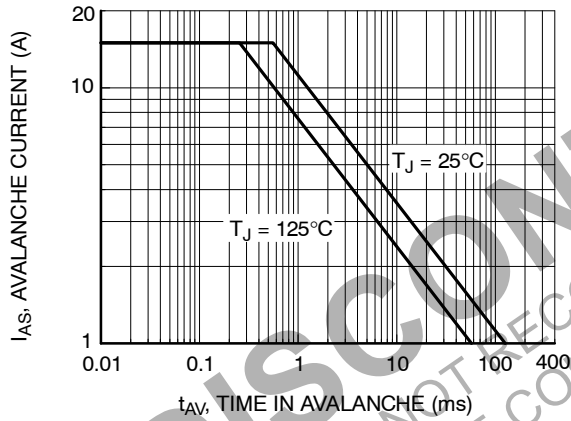


Figure 9. Unclamped Inductive Switching Capability

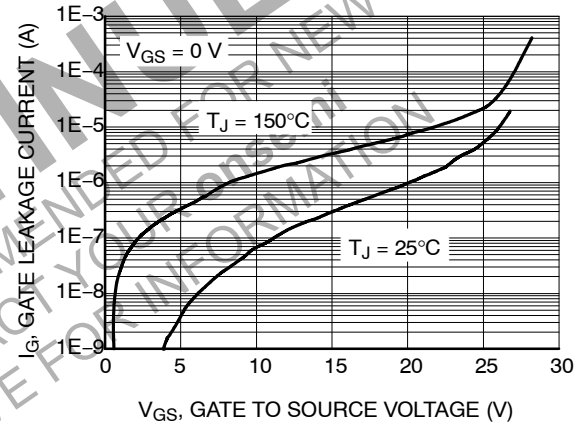


Figure 10. Gate Leakage Current vs. Gate to Source Voltage

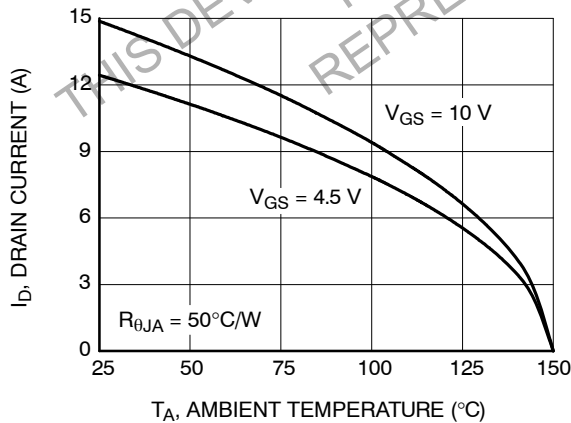


Figure 11. Maximum Continuous Drain Current vs. Ambient Temperature

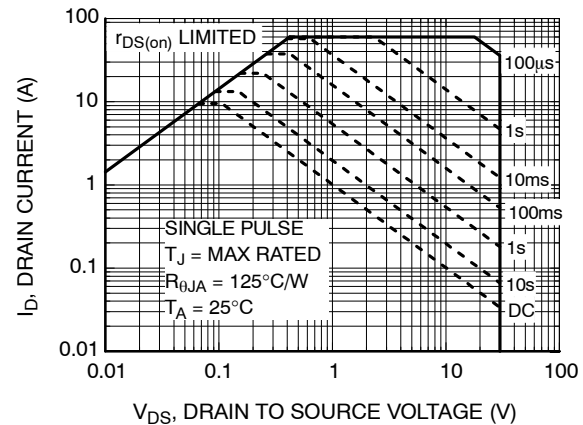


Figure 12. Forward Bias Safe Operating Area

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TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

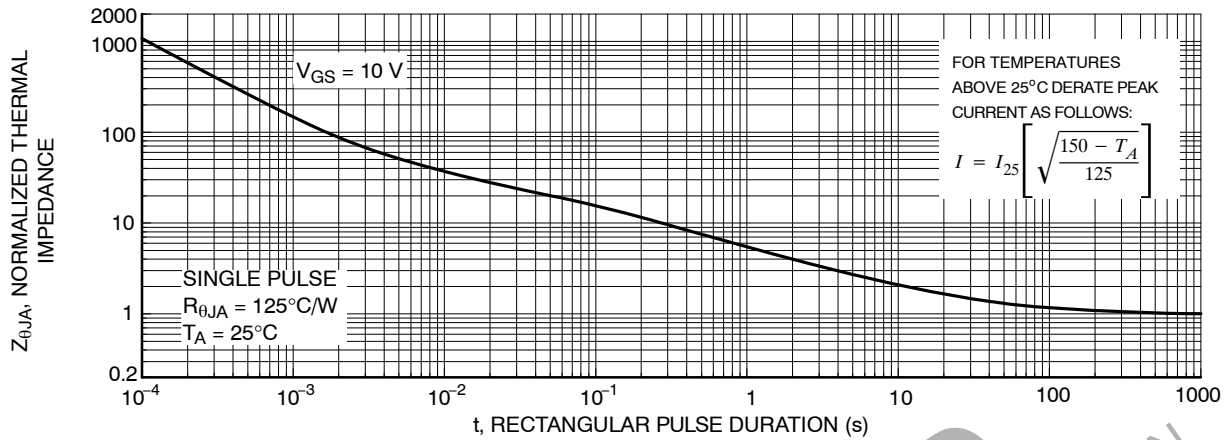


Figure 13. Single Pulse Maximum Power Dissipation

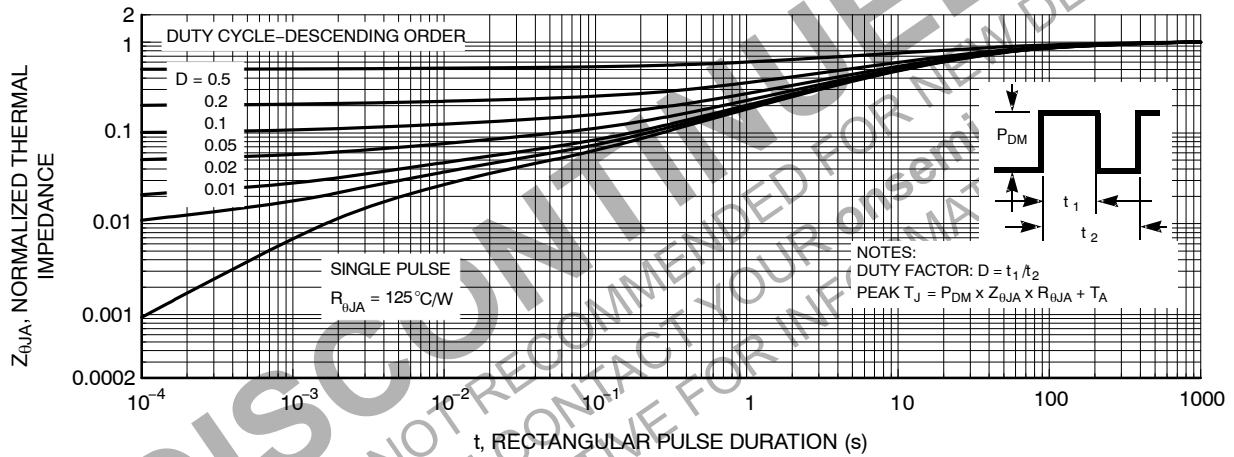


Figure 14. Transient Thermal Response Curve

ORDERING INFORMATION

Device	Device Marking	Package Type	Shipping [†]
FDS8817NZ	FDS8817NZ	SOIC8 (Pb-Free)	2500 / Tape & Reel
FDS8817NZ-G	FDS8817NZ	SOIC8 (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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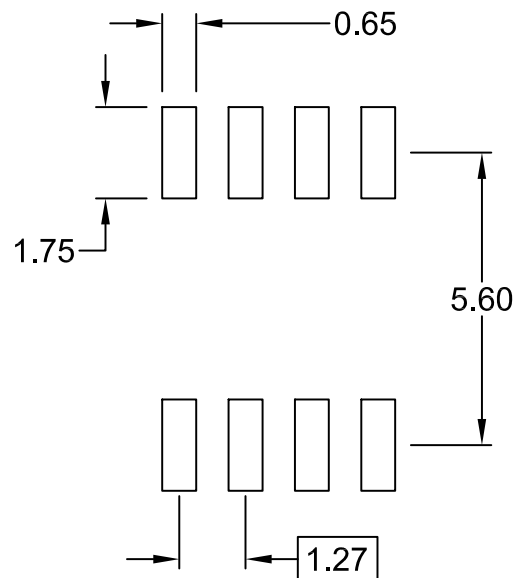
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

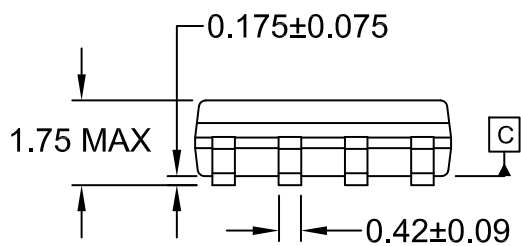


SOIC8
CASE 751EB
ISSUE A

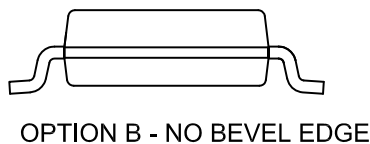
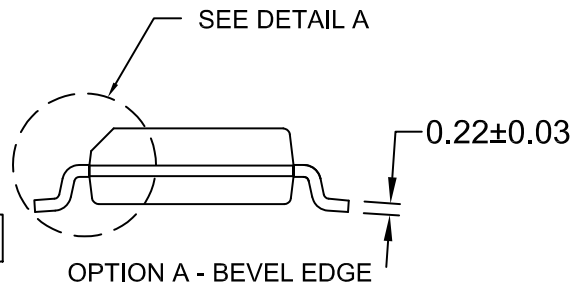
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⊕ 0.25 (M) C B A



⌒ 0.10



NOTES:

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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