MOSFET – N-Channel, POWERTRENCH®

150 V, 4.1 A, 67 mΩ

FDS86242

General Description

This N−Channel MOSFET is produced using **onsemi**’s advanced POWERTRENCH process that has been optimized for $r_{DS(on)}$, switching performance and ruggedness.

Features

- Max $r_{DS(on)} = 67$ mΩ at $V_{GS} = 10$ V, $I_D = 4.1$ A
- Max $r_{DS(on)} = 98$ mΩ at $V_{GS} = 6$ V, $I_D = 3.3$ A
- High Performance Trench Technology for Extremely Low $r_{DS(on)}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- 100% UIL Tested
- ESD Protection Level: HBM > 500 V, CDM > 2 kV
- This Device is Pb−Free, Halide Free and is RoHS Compliant

Applications

- DC/DC Converters and Off−Line UPS
- Distributed Power Architectures and VRMs
- Primary Switch for 24 V and 48 V Systems
- High Voltage Synchronous Rectifier

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

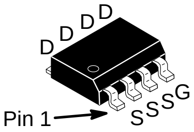
Symbol	Parameter		Ratings	Unit
V_{DS}	Drain to Source Voltage		150	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Drain Current	− Continuous	4.1	A
		− Pulsed	20	
E_{AS}	Single Pulse Avalanche Energy (Note 3)		40	mJ
P_D	Power Dissipation	T_C = 25°C (Note 1)	5.0	W
		T_A = 25°C (Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

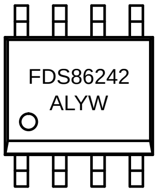
Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	25	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

V_{DSS} MAX	$r_{DS(on)}$ MAX	I_D MAX
150 V	67 mΩ @ 10 V	4.1 A
	98 mΩ @ 3.3 V	



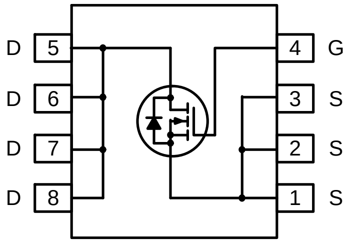
SOIC8
(SO−8)
CASE 751EB

MARKING DIAGRAM



FDS86242	= Device Code
A	= Assembly Site
L	= Wafer Lot Number
YW	= Assembly Start Week

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

June, 2024 − Rev. 2

Publication Order Number:
FDS86242/D

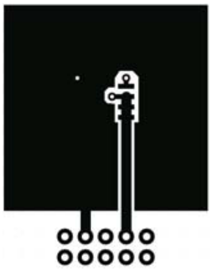
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	150	−	−	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	−	104	−	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 120 V, V_{GS} = 0 V	−	−	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	−	−	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, I_D = 250 μA	2	3.5	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_j}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	−	−10	−	mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 4.1 A	−	56.3	67	mΩ
		V_{GS} = 6 V, I_D = 3.3 A	−	73.8	98	
		V_{GS} = 10 V, I_D = 4.1 A, T_J = 125°C	−	107	126	
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 4.1 A	−	11	−	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 75 V, V_{GS} = 0 V, f = 1MHz	−	570	760	pF
C_{oss}	Output Capacitance		−	64	85	pF
C_{rss}	Reverse Transfer Capacitance		−	2.9	5	pF
R_g	Gate Resistance		−	0.5	−	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 75 V, I_D = 4.1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	−	7.9	16	ns
t_r	Rise Time		−	1.5	10	ns
$t_{d(off)}$	Turn−Off Delay Time		−	13	23	ns
t_f	Fall Time		−	2.8	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 75 V, I_D = 4.1 A	−	8.9	13	nC
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 5 V, V_{DD} = 75 V, I_D = 4.1 A	−	4.9	7	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 75 V, I_D = 4.1 A	−	3.0	−	nC
Q_{gd}	Gate to Drain “Miller” Charge		−	2.0	−	nC
DRAIN−SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 4.1 A (Note 2)	−	0.81	1.3	V
		V_{GS} = 0 V, I_S = 2 A (Note 2)	−	0.77	1.2	
t_{rr}	Reverse Recovery Time	I_F = 4.1 A, di/dt = 100 A/μs	−	61	98	ns
Q_{rr}	Reverse Recovery Charge		−	71	114	nC

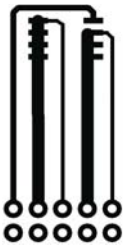
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.



a) 50°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b) 125°C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Starting T_J = 25°C, L = 1 mH, I_{AS} = 9 A, V_{DD} = 135 V, V_{GS} = 10 V.

TYPICAL CHARACTERISTICS

(T_J = 25°C UNLESS OTHERWISE NOTED)

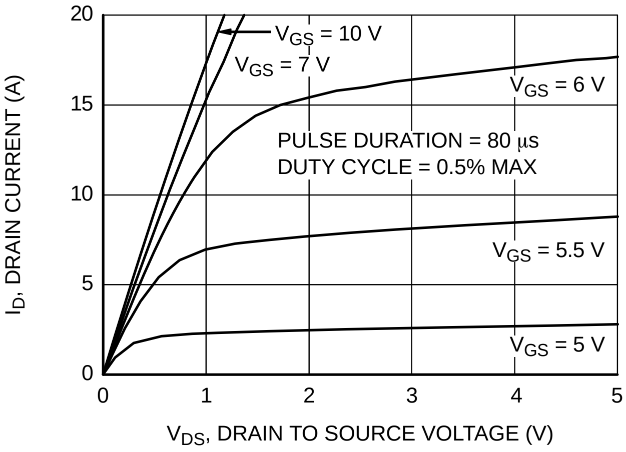


Figure 1. On−Region Characteristics

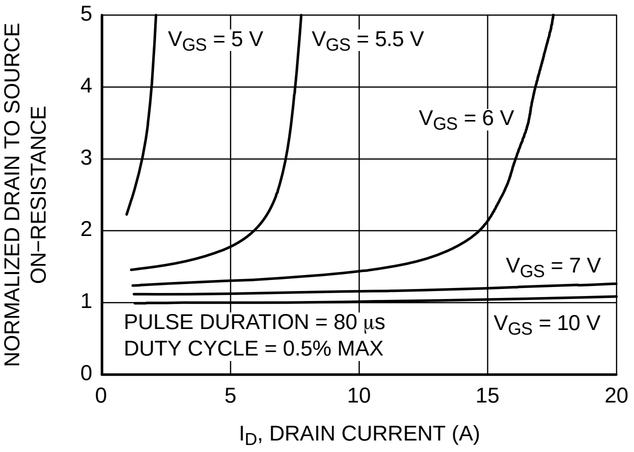


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

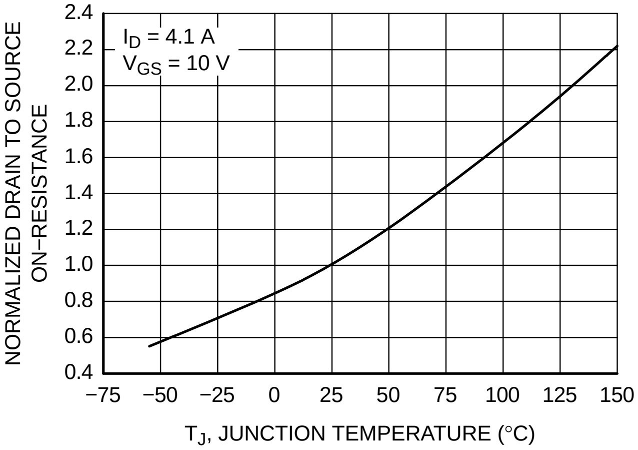


Figure 3. Normalized On− Resistance vs. Junction Temperature

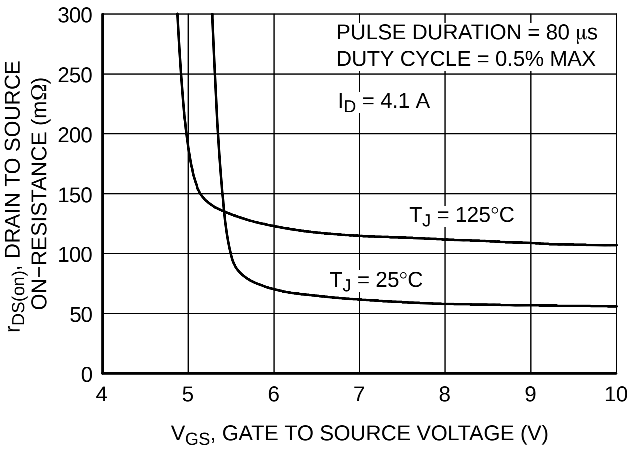


Figure 4. On−Resistance vs. Gate to Source Voltage

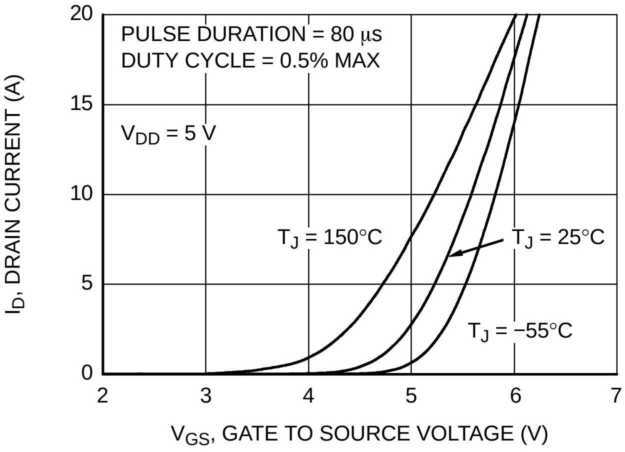


Figure 5. Transfer Characteristics

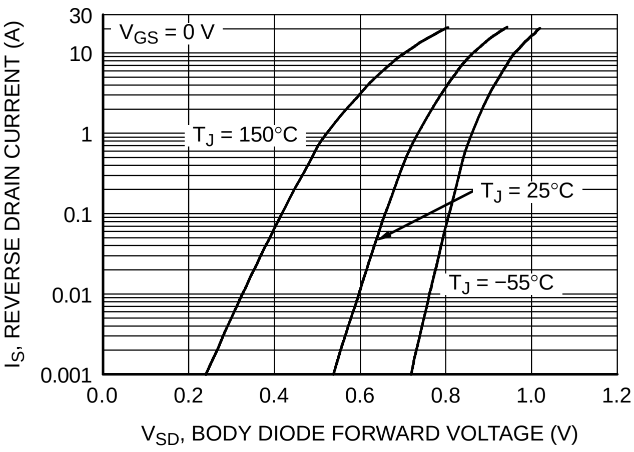


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS

(T_J = 25°C UNLESS OTHERWISE NOTED) (CONTINUED)

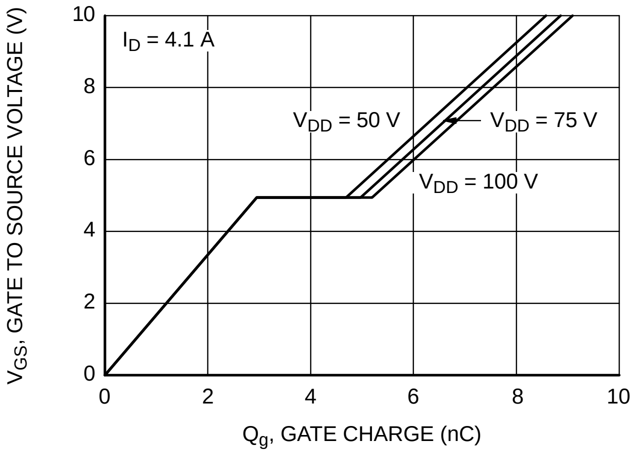


Figure 7. Gate Charge Characteristics

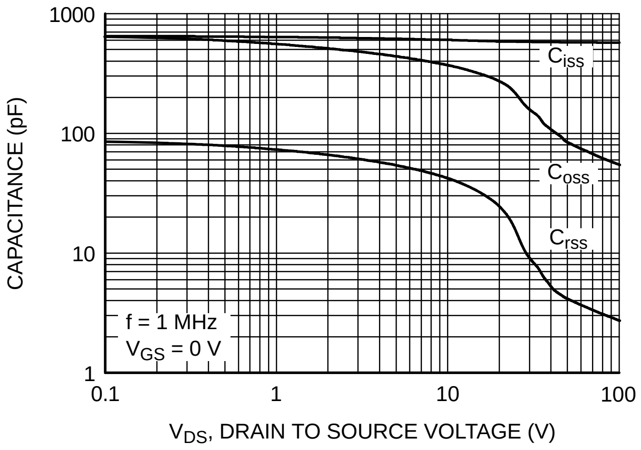


Figure 8. Capacitance vs. Drain to Source Voltage

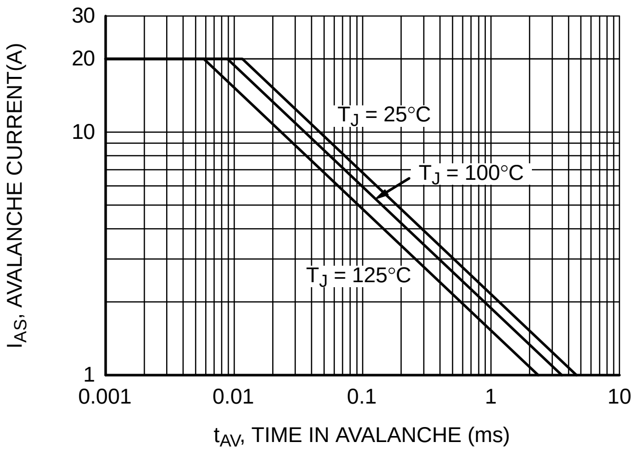


Figure 9. Unclamped Inductive Switching Capability

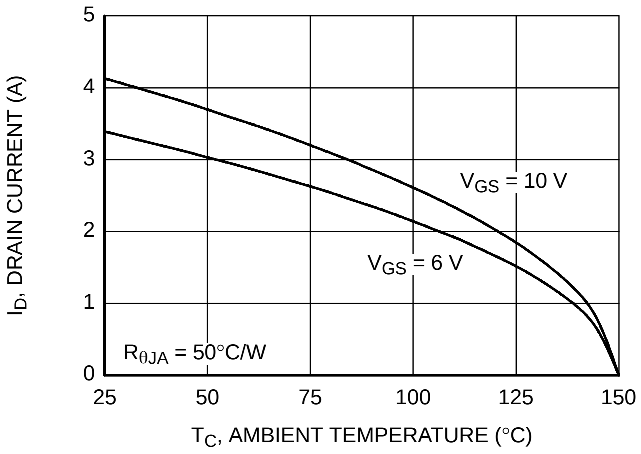


Figure 10. Maximum Continuous Drain Current vs. Ambient Temperature

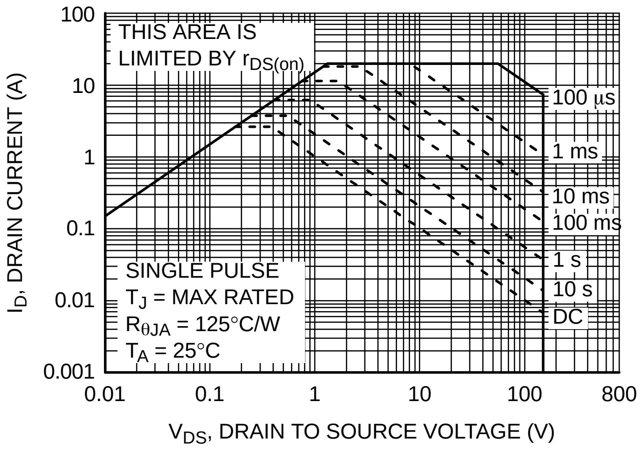


Figure 11. Forward Bias Safe Operating Area

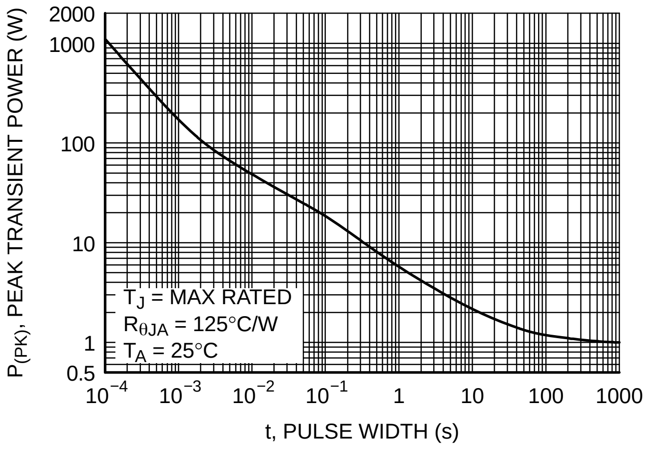


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS

(T_J = 25°C UNLESS OTHERWISE NOTED) (CONTINUED)

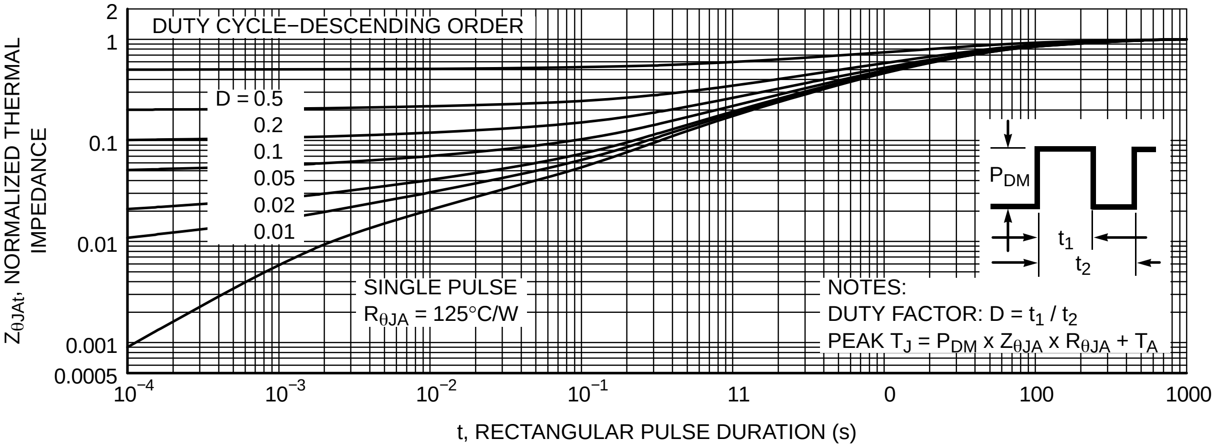


Figure 13. Junction−to−Ambient Transient Thermal Response Curve

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping†
FDS86242	FDS86242	SOIC8 (SO−8) (Pb−Free, Halide Free)	13”	12 mm	2500 / Tape & Reel

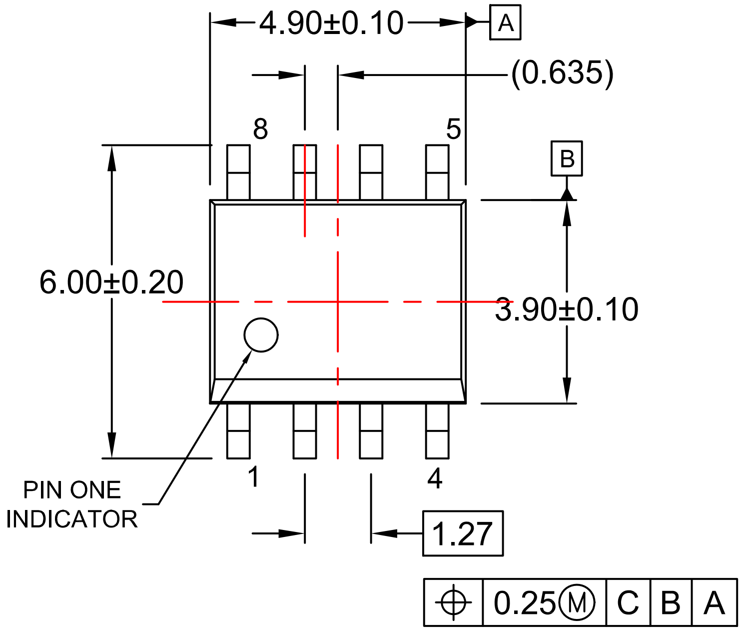
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

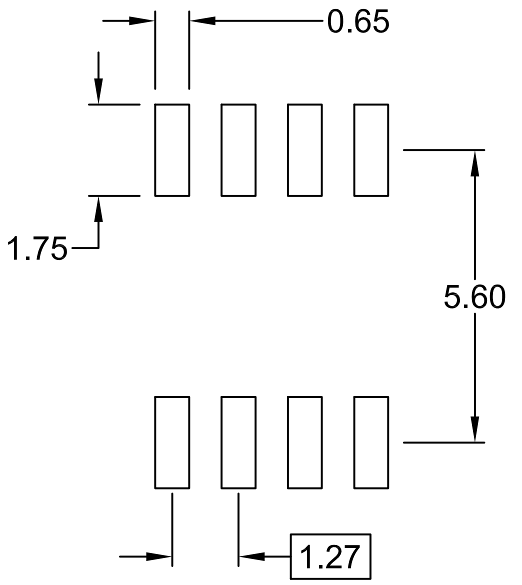
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

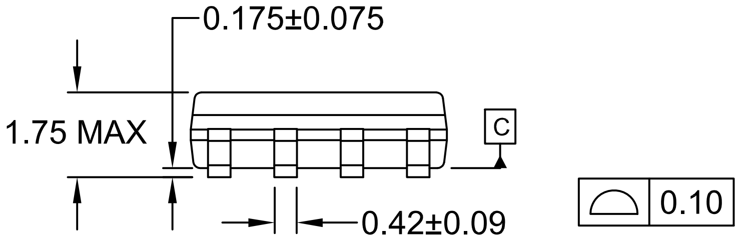
SOIC8
CASE 751EB
ISSUE A

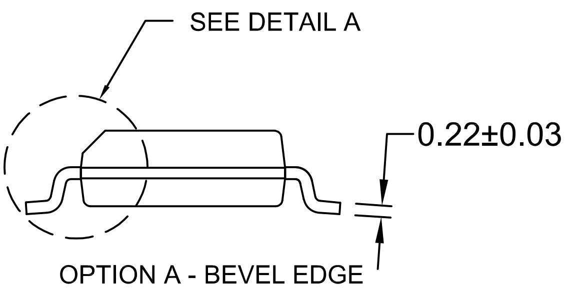
DATE 24 AUG 2017



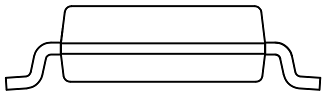


LAND PATTERN RECOMMENDATION

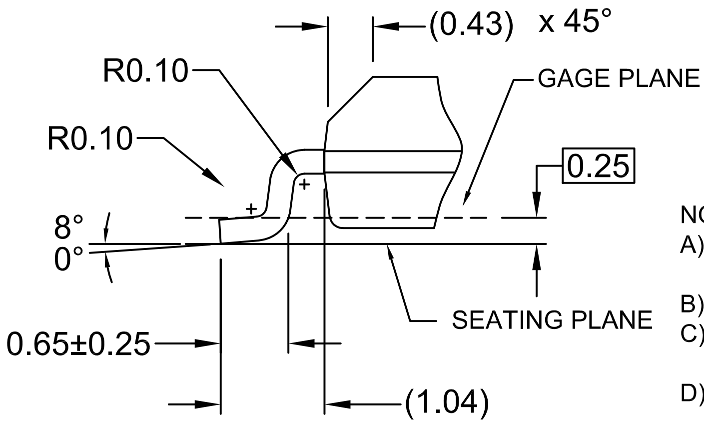




OPTION A - BEVEL EDGE



OPTION B - NO BEVEL EDGE



DETAIL A
SCALE: 2:1

NOTES:
- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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