

# MOSFET – N-Channel, Shielded Gate, POWERTRENCH®

100 V, 43 A, 14 mΩ

## FDMC86160

### General Description

This N-Channel MOSFET is produced using onsemi's advanced PowerTrench process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance. This device is well suited for applications where ultra low  $R_{DS(on)}$  is required in small spaces such as High performance VRM, POL and orring functions.

### Applications

- Bridge Topologies
- Synchronous Rectifier

### Features

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)}$  = 14 mΩ at  $V_{GS} = 10$  V,  $I_D = 9$  A
- Max  $r_{DS(on)}$  = 23 mΩ at  $V_{GS} = 6$  V,  $I_D = 7$  A
- High Performance Technology for Extremely Low  $r_{DS(on)}$
- This Device is Lead-Free and RoHS Compliant

### ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise noted

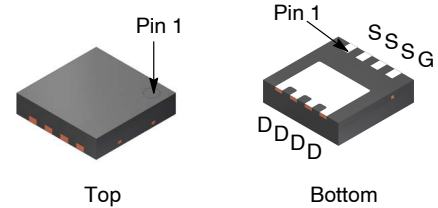
Symbol	Parameter	Value	Unit	
$V_{DSS}$	Drain-Source Voltage	100	V	
$V_{GSS}$	Gate-Source Voltage	±20	V	
$I_D$	Drain Current		A	
	- Continuous ( $T_C = 25^\circ\text{C}$ )	43		
	- Continuous ( $T_A = 25^\circ\text{C}$ ) (Note 1a)	9		
	- Pulsed (Note 4)	50		
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	181	mJ	
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	54	W
		( $T_A = 25^\circ\text{C}$ ) (Note 1a)	2.3	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise noted

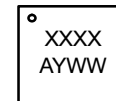
Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Ambient (Note 1)	2.3	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Case (Note 1a)	53	$^\circ\text{C}/\text{W}$

$V_{DS}$	$r_{DS(on)}$ MAX	$I_D$ MAX
100 V	14 mΩ @ 10 V	43 A
	23 mΩ @ 6 V	



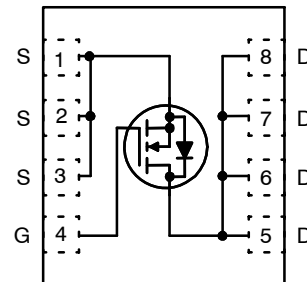
WDFN8 3.3X3.3, 0.65P  
CASE 483AW

### MARKING DIAGRAM



XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week

### PIN ASSIGNMENT



### ORDERING INFORMATION

Device	Package	Shipping†
FDMC86160	WDFN8 3.3X3.3, 0.65P CASE 483AW (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# FDMC86160

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

B <sub>V</sub> DSS	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V	100	-	-	V
$\frac{\Delta B_{V_{DSS}}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25°C	-	73	-	mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V	-	-	1	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V	-	-	±100	nA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	2	2.9	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, referenced to 25°C	-	-9	-	mV/°C
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 9 A	-	11.2	14	mΩ
		V <sub>GS</sub> = 6 V, I <sub>D</sub> = 7 A	-	16	23	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 9 A, T <sub>J</sub> = 125°C	-	21	26	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 9 A	-	43	-	S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	968	1290	pF
C <sub>oss</sub>	Output Capacitance		-	241	320	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	11	20	pF
R <sub>g</sub>	Gate Resistance		0.1	0.6	2.5	Ω

### SWITCHING CHARACTERISTICS

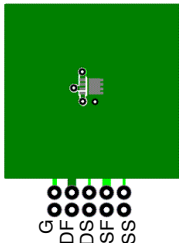
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 9 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω	-	9.7	19	ns	
t <sub>r</sub>	Rise Time		-	3.6	10	ns	
t <sub>d(off)</sub>	Turn-Off Delay Time		-	16	30	ns	
t <sub>f</sub>	Fall Time		-	3.4	10	ns	
Q <sub>g(TOT)</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 9 A	-	15	22	nC
Q <sub>g(TOT)</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to 6 V		-	9.8	15	nC
Q <sub>gs</sub>	Total Gate Charge			-	4.4	-	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge			-	3.5	-	nC

### DRAIN-SOURCE DIODE CHARACTERISTICS

V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 9 A (Note 2)	-	0.79	1.3	V
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.9 A (Note 2)	-	0.72	1.2	
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 9 A, di/dt = 100 A/μs	-	47	75	ns
Q <sub>rr</sub>	Reverse Recovery Charge		-	45	73	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- R<sub>θJA</sub> is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.



a. 53°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 125°C/W when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
- E<sub>AS</sub> of 181 mJ is based on starting T<sub>J</sub> = 25 °C, L = 3 mH, I<sub>AS</sub> = 11 A, V<sub>DD</sub> = 100 V, V<sub>GS</sub> = 10 V. 100% test at L = 0.1 mH, I<sub>AS</sub> = 35 A.
- Pulse Id refers to Figure.11 Forward Bias Safe Operation Area.

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

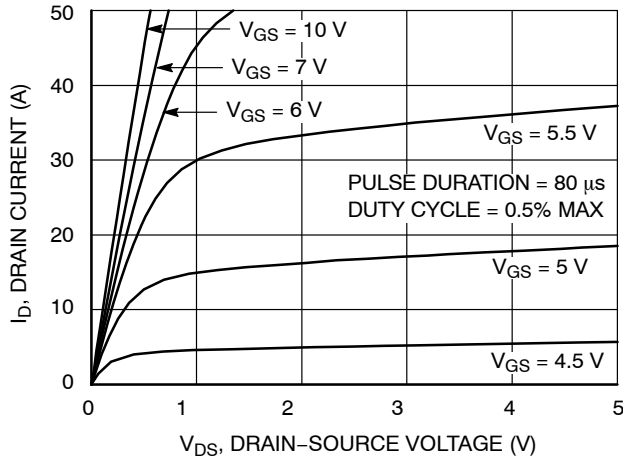


Figure 1. On-Region Characteristics

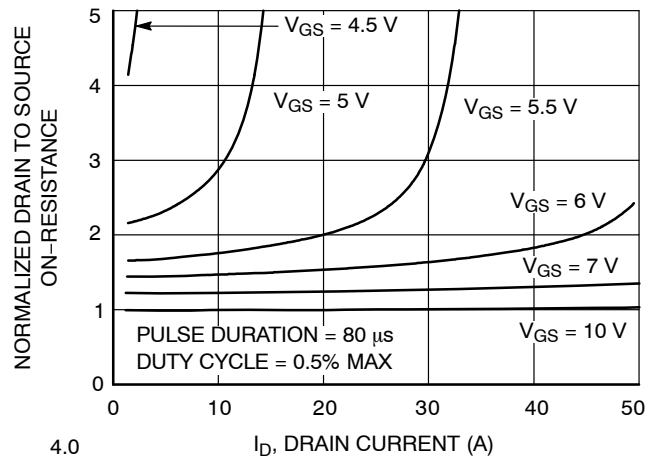


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

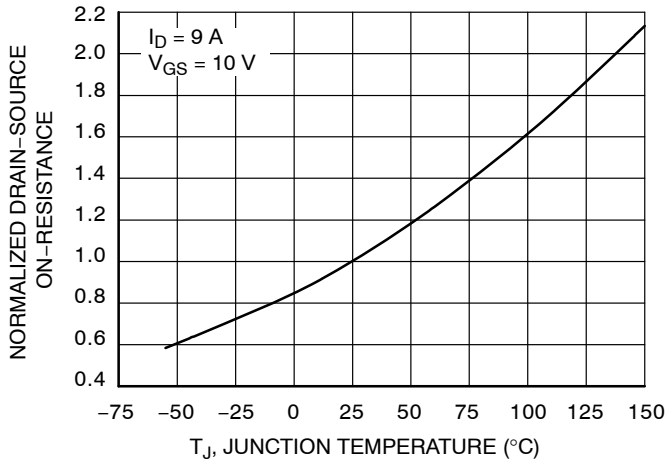


Figure 3. Normalized On-Resistance vs Junction Temperature

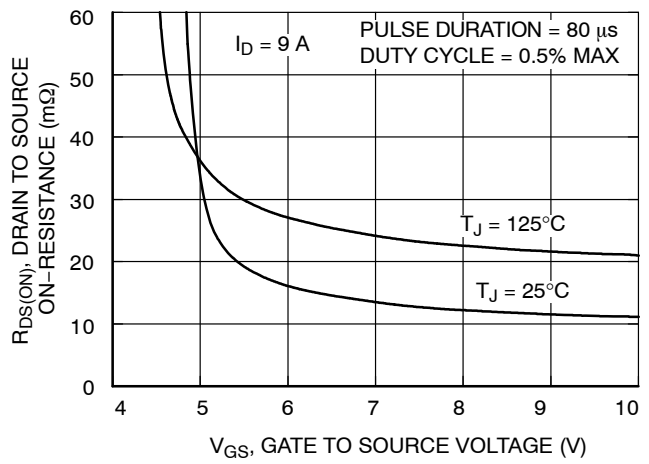


Figure 4. On-Resistance vs Gate to Source Voltage

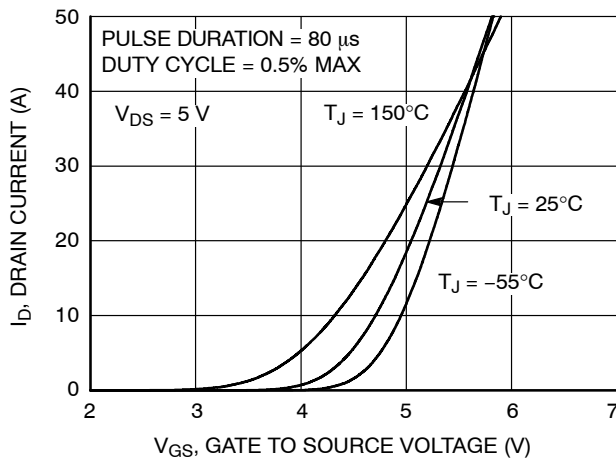


Figure 5. Transfer Characteristics

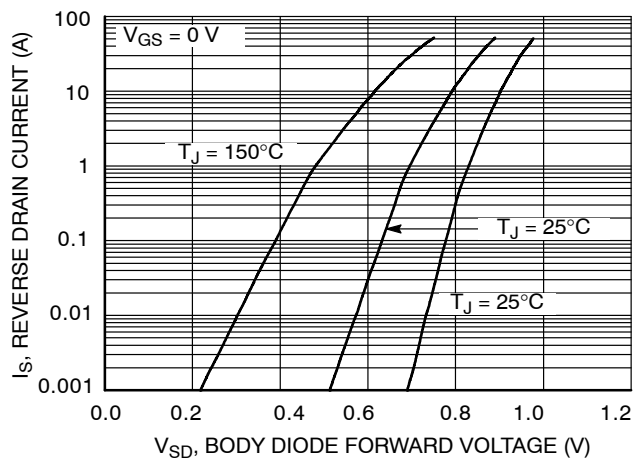


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

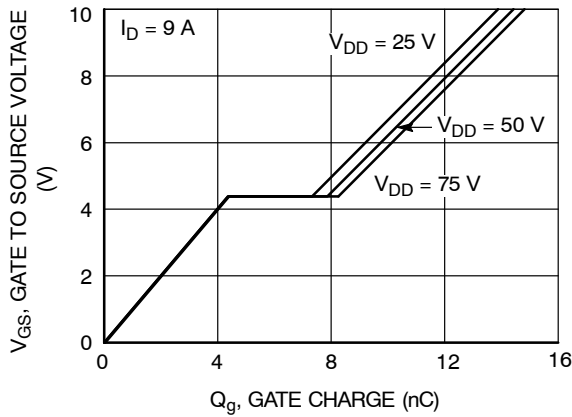


Figure 7. Gate Charge Characteristics

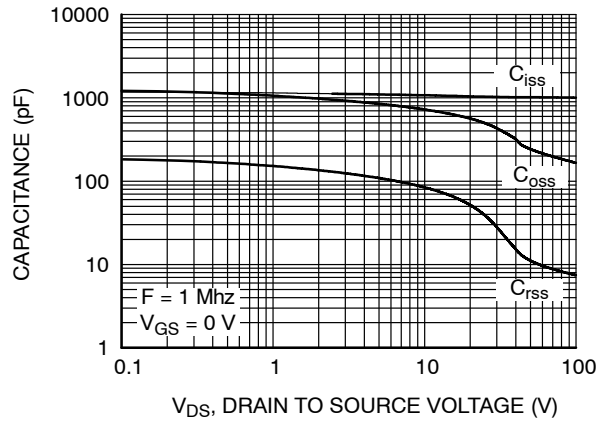


Figure 8. Capacitance vs Drain to Source Voltage

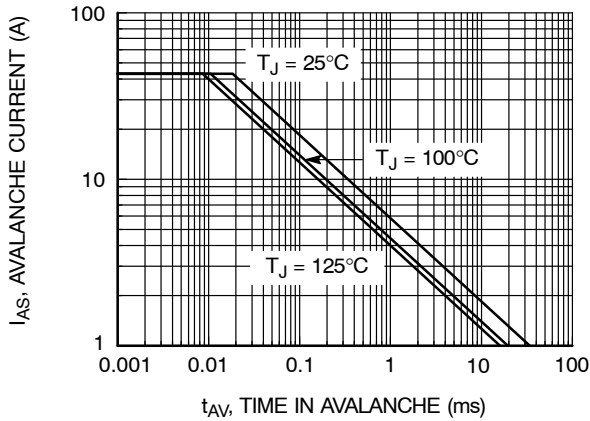


Figure 9. Unclamped Inductive Switching Capability

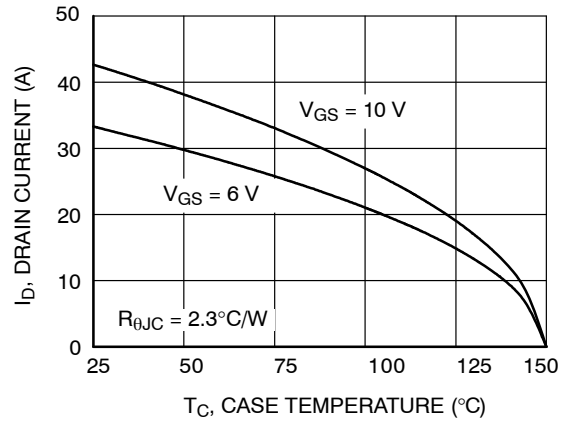


Figure 10. Maximum Continuous Drain Current vs Case Temperature

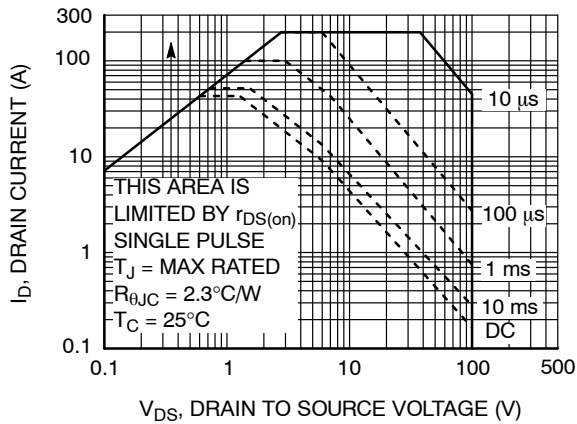


Figure 11. Forward Bias Safe Operating Area

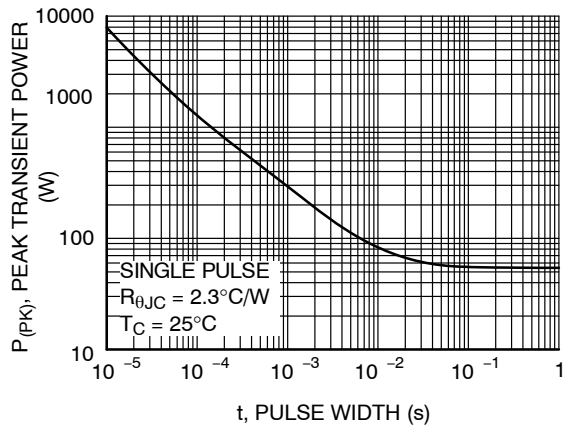


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)

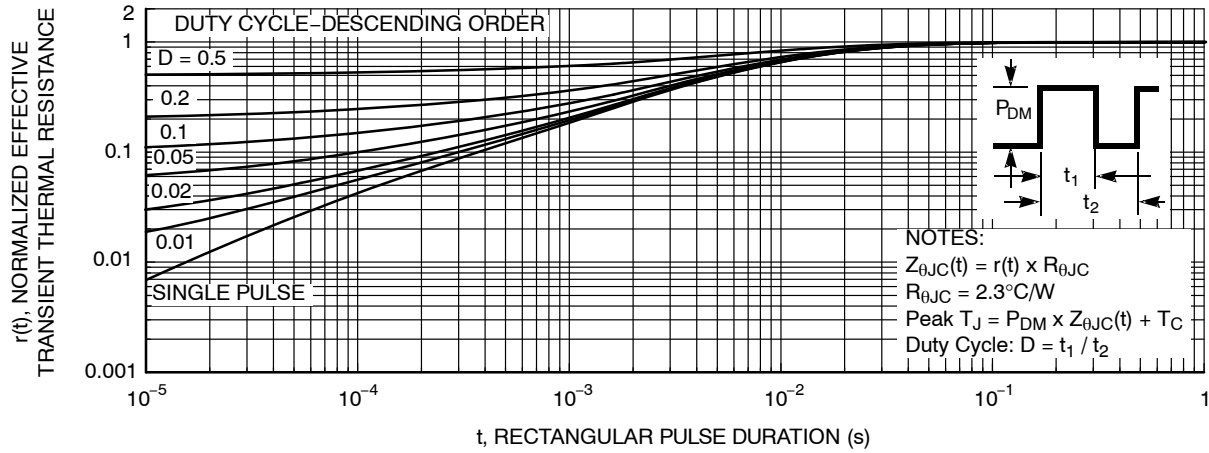
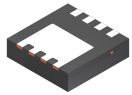


Figure 13. Junction-to-Case Transient Thermal Response Curve

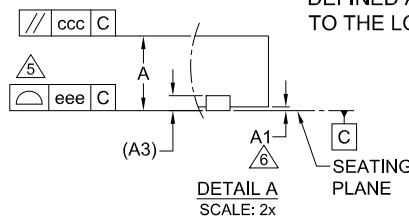
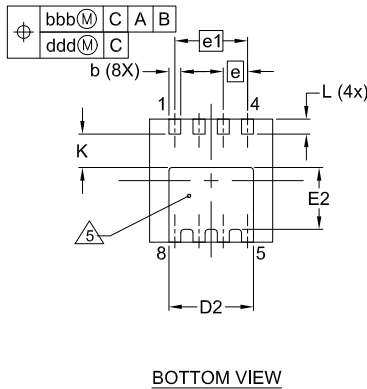
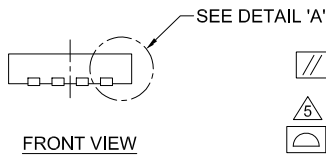
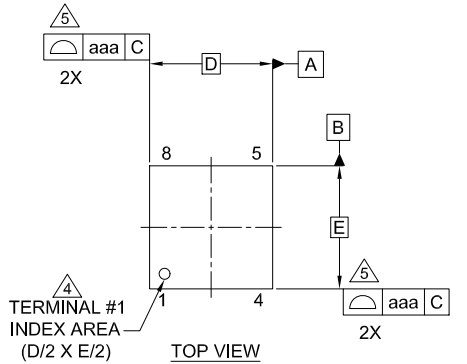
# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

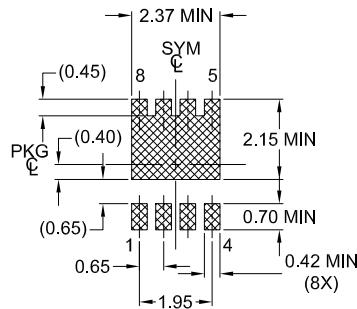


**WDFN8 3.30x3.30x0.75, 0.65P**  
**CASE 483AW**  
**ISSUE B**

DATE 22 MAR 2024



### LAND PATTERN RECOMMENDATION



### NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEP95 SEC. 3 SPP-12. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD, EMBEDDED METAL OR MARKED FEATURE.
5. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	--	--	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	3.30 BSC		
D2	2.17	2.27	2.37
E	3.30 BSC		
E2	1.56	1.66	1.76
e	0.65 BSC		
e1	1.95 BSC		
K	0.90	--	--
L	0.30	0.40	0.50
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.05		

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



XXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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