

MOSFET – N-Channel, POWERTRENCH®

30 V, 13.3 A, 8.5 mΩ

FDMC7692

General Description

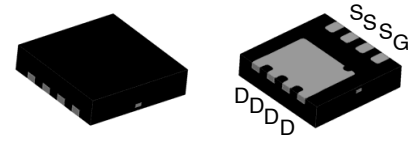
This N-Channel MOSFET is produced using onsemi’s advanced POWERTRENCH process that has been especially tailored to minimize the on-state resistance. This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

Features

- Max $r_{DS(on)}$ = 8.5 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 13.3\text{ A}$
- Max $r_{DS(on)}$ = 11.5 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 10.6\text{ A}$
- High Performance Technology for Extremely Low $r_{DS(on)}$
- These Devices are Pb-Free and are RoHS Compliant

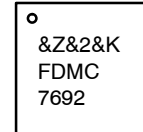
Applications

- DC – DC Buck Converters
- Notebook Battery Power Management
- Load Switch in Notebook



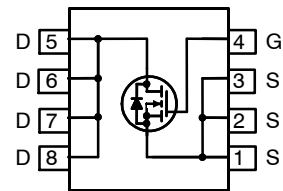
Top Bottom
 WDFN8 3.3x3.3, 0.65P
 CASE 511DQ (Option A)

MARKING DIAGRAM



&Z = Assembly Plant Code
 &2 = 2-Digit Date Code
 &K = 2-Digit Lot Code
 FDMC7692 = Device Code

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

FDMC7692

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

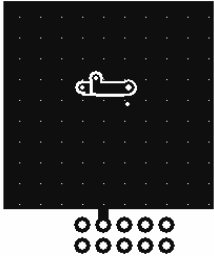
Symbol	Parameter	Rating	Unit			
V_{DS}	Drain to Source Voltage	30	V			
V_{GS}	Gate to Source Voltage	± 20	V			
I_D	Drain Current	Continuous (Package limited)	$T_C = 25^\circ\text{C}$	16	A	
		Continuous (Note 1a)	$T_A = 25^\circ\text{C}$			13.3
		Pulsed				40
E_{AS}	Single Pulse Avalanche Energy (Note 2)	58	mJ			
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	29	W		
	Power Dissipation (Note 1a)	$T_A = 25^\circ\text{C}$	2.3			
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$			

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	4.3	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



- 53 $^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



- 125 $^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

- E_{AS} of 58 mJ is based on starting $T_J = 25^\circ\text{C}$; $L = 1$ mH, $I_{AS} = 10.8$ A, $V_{DD} = 27$ V, $V_{GS} = 10$ V. 100% test at $L = 0.1$ mH, $I_{AS} = 21$ A.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}$, $V_{GS} = 0 \text{ V}$	30	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C	-	16	-	$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V}$, $V_{GS} = 0 \text{ V}$	-	-	1	μA
		$V_{DS} = 24 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 125^\circ\text{C}$	-	-	250	
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = 20 \text{ V}$, $V_{DS} = 0 \text{ V}$	-	-	100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250 \mu\text{A}$	1.2	1.9	3.0	V
$\Delta V_{GS(th)} / \Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C	-	-6	-	$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}$, $I_D = 13.3 \text{ A}$	-	7.2	8.5	$\text{m}\Omega$
		$V_{GS} = 4.5 \text{ V}$, $I_D = 10.6 \text{ A}$	-	9.5	11.5	
		$V_{GS} = 10 \text{ V}$, $I_D = 13.3 \text{ A}$, $T_J = 125^\circ\text{C}$	-	9.5	12.0	
g_{FS}	Forward Transconductance	$V_{DD} = 5 \text{ V}$, $I_D = 13.3 \text{ A}$	-	60	-	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 15 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$	-	1260	1680	pF
C_{oss}	Output Capacitance		-	480	635	pF
C_{rss}	Reverse Transfer Capacitance		-	65	100	pF
R_g	Gate Resistance	$f = 1 \text{ MHz}$	-	0.9	2.4	Ω

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15 \text{ V}$, $I_D = 13.3 \text{ A}$, $V_{GS} = 10 \text{ V}$, $R_{GEN} = 6 \Omega$	-	9	18	ns
t_r	Rise Time		-	4	10	ns
$t_{d(off)}$	Turn-Off Delay Time		-	21	33	ns
t_f	Fall Time		-	3	10	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0 \text{ V}$ to 10 V , $V_{DD} = 15 \text{ V}$, $I_D = 13.3 \text{ A}$	-	21	29	nC
		$V_{GS} = 0 \text{ V}$ to 4.5 V , $V_{DD} = 15 \text{ V}$, $I_D = 13.3 \text{ A}$	-	10	14	nC
Q_{gs}	Total Gate Charge	$V_{DD} = 15 \text{ V}$, $I_D = 13.3 \text{ A}$	-	5	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	3	-	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}$, $I_S = 13.3 \text{ A}$ (Note 3)	-	0.86	1.2	V
		$V_{GS} = 0 \text{ V}$, $I_S = 1.9 \text{ A}$ (Note 3)	-	0.75	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 13.3 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$	-	24	38	ns
Q_{rr}	Reverse Recovery Charge		-	7	14	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

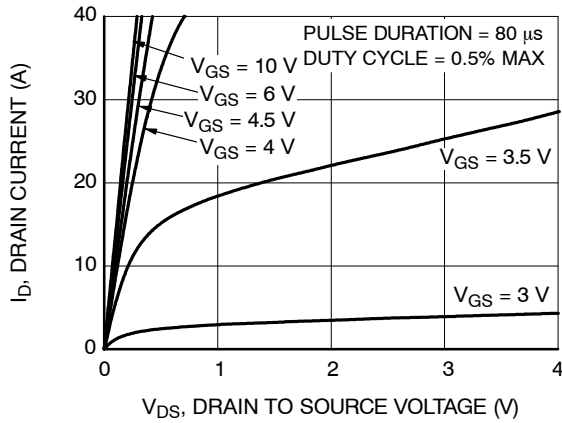


Figure 1. On Region Characteristics

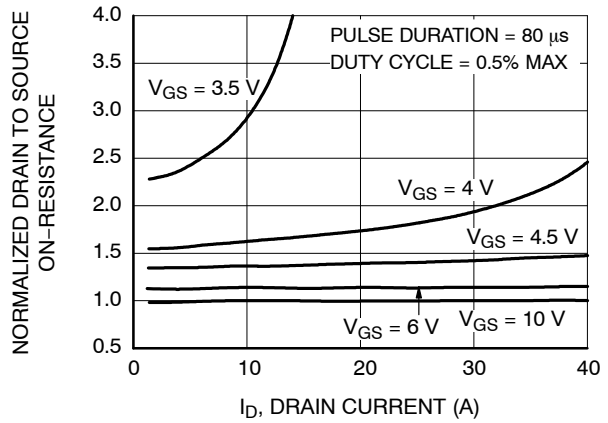


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

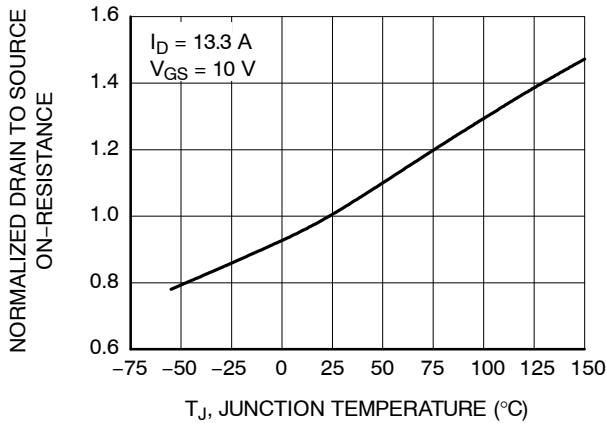


Figure 3. Normalized On Resistance vs. Junction Temperature

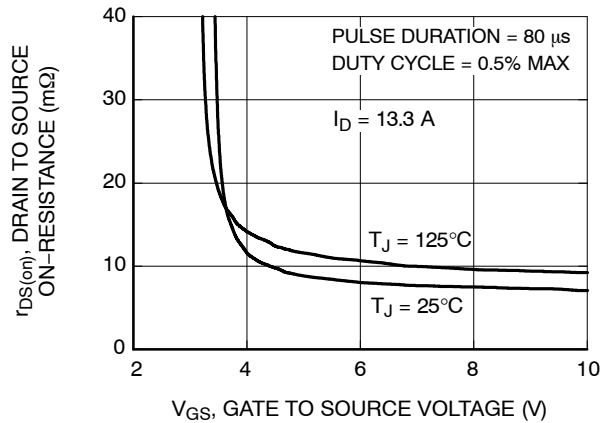


Figure 4. On-Resistance vs. Gate to Source Voltage

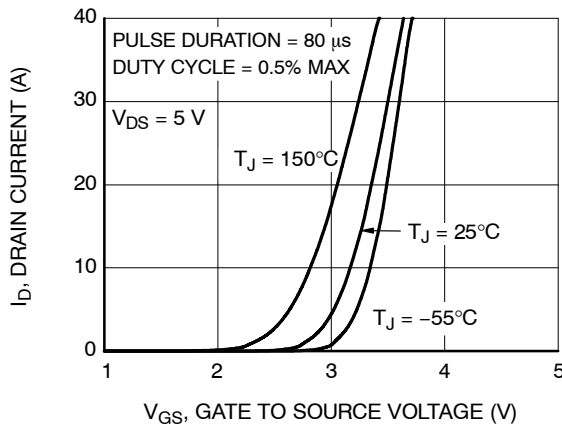


Figure 5. Transfer Characteristics

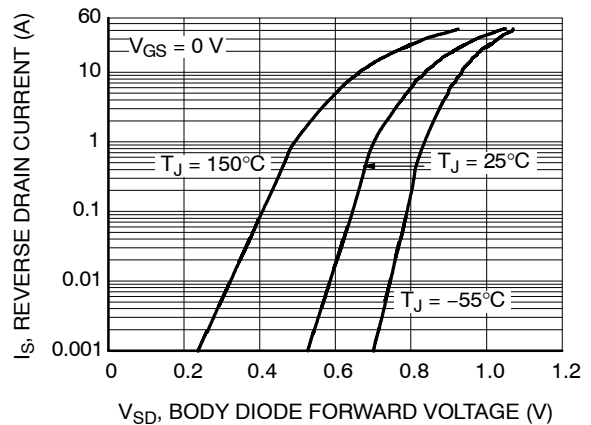


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

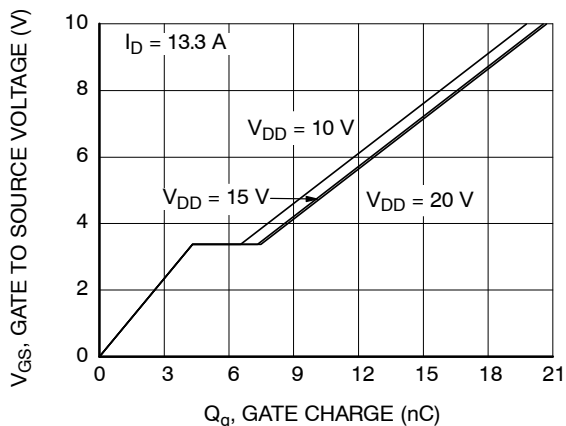


Figure 7. Gate Charge Characteristics

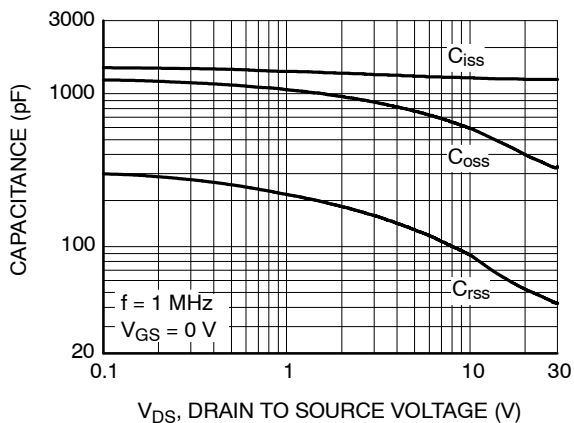


Figure 8. Capacitance vs. Drain to Source Voltage

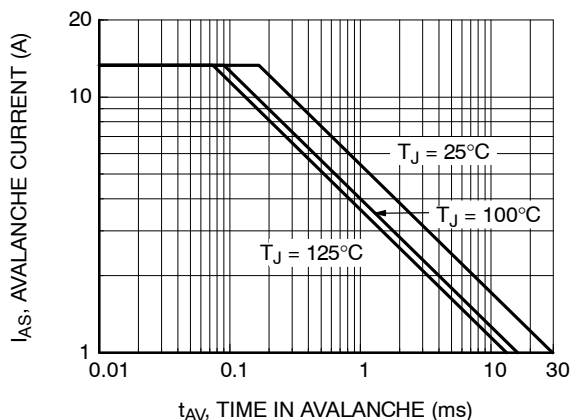


Figure 9. Unclamped Inductive Switching Capability

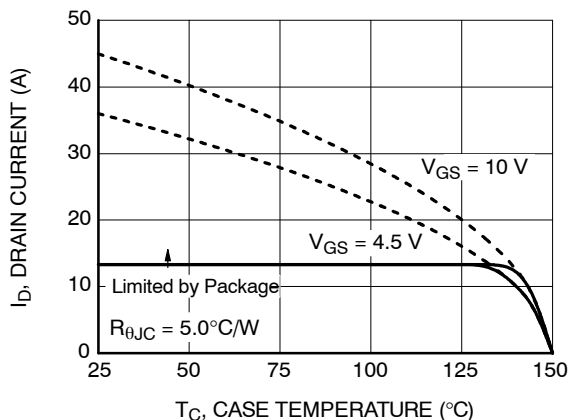


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

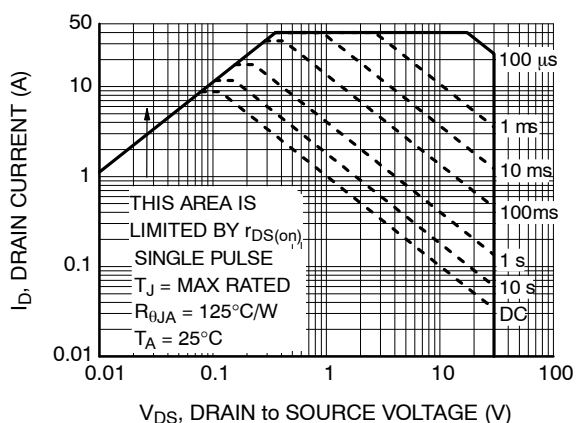


Figure 11. Forward Bias Safe Operating Area

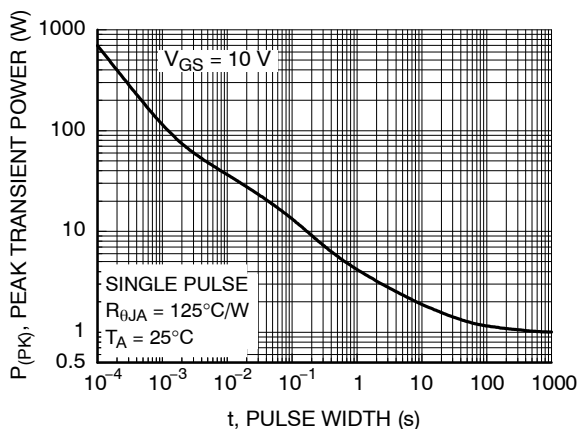


Figure 12. Single Pulse Maximum Power Dissipation

FDMC7692

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

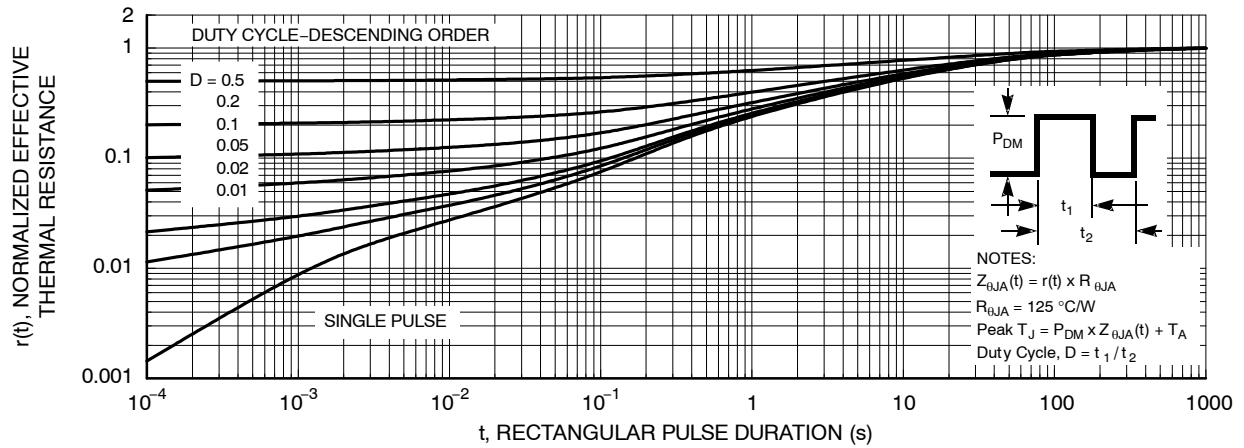


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

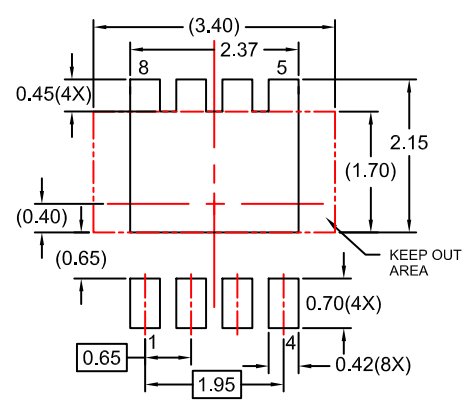
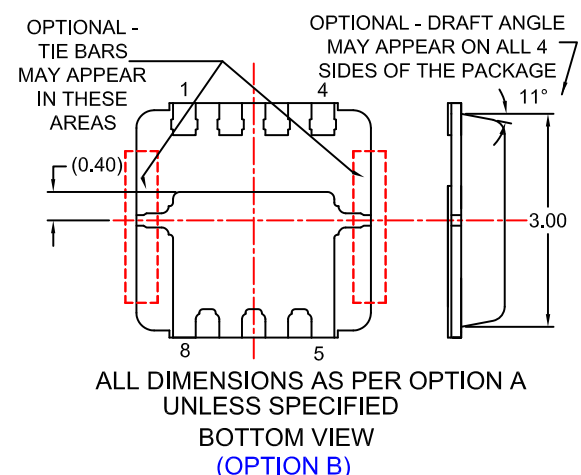
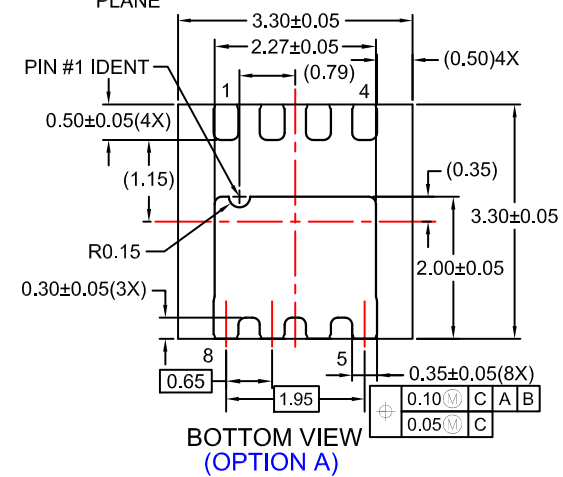
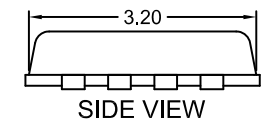
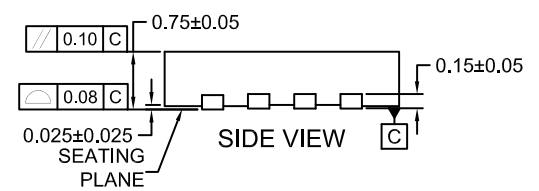
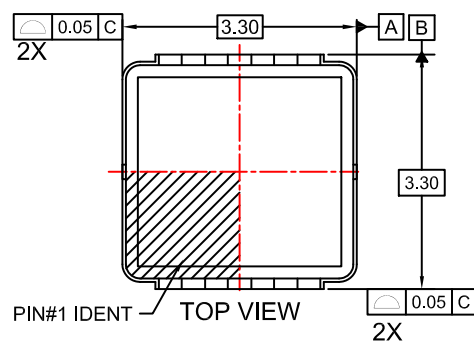
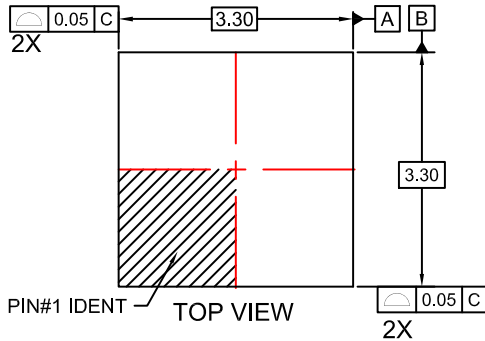
ORDERING INFORMATION

Device	Device Marking	Package Type	Shipping [†]
FDMC7692	FDMC7692	WDFN8 3.3x3.3, 0.65P case 511DQ (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

WDFN8 3.3x3.3, 0.65P
CASE 511DQ
ISSUE O

DATE 31 OCT 2016

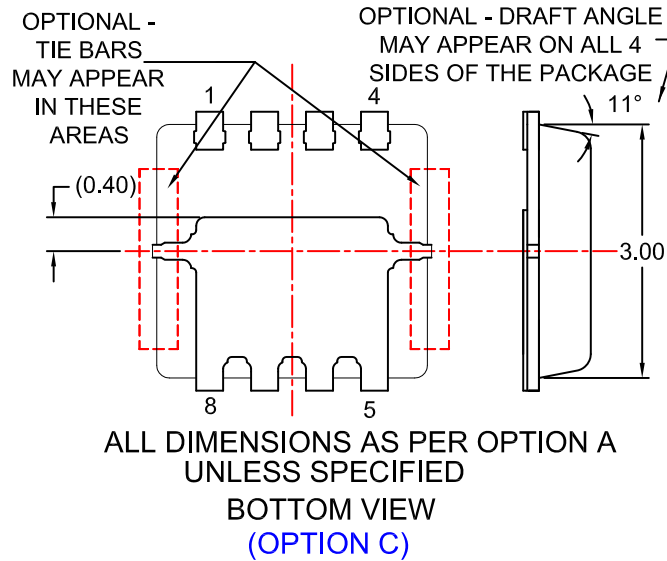
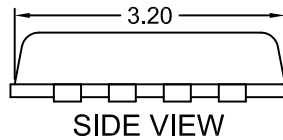
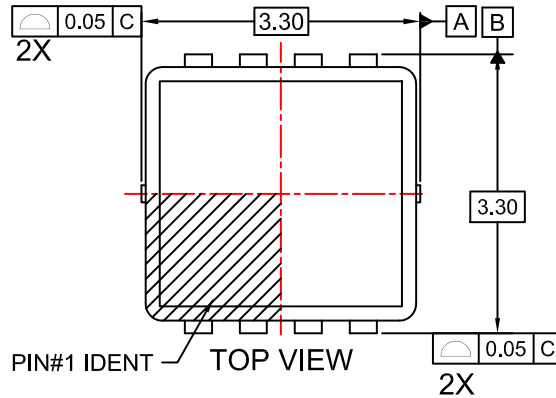


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WDFN8 3.3x3.3, 0.65P
CASE 511DQ
ISSUE O

DATE 31 OCT 2016



NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-240.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN
- E. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. BURRS OR MOLD FLASH SHALL NOT EXCEED 0.10MM.

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