DATA SHEET
www.onsemi.com

Digital FET, Dual P-Channel

FDG6304P

General Description

These dual P−Channel logic level enhancement mode field effect transistors are produced using **onsemi** proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on−state resistance. This device has been designed especially for low voltage applications as a replacement for bipolar digital transistors and small signal MOSFETs.

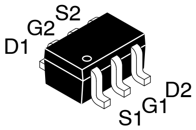
Features

- −25 V, −0.41 A Continuous, −1.5 A Peak
  - $R_{DS(ON)} = 1.1\ \Omega$ @ $V_{GS} = -4.5$ V
  - $R_{DS(ON)} = 1.5\ \Omega$ @ $V_{GS} = -2.7$ V
- Very Low Level Gate Drive Requirements Allowing Direct Operation in 3 V Circuits ($V_{GS(th)} < 1.5$ V)
- Gate−Source Zener for ESD Ruggedness (>6 kV Human Body Model)
- Compact Industry Standard SC70−6 Surface Mount Package
- These Devices are Pb−Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

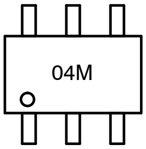
Symbol	Parameter		FDG6304P	Units
V_{DSS}	Drain−Source Voltage		−25	V
V_{GSS}	Gate−Source Voltage		−8	V
I_D	Drain/Output Current	Continuous	−0.41	A
		Pulsed	−1.5	
P_D	Maximum Power Dissipation (Note 1)		0.3	W
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +150	°C
ESD	Electrostatic Discharge Rating MIL−STD−883D Human Body Model (100 pF / 1500 Ω)		6.0	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



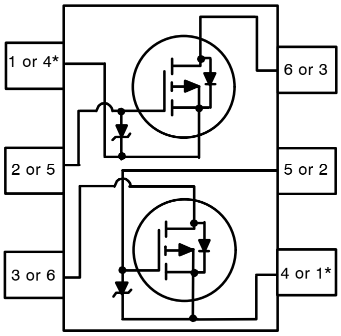
SC−88/SC70−6/SOT−363
CASE 419B−02

MARKING DIAGRAM



04 = Specific Device Code
M = Assembly Operation Month

PIN CONNECTIONS



*The pinouts are symmetrical; pin 1 and 4 are interchangeable.
Units inside the carrier can be of either orientation and will not affect the functionality of the device.

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

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THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient (Note 1)	415	°C/W

1. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ = 415°C/W on minimum pad mounting on FR−4 board in still air.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain−Source Breakdown Voltage	V_{GS} = 0 V, I_D = −250 μA	−25	−	−	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = −250 μA, Referenced to 25°C	−	−22	−	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −20 V, V_{GS} = 0 V	−	−	−1	μA
		V_{DS} = −20 V, V_{GS} = 0 V, T_J = 55°C	−	−	−10	μA
I_{GSS}	Gate−Body Leakage Current	V_{GS} = −8 V, V_{DS} = 0 V	−	−	100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = −250 μA	−0.65	−0.82	−1.5	V
$\Delta V_{GS(th)}$ / ΔT_J	Gate Threshold Voltage Temperature Coefficient	I_D = −250 μA, Referenced to 25°C	−	2	−	mV/°C
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = −4.5 V, I_D = −0.41 A	−	0.85	1.1	Ω
		V_{GS} = −4.5 V, I_D = −0.41 A, T_J = 125°C	−	1.2	1.9	
		V_{GS} = −2.7 V, I_D = −0.25 A	−	1.15	1.5	
$I_{D(on)}$	On−State Drain Current	V_{GS} = −4.5 V, V_{DS} = −5 V	−1.5	−	−	A
g_{FS}	Forward Transconductance	V_{DS} = −5 V, I_D = −0.41 A	−	0.9	−	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz	−	62	−	pF
C_{oss}	Output Capacitance		−	34	−	pF
C_{rss}	Reverse Transfer Capacitance		−	10	−	pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn-On Delay Time	V_{DD} = −5 V, I_D = −0.5 A, V_{GS} = −4.5 V, R_{GEN} = 6 Ω	−	7	15	ns
t_r	Turn-On Rise Time		−	8	16	ns
$t_{D(off)}$	Turn-Off Delay Time		−	55	80	ns
t_f	Turn-Off Fall Time		−	35	60	ns
Q_g	Total Gate Charge	V_{DS} = −5 V, I_D = −0.41 A, V_{GS} = −4.5 V	−	1.1	1.5	nC
Q_{gs}	Gate−Source Charge		−	0.31	−	nC
Q_{gd}	Gate−Drain Charge		−	0.29	−	nC
DRAIN−SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Source Current		−	−	−0.25	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = −0.25 A (Note 2)	−	−0.85	−1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

TYPICAL PERFORMANCE CHARACTERISTICS

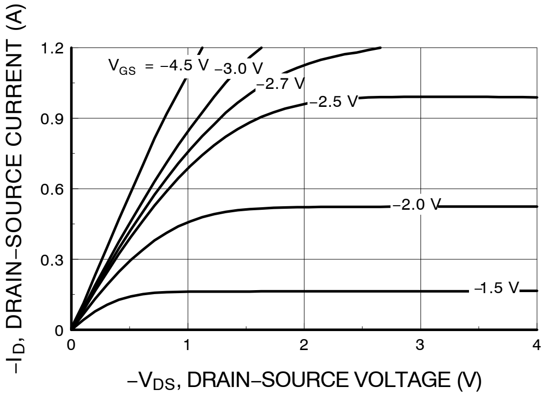


Figure 1. On−Region Characteristics

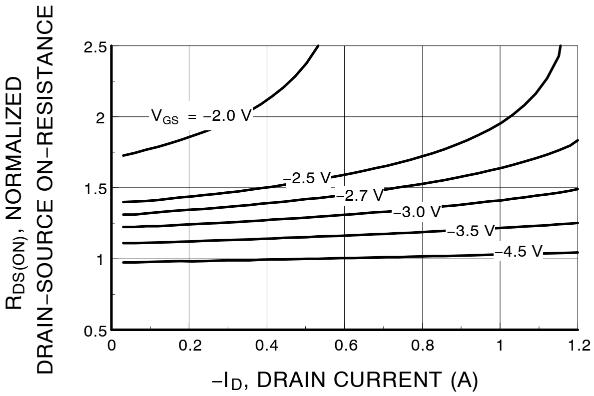


Figure 2. On−Resistance Variation with Drain Current and Gate Voltage

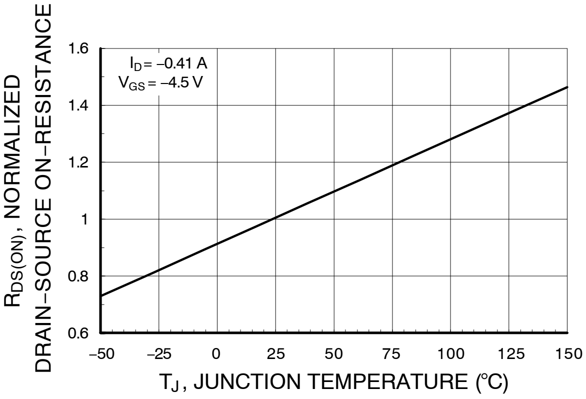


Figure 3. On−Resistance Variation with Temperature

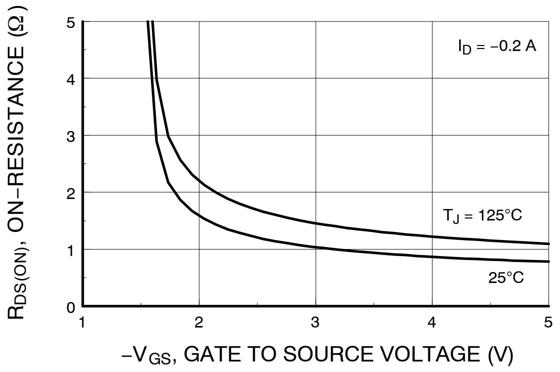


Figure 4. On−Resistance Variation with Gate−to−Source Voltage

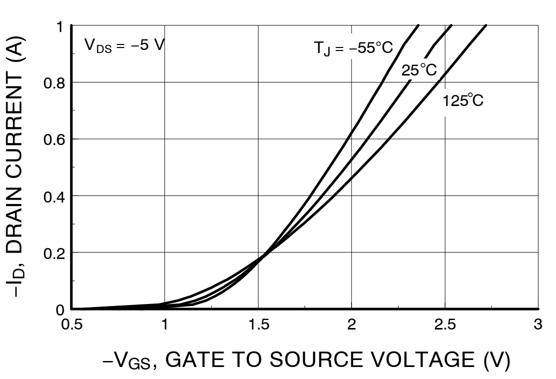


Figure 5. Transfer Characteristics

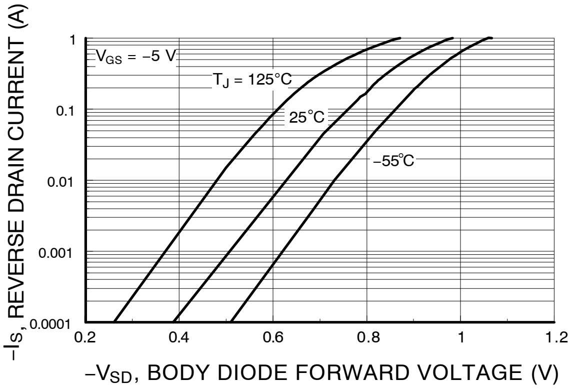


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

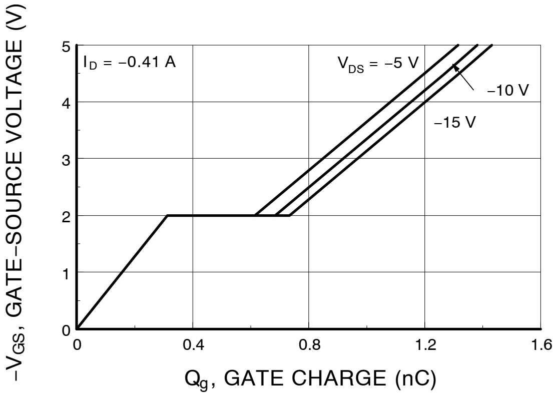


Figure 7. Gate Charge Characteristics

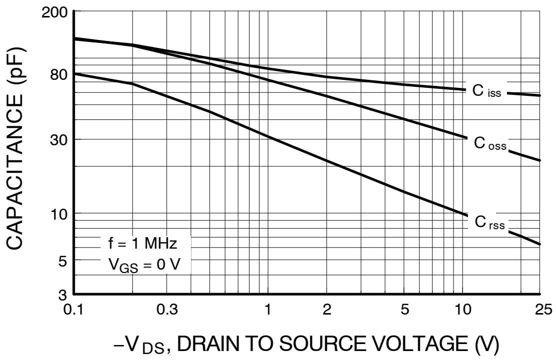


Figure 8. Capacitance Characteristics

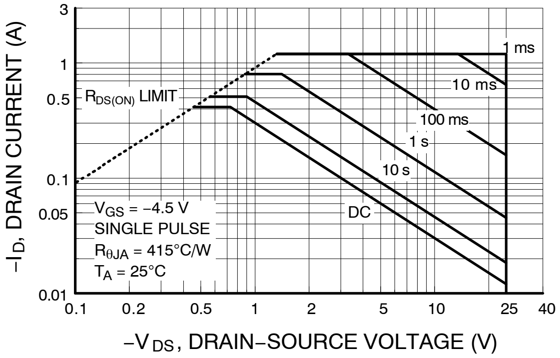


Figure 9. Maximum Safe Operating Area

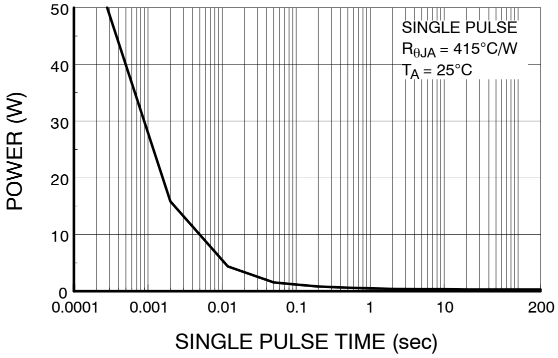
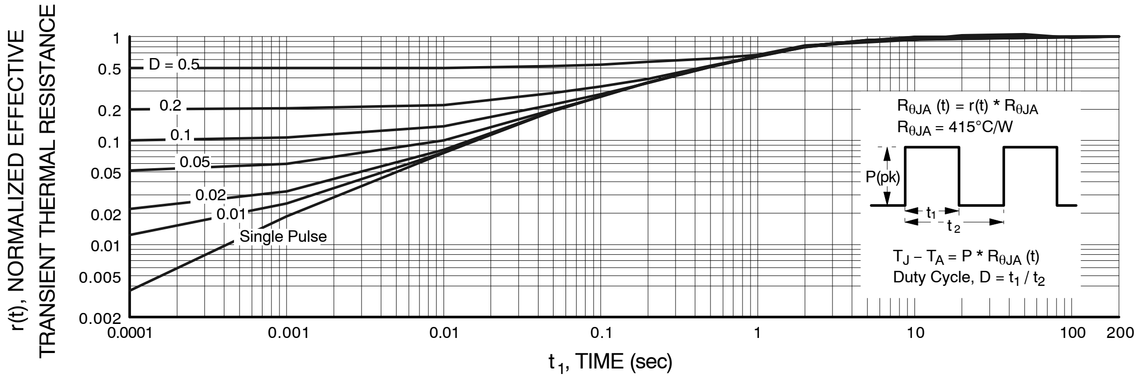


Figure 10. Single Pulse Maximum Power Dissipation



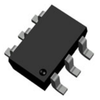
Thermal characterization performed using the conditions described in Note 1.
Transient thermal response will change depending on the circuit board design.

Figure 11. Transient Thermal Response Curve

ORDERING INFORMATION

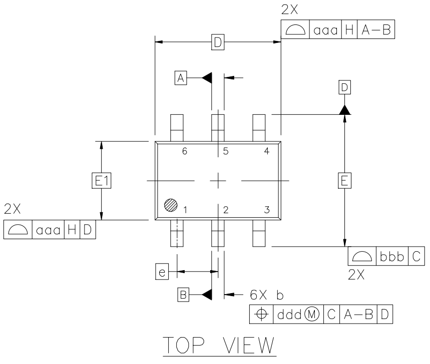
Device Order Number	Device Marking	Package Type	Shipping†
FDG6304P	04	SC−88/SC70−6/SOT−363 (Pb−Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



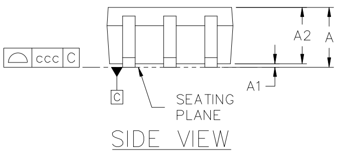
SC−88 2.00x1.25x0.90, 0.65P
CASE 419B−02
ISSUE Z

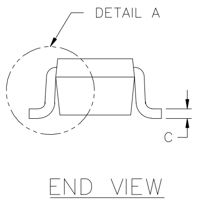
DATE 18 APR 2024

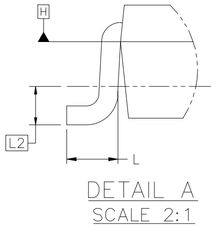


NOTES:

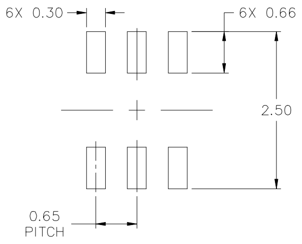
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.







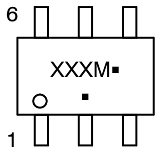
DIM	MILLIMETERS MIN.	NOM.	MAX.
A	−−−	−−−	1.10
A1	0.00	−−−	0.10
A2	0.70	0.90	1.00
b	0.15	0.20	0.25
c	0.08	0.15	0.22
D	2.00 BSC		
E	2.10 BSC		
E1	1.25 BSC		
e	0.65 BSC		
L	0.26	0.36	0.46
L2	0.15 BSC		
aaa	0.15		
bbb	0.30		
ccc	0.10		
ddd	0.10		



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42985B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SC−88 2.00x1.25x0.90, 0.65P**	**PAGE 1 OF 2**

SC−88 2.00x1.25x0.90, 0.65P
CASE 419B−02
ISSUE Z

DATE 18 APR 2024

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE 1
2. ANODE 2
3. ANODE 3
4. CATHODE 3
5. CATHODE 2
6. CATHODE 1

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 21:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. N/C
6. CATHODE 1

STYLE 22:
PIN 1. D1 (i)
2. GND
3. D2 (i)
4. D2 (c)
5. VBUS
6. D1 (c)

STYLE 23:
PIN 1. Vn
2. CH1
3. Vp
4. N/C
5. CH2
6. N/C

STYLE 24:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 25:
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 27:
PIN 1. BASE 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. EMITTER 2
6. COLLECTOR 2

STYLE 28:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 29:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE/ANODE
6. CATHODE

STYLE 30:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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