

# MOSFET – N-Channel, POWERTRENCH® 60 V

## FDD5612

### General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable  $R_{DS(ON)}$  specifications. The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.

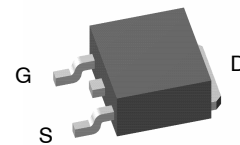
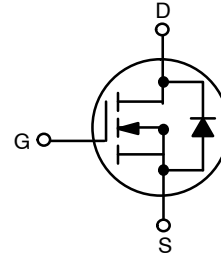
### Features

- 18 A, 60 V
  - ♦  $R_{DS(ON)} = 55 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$
  - ♦  $R_{DS(ON)} = 64 \text{ m}\Omega @ V_{GS} = 6 \text{ V}$
- Optimized for Use in High Frequency DC/DC Converters
- Low Gate Charge
- Very Fast Switching
- This Device is Pb-Free and are RoHS Compliant



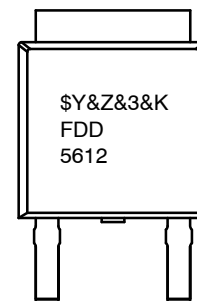
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**DPAK3 (TO-252 3 LD)  
CASE 369AS**

### MARKING DIAGRAM



\$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDD5612	= Specific Device Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# FDD5612

## ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C, Unless otherwise noted)

Symbol	Parameter	Ratings	Units	
V <sub>DSS</sub>	Drain–Source Voltage	60	V	
V <sub>GSS</sub>	Gate–Source Voltage	±20	V	
I <sub>D</sub>	Drain Current – Continuous	T <sub>C</sub> = 25°C	18	A
		T <sub>C</sub> = 100°C	13	
		T <sub>A</sub> = 25°C (Note 1a)	5.4	
		T <sub>A</sub> = 25°C (Note 1b)	3.5	
	Drain Current – Pulsed	100		
P <sub>D</sub>	Maximum Power Dissipation	T <sub>C</sub> = 25°C	42	W
		T <sub>C</sub> = 100°C	21	
		T <sub>A</sub> = 25°C (Note 1a)	3.8	
		T <sub>A</sub> = 25°C (Note 1b)	1.6	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	–55 to +175	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
R <sub>θJC</sub>	Thermal Resistance, Junction–to–Case	3.5	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction–to–Ambient (Note 1a)	40	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction–to–Ambient (Note 1b)	96	°C/W

## PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Device	Reel Size	Tape Width	Quantity
FDD5612	FDD5612	13"	16 mm	2500 Units

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### DRAIN–SOURCE AVALANCHE RATINGS (Note 1)

W <sub>DSS</sub>	Single Pulse Drain–Source Avalanche Energy	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 5.4 A			90	mJ
I <sub>AR</sub>	Maximum Drain–Source Avalanche Current				5.4	A

### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain–Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	60			V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = –250 μA, Referenced to 25°C		62		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 48 V, V <sub>GS</sub> = 0 V			1	μA
I <sub>GSSF</sub>	Gate–Body Leakage, Forward	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate–Body Leakage, Reverse	V <sub>GS</sub> = –20V, V <sub>DS</sub> = 0 V			–100	nA

### ON CHARACTERISTICS (Note 2)

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1	2.4	3	V
ΔV <sub>GS(th)</sub> / ΔT <sub>J</sub>	Gate Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C		–6		mV/°C

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## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>ON CHARACTERISTICS</b> (Note 2)						
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 10\text{ V}, I_D = 5.4\text{ A}$ $V_{GS} = 6\text{ V}, I_D = 5\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 5.4\text{ A}, T_J = 125^\circ\text{C}$		36 42 64	55 64 103	$\text{m}\Omega$
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	20			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 5.4\text{ A}$		15		S

## DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		660		pF
$C_{oss}$	Output Capacitance			79		pF
$C_{rss}$	Reverse Transfer Capacitance			36		pF

## SWITCHING CHARACTERISTICS (Note 2)

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 30\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		8	16	ns
$t_r$	Turn–On Rise Time			4	8	ns
$t_{d(off)}$	Turn–Off Delay Time			24	38	ns
$t_f$	Turn–Off Fall Time			4	8	ns
$Q_g$	Total Gate Charge	$V_{DS} = 30\text{ V}, I_D = 5.4\text{ A},$ $V_{GS} = 10\text{ V}$		7.5	11	nC
$Q_{gs}$	Gate–Source Charge			2.5		nC
$Q_{gd}$	Gate–Drain Charge			3		nC

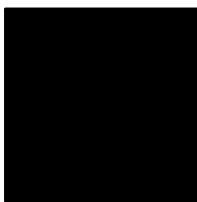
## DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

$I_S$	Source Current (Body Diode)	$T_C = 25^\circ\text{C}$			18	A
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.7\text{ A}$ (Note 2)		0.8	1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

### NOTES:

- $R_{\theta JA}$  is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the drain tab.  $R_{\theta JA}$  is the guaranteed design while  $R_{\theta JA}$  is determined by the user's design.  $R_{\theta JA}$  has been used to determine some of the maximum ratings.



- a)  $R_{\theta JA} = 40^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



- b)  $R_{\theta JA} = 96^\circ\text{C/W}$  when mounted on a  $0.076\text{ in}^2$  pad of 2 oz copper

- Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty Cycle < 2.0%

TYPICAL CHARACTERISTICS

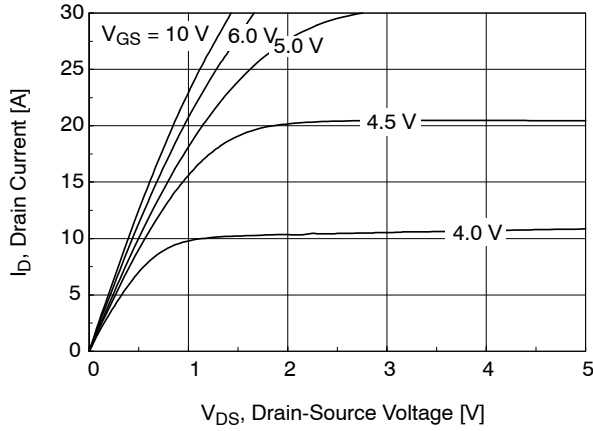


Figure 1. On-Region Characteristics

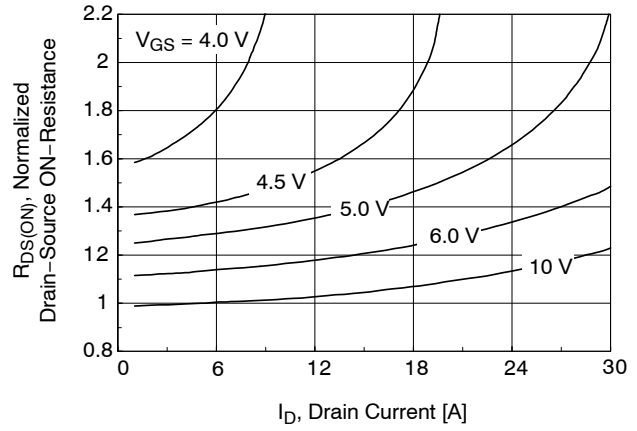


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

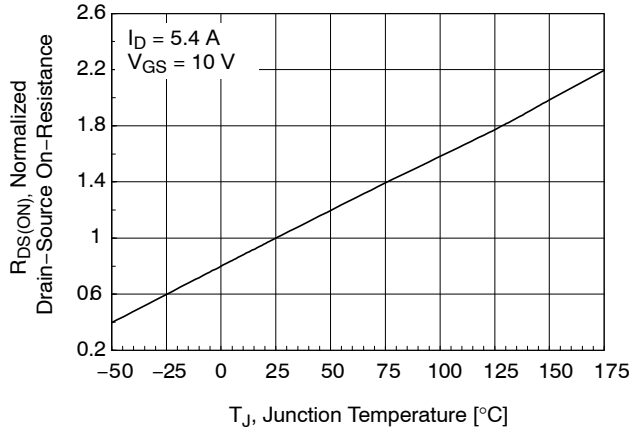


Figure 3. On-Resistance Variation with Temperature

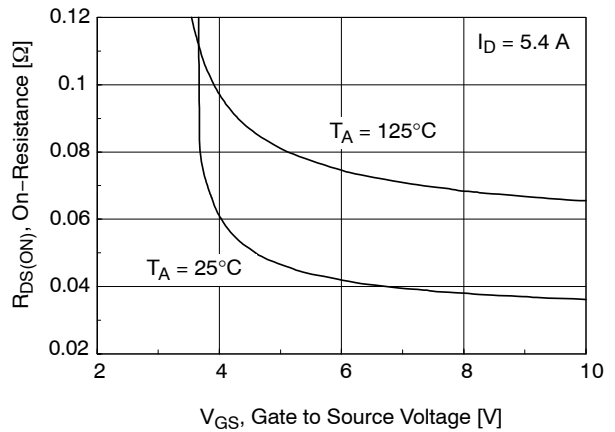


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

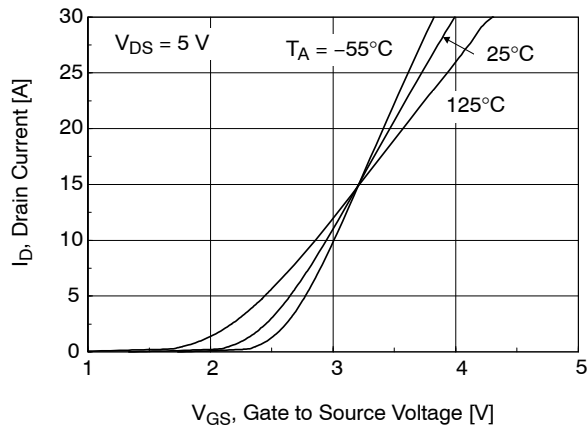


Figure 5. Transfer Characteristics

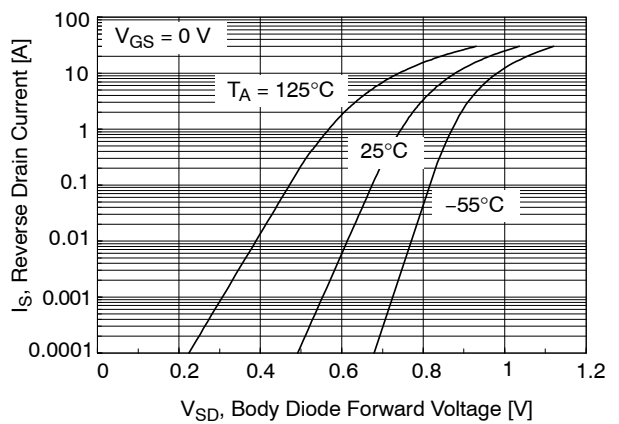


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS (continued)

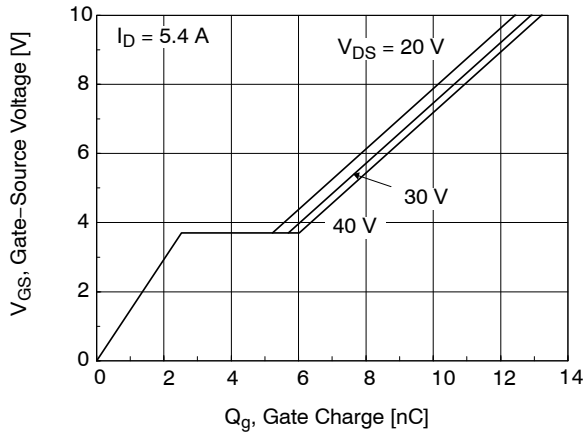


Figure 7. Gate Charge Characteristics

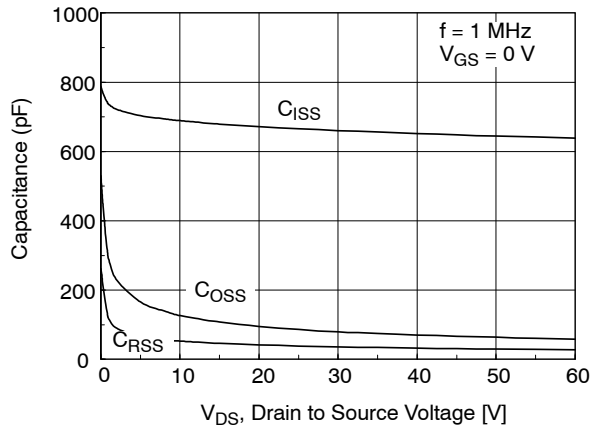


Figure 8. Capacitance Characteristics

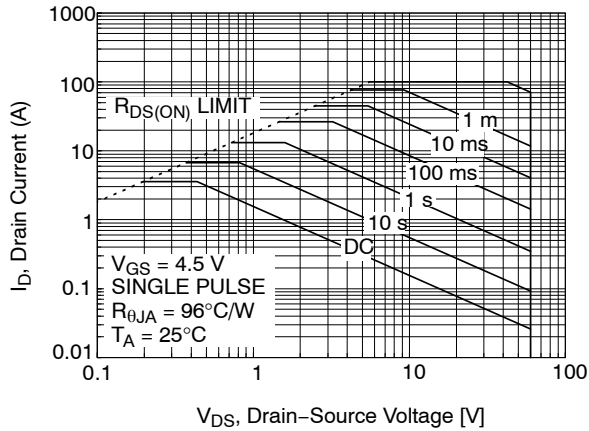


Figure 9. Maximum Safe Operating Area

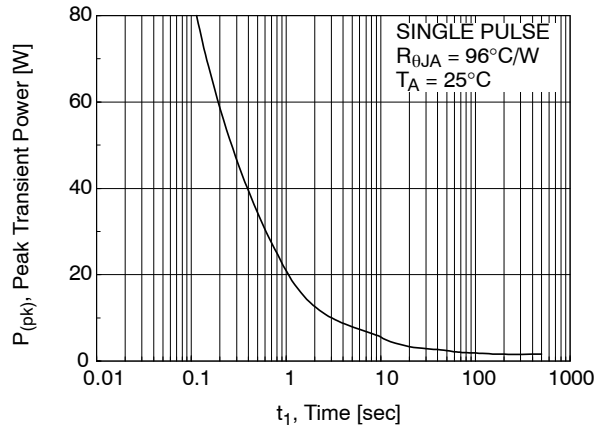


Figure 10. Single Pulse Maximum Power Dissipation

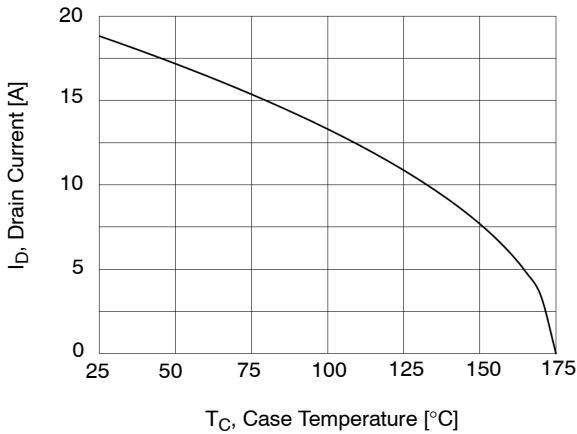
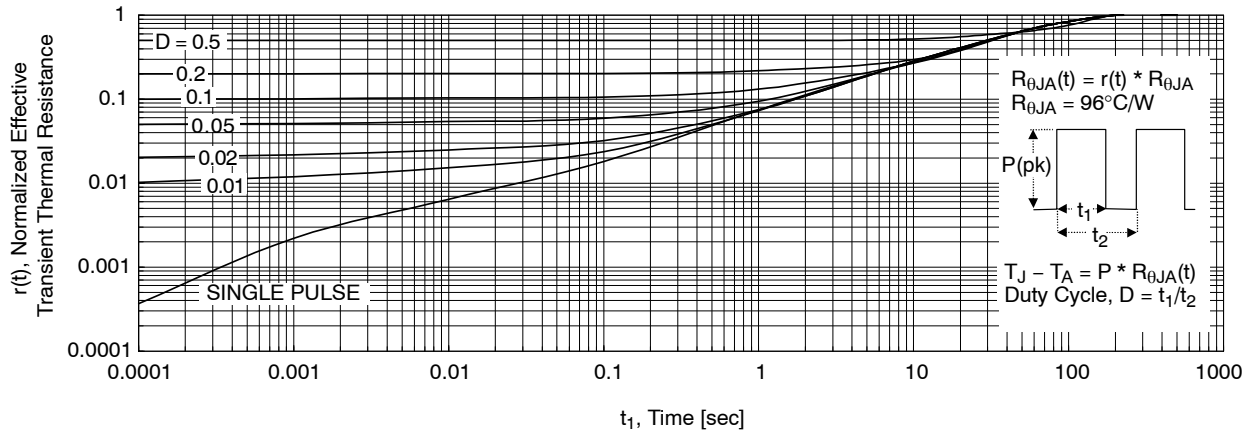


Figure 11. Maximum Drain Current vs. Case Temperature

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**Figure 12. Transient Thermal Response Curve**

**NOTES:**

3. Thermal characterization performed using the conditions described in Note 1b.
4. Transient thermal response will change depending on the circuit board design.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

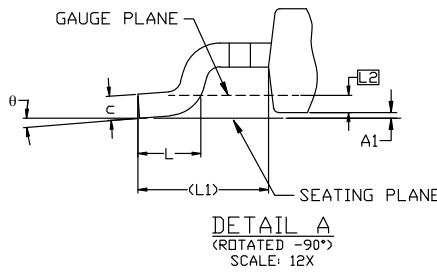


## DPAK3 6.10x6.54x2.29, 4.57P CASE 369AS ISSUE B

DATE 20 DEC 2023



- NOTES: UNLESS OTHERWISE SPECIFIED  
 A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE F, VARIATION AA.  
 B) ALL DIMENSIONS ARE IN MILLIMETERS.  
 C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2018.  
 D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.  
 E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX PLASTIC BODY STUB WITHOUT CENTER LEAD.  
 F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.  
 G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TD228P991X239-3N.



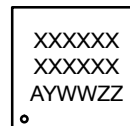
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.29	2.39
A1	0.00	-	0.127
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	5.21	5.34	5.46
c	0.45	0.53	0.61
c2	0.45	0.52	0.58
D	5.97	6.10	6.22
D1	5.21	---	---
E	6.35	6.54	6.73
E1	4.32	---	---
e	2.286 BSC		
e1	4.572 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	1.08	1.27
L4	---	---	1.02
$\theta$	0°	---	10°



### LAND PATTERN RECOMMENDATION

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

### GENERIC MARKING DIAGRAM\*



\*This information is generic. Please refer to device data sheet for actual part marking. Pb-free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

XXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ZZ = Assembly Lot Code

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<b>DESCRIPTION:</b>	<b>DPAK3 6.10x6.54x2.29, 4.57P</b>	<b>PAGE 1 OF 1</b>

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