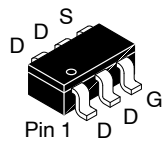
# MOSFET – Single, N-Channel, Logic Level, POWERTRENCH®

## 30 V, 6.3 A, 25 mΩ

# FDC655BN

| $V_{DSS}$ | $R_{DS(ON)}$ MAX | $I_D$ MAX |
|---|---|---|
| 30 V | 25 mΩ @ 10 V | 6.3 A |
| | 33 mΩ @ 4.5 V | |




**TSOT23 6−Lead**
**(SUPERSOT™ −6)**
**CASE 419BL**

### General Description

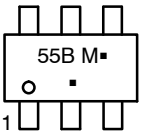
This N−Channel Logic Level MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that has been especially tailored to minimize the on−state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in−line power loss and fast switching are required.

### Features

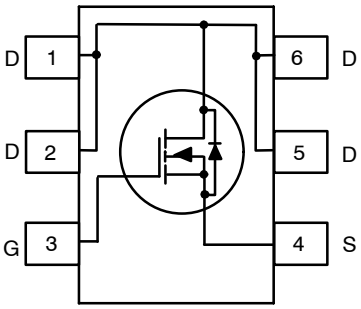
- Max $R_{DS(ON)}$ = 25 mΩ @ $V_{GS}$ = 10 V, $I_D$ = 6.3 A
- Max $R_{DS(ON)}$ = 33 mΩ @ $V_{GS}$ = 4.5 V, $I_D$ = 5.5 A
- Fast Switching
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{DS(ON)}$
- This Device is Pb−Free, Halide Free and is RoHS Compliant

### MARKING DIAGRAM




55B = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

### PIN ASSIGNMENT




### MOSFET MAXIMUM RATINGS ($T_C$ = 25°C, unless otherwise noted)

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | | 30 | V |
| $V_{GS}$ | Gate to Source Voltage | | ±20 | V |
| $I_D$ | −Continuous $T_A$ = 25°C | (Note 1a) | 6.3 | A |
| | −Pulsed | | 20 | |
| $P_D$ | Power Dissipation | (Note 1a) | 1.6 | W |
| | | (Note 1b) | 0.8 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | −55 to +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

| Symbol | Parameter | | Max | Unit |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | (Note 1a) | 78 | °C/W |

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| FDC655BN | TSOT23−6 (Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V, | 30 | – | – | V |
| $\Delta BV_{DSS}$ / $\Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25°C | – | 25 | – | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V | – | – | 1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | – | – | ±100 | nA |
| **ON CHARACTERISTICS** | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 1 | 1.9 | 3 | V |
| $\Delta V_{GS(th)}$ / $\Delta T_J$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25°C | – | –5 | – | mV/°C |
| $R_{DS(ON)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 6.3 A | – | 21 | 25 | mΩ |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 5.5 A | – | 26 | 33 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 6.3 A, $T_J$ = 125°C | – | 30 | 36 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 10 V, $I_D$ = 6.3 A | – | 35 | – | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V, f = 1 MHz | – | 470 | 620 | pF |
| $C_{oss}$ | Output Capacitance | | – | 100 | 130 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | – | 60 | 90 | pF |
| $R_g$ | Gate Resistance | | – | 3.0 | – | Ω |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD}$ = 15 V, $I_D$ = 1 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | – | 6 | 11 | ns |
| $t_r$ | Rise Time | | – | 2 | 10 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | – | 15 | 26 | ns |
| $t_f$ | Fall Time | | – | 2 | 10 | ns |
| $Q_{g(Tot)}$ | Total Gate Charge | $V_{GS}$ = 0 V to 10 V, $V_{DD}$ = 15 V, $I_D$ = 6.3 A | – | 9 | 13 | nC |
| $Q_{g(Tot)}$ | Total Gate Charge | $V_{GS}$ = 0 V to 5 V, $V_{DD}$ = 15 V, $I_D$ = 6.3 A | – | 5 | 7 | nC |
| $Q_{gs}$ | Gate to Source Charge | $V_{DD}$ = 15 V, $I_D$ = 6.3 A | – | 1.4 | – | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | | – | 1.6 | – | nC |
| **DRAIN–SOURCE DIODE CHARACTERISTICS** | | | | | | |
| $I_S$ | Maximum Continuous Drain–Source Diode Forward Current | | – | – | 1.3 | A |
| $V_{SD}$ | Source–Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 1.3 A (Note 2) | – | 0.8 | 1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 6.3 A, di/dt = 100 A/μs | – | 15 | 26 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | – | 4 | 10 | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.
   a. 78°C/W when mounted on a 1 $in^2$ pad of 2 oz copper on FR–4 board.
   b. 156°C/W when mounted on a minimum pad.
2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

## TYPICAL CHARACTERISTICS

($T_J$ = 25°C unless otherwise noted)

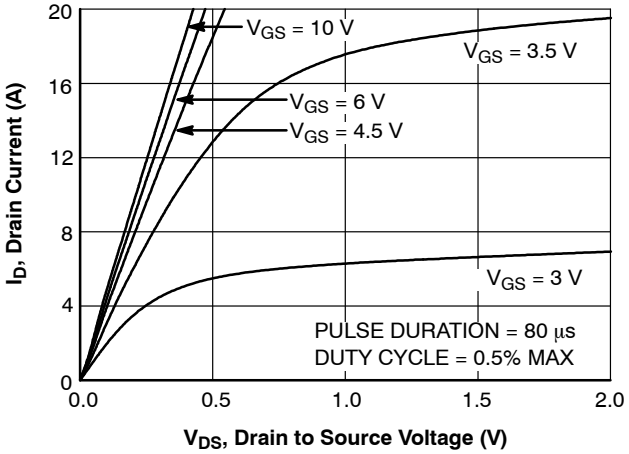



**Figure 1. On Region Characteristics**

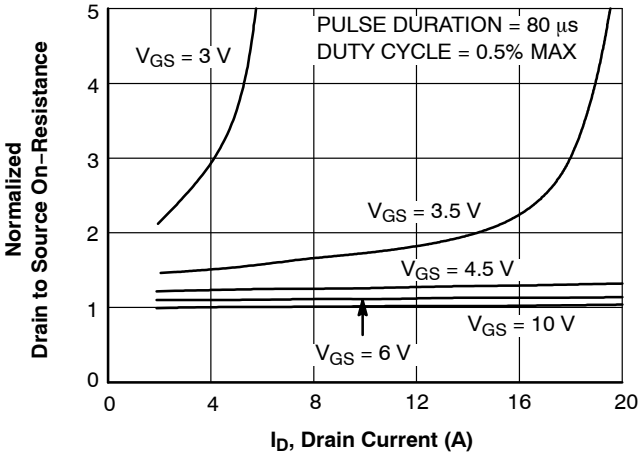



**Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage**

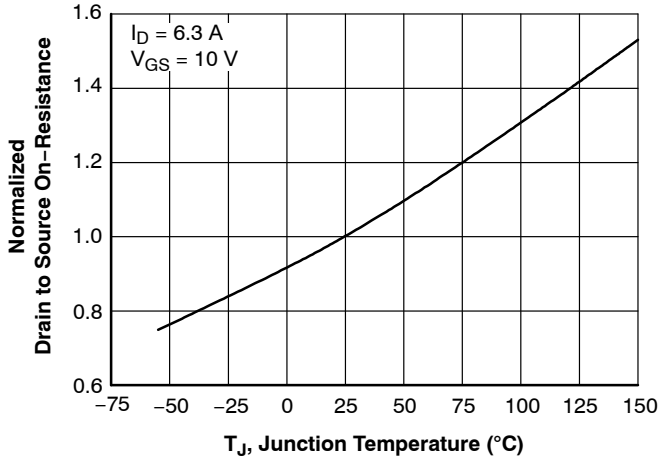



**Figure 3. Normalized On Resistance vs. Junction Temperature**

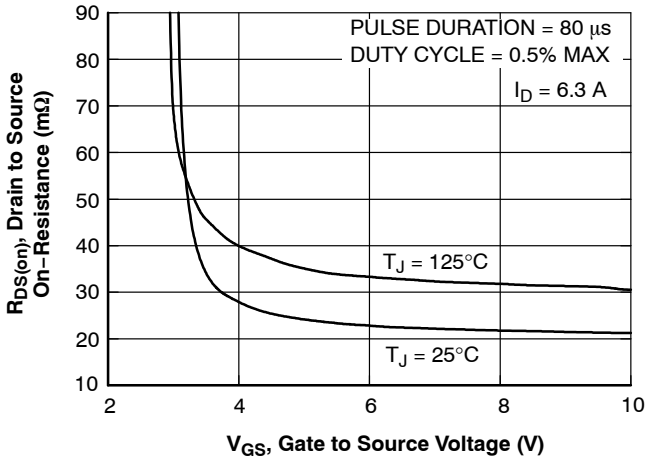



**Figure 4. On−Resistance vs. Gate to Source Voltage**

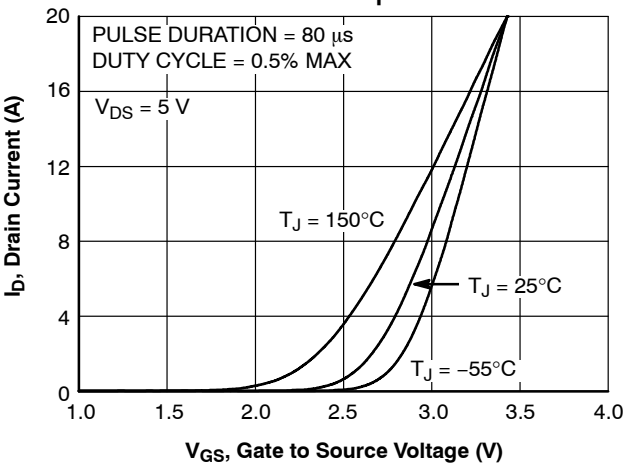



**Figure 5. Transfer Characteristics**

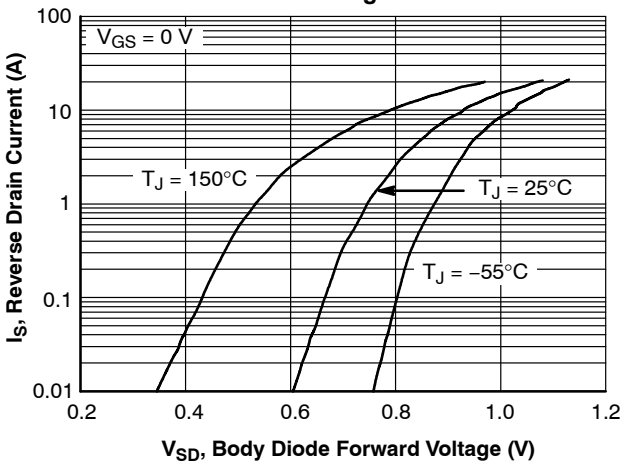



**Figure 6. Source to Drain Diode Forward Voltage vs. Source Current**

## TYPICAL CHARACTERISTICS (continued)

($T_J$ = 25°C unless otherwise noted)

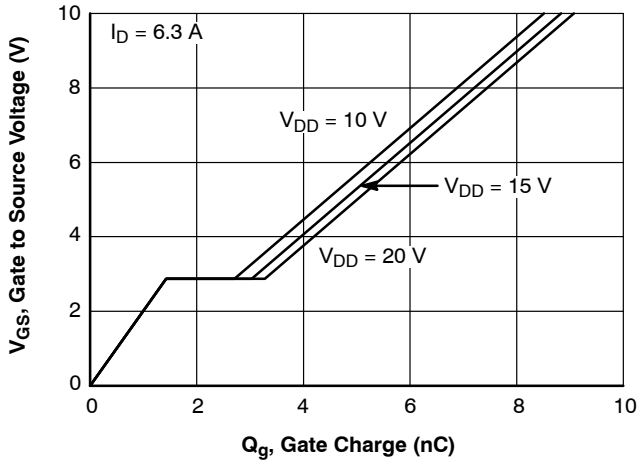



**Figure 7. Gate Charge Characteristics**

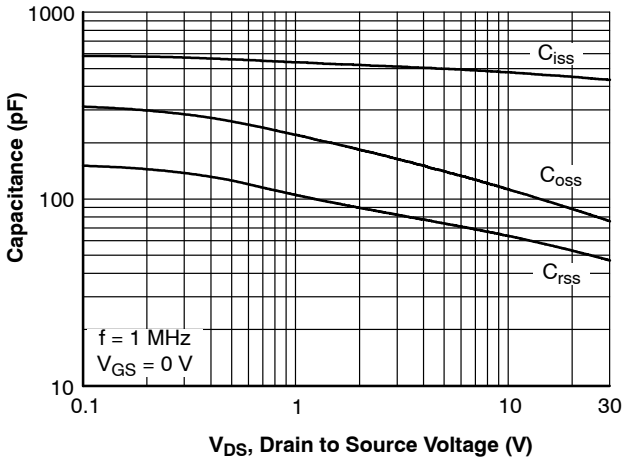



**Figure 8. Capacitance vs. Drain to Source Voltage**

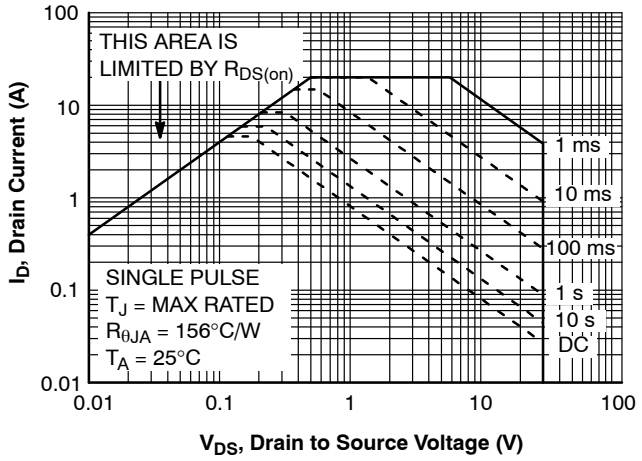



**Figure 9. Forward Bias Safe Operating Area**

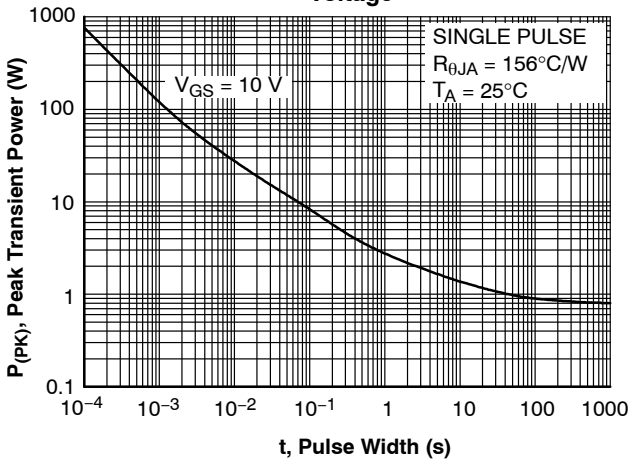



**Figure 10. Single Pulse Maximum Power Dissipation**

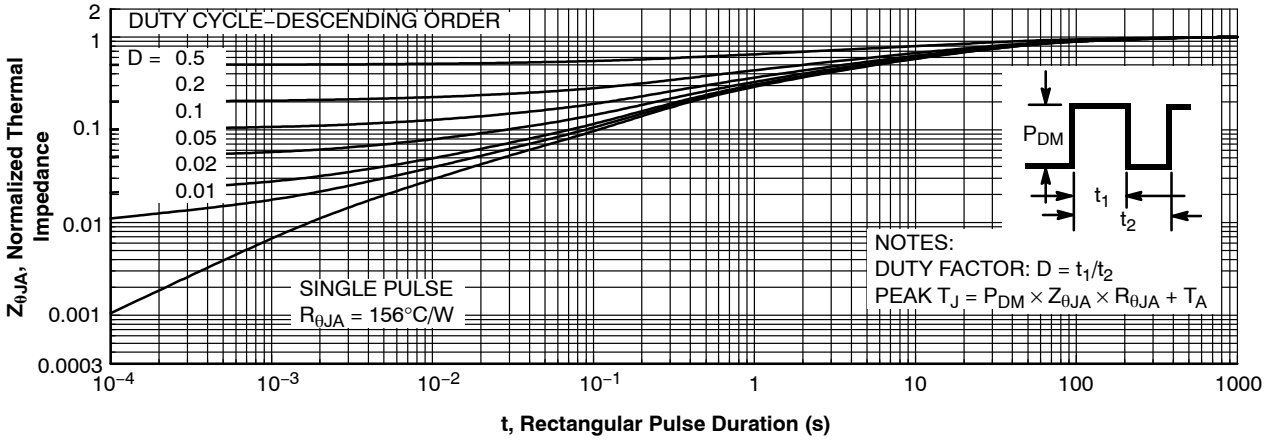



**Figure 11. Junction−to−Ambient Transient Thermal Response Curve**

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

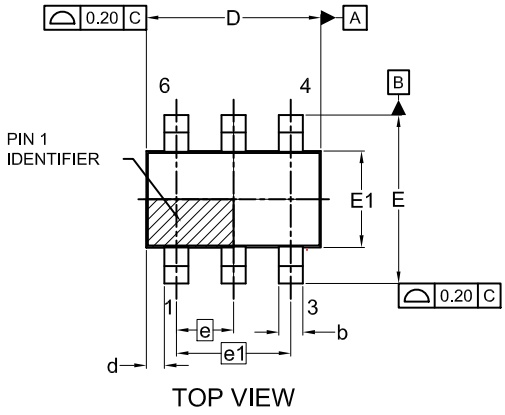
ON Semiconductor®

1

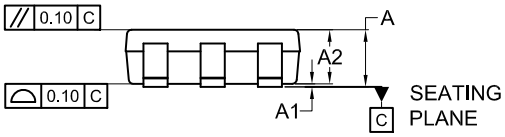
**SCALE 2:1**

**TSOT23 6−Lead**
CASE 419BL
ISSUE A

DATE 31 AUG 2020

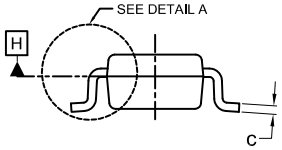



TOP VIEW

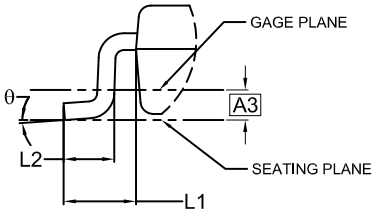



FRONT VIEW

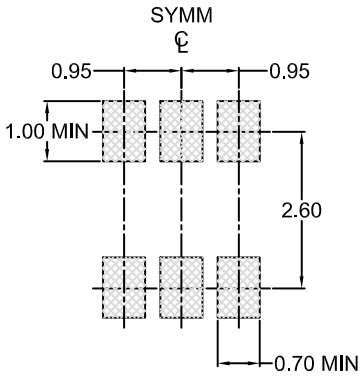
NOTE 4




SIDE VIEW




DETAIL A




LAND PATTERN
RECOMMENDATION

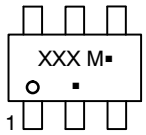
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.90 | 1.00 | 1.10 |
| A1 | 0.00 | 0.05 | 0.10 |
| A2 | 0.70 | 0.85 | 1.00 |
| A3 | | 0.25 BSC | |
| b | 0.25 | 0.38 | 0.50 |
| c | 0.10 | 0.18 | 0.26 |
| D | 2.80 | 2.95 | 3.10 |
| d | | 0.30 REF | |
| E | 2.50 | 2.75 | 3.00 |
| E1 | 1.30 | 1.50 | 1.70 |
| e | | 0.95 BSC | |
| e1 | | 1.90 BSC | |
| L1 | | 0.60 REF | |
| L2 | 0.20 | 0.40 | 0.60 |
| θ | 0° | --- | 10° |

**GENERIC MARKING DIAGRAM***




XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
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| **DESCRIPTION:** | **TSOT23 6−Lead** | **PAGE 1 OF 1** |

## ADDITIONAL INFORMATION

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**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT**: www.onsemi.com/support
**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales