

MOSFET - UniFET™, N-Channel

300 V, 28 A, 129 mΩ

FDB28N30TM

Description

UniFET MOSFET is **onsemi**'s high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on–state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

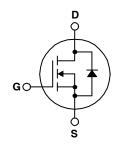
Features

- Typical $R_{DS(on)} = 108 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_D = 14 \text{ A}$
- Low Gate Charge (Typical Q_g = 39 nC)
- Low Reverse Transfer Capacitance C_{rss} (Typical $C_{rss} = 35 pF$)
- 100% Avalanche Tested
- This Device is Pb-Free and is RoHS Compliant

Applications

- Uninterruptible Power Supply
- AC-DC Power Supply

N-Channel





D²PAK-3 (TO-263, 3-LEAD) CASE 418AJ

MARKING DIAGRAM

O \$Y&Z&3&K FDB28N30

\$Y = **onsemi** Logo &Z = Assembly Plant Code &3 = Numeric Date Code &K = Lot Code

FDB28N30 = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

MOSFET MAXIMUM RATINGS ($T_C = 25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	300	V
V_{GSS}	Gate to Source Voltage	±30	V
Ι _D	Drain Current –Continuous (T _C = 25°C)	28	Α
	-Continuous (T _C = 100°C)	19	
I _{DM}	Drain Current -Pulsed (Note 1)	112	Α
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	588	mJ
I _{AR}	Avalanche Current (Note 1)	28	Α
E _{AR}	Repetitive Avalanche Energy (Note 1)	25	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P_{D}	Power Dissipation (T _C = 25°C)	250	W
	-Derate above 25°C	2.0	W/°C
TJ, T _{STG}	Operating and Storage Temperature Range	−55 to +150	°C
TL	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. Repetitive rating: pulse–width limited by maximum junction temperature 2. L = 1.5 mH, I_{AS} = 28 A, V_{DD} = 50 V, R_{G} = 25 Ω , starting T_{J} = 25°C 3. $I_{SD} \le$ 28 A, $I_{CD} \le$ 30 A/ μ s, $I_{CD} \le$ 8VDSS, starting $I_{CD} =$ 25°C

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Units
RеJC	Maximum Thermal Resistance, Junction to Case	0.5	°C/W
RθJA	Maximum Thermal Resistance, Junction to Ambient (1 in2 Pad of 2-oz Copper)	40	°C/W
Reja	Maximum Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper)	62.5	°C/W

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Shipping [†]		
FDB28N30TM	FDB28N30	D ² PAK-3 (TO-263, 3-LEAD) (Pb-Free)	800 units / Tape & Reel		

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
OFF CHAI	RACTERISTICS					
BV _{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μ A, V_{GS} = 0 V, T_J = 25°C	300			٧
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25°C		0.4		V/°C
I _{DSS}	Drain-to-Source Leakage Current	V _{DS} = 300 V, V _{GS} = 0 V			1	μΑ
		V _{DS} = 240 V, T _C = 125°C			10	
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA
ON CHAR	ACTERISTICS					
V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	3.0		5.0	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 14 A		0.108	0.129	Ω
g _F s	Forward Transconductance	V _{DS} = 40 V, I _D = 14 A		24.8		S
DYNAMIC	CHARACTERISTICS					
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz		1690	2250	pF
C _{oss}	Output Capacitance			305	405	pF
C _{rss}	Reverse Transfer Capacitance			35	50	pF
Qg	Total Gate Charge at 10 V	V _{DS} = 240 V, I _D = 28 A, V _{GS} = 10 V		39	50	nC
Q _{gs}	Gate to Source Gate Charge	(Note 4)		12		nC
Q_{gd}	Gate to Drain "Miller" Charge			17		nC
SWITCHIN	IG CHARACTERISTICS					
t _{d(on)}	Turn-On Delay Time	V_{DD} = 150 V, I_D = 28 A, V_{GS} = 10V, R_G = 25 Ω		35	80	ns
t _r	Turn-On Rise Time	(Note 4)		135	280	ns
t _{d(off)}	Turn-Off Delay Time			79	168	ns
t _f	Turn-Off Fall Time			69	148	ns
DRAIN-SC	OURCE DIODE CHARACTERIST	ics				
I _S	Maximum Continuous Drain to Source Diode Forward Current				28	А
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current				112	А
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 28 A			1.4	٧
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 28 A, dI _F /dt = 100 A/μs		279		ns
Q _{rr}	Reverse Recovery Charge			2.7		μС

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

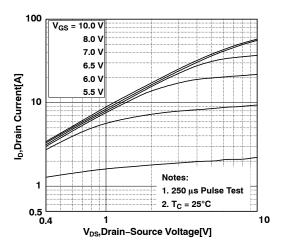


Figure 1. On-Region Characteristics

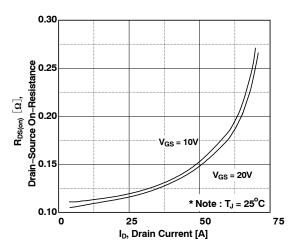


Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

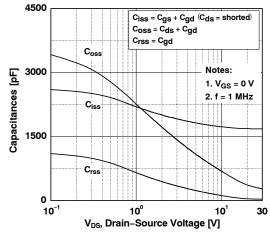


Figure 5. Capacitance Characteristics

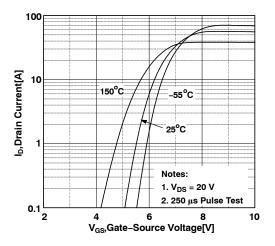


Figure 2. Transfer Characteristics

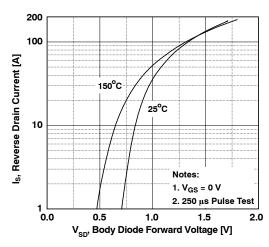


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

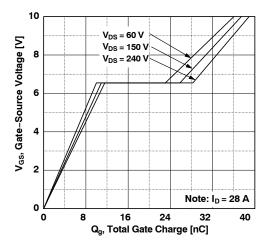


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

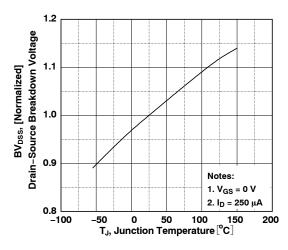


Figure 7. Breakdown Voltage Variation vs. Temperature

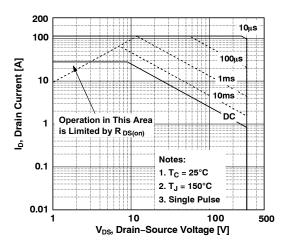


Figure 9. Maximum Safe Operating Area

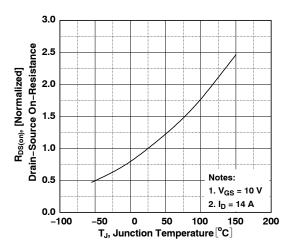


Figure 8. On–Resistance Variation vs.
Temperature

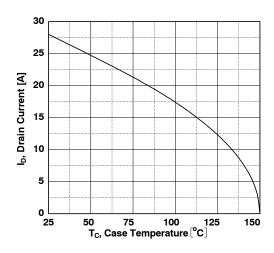


Figure 10. Maximum Drain Current vs. Case Temperature

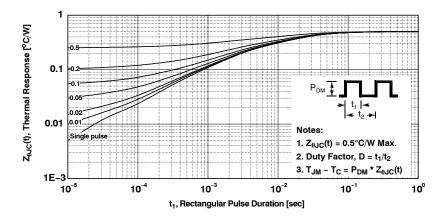


Figure 11. Transient Thermal Response Curve

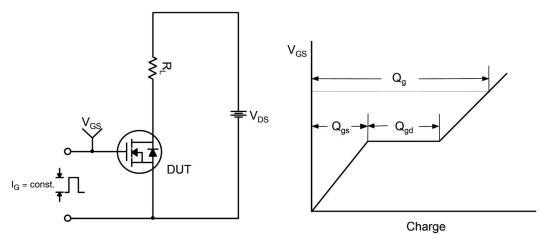


Figure 12. Gate Charge Test Circuit & Waveform

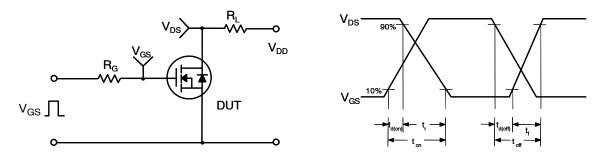


Figure 13. Resistive Switching Test Circuit & Waveform

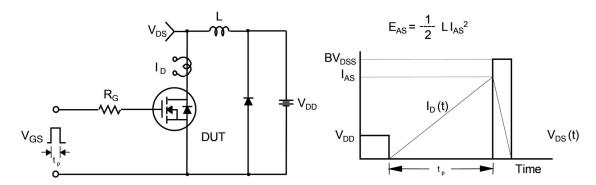
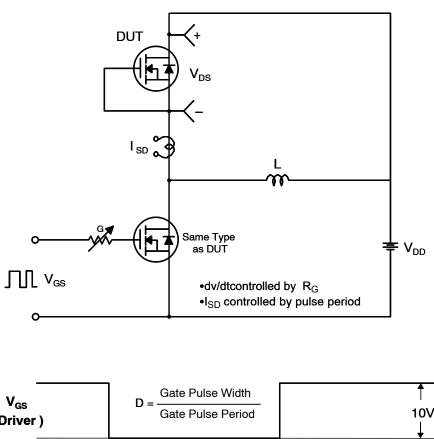


Figure 14. Unclamped inductive Switching Test Circuit & Waveform



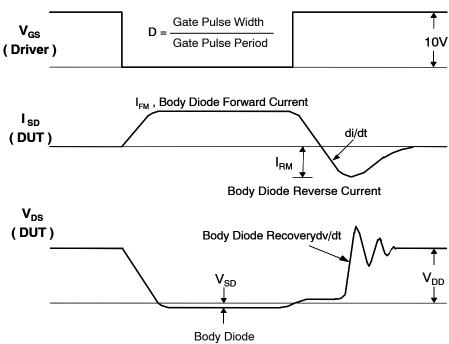


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveform

Forward Voltage Drop

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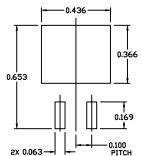




D²PAK-3 (TO-263, 3-LEAD) CASE 418AJ

ISSUE F

DATE 11 MAR 2021



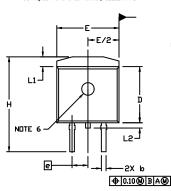
RECOMMENDED
MOUNTING FOOTPRINT

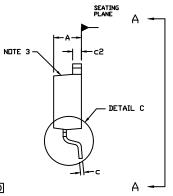
 For additional information on our Pb-Free strategy and soldering details, please downloa the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SDL DERRIV/D.

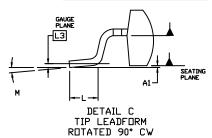
NOTES

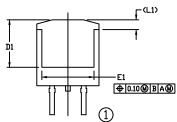
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- 2. CONTROLLING DIMENSION: INCHES
- 3. CHAMFER OPTIONAL
- I. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE DUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
- 5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
- 6. OPTIONAL MOLD FEATURE.
- 7. ①,② ... OPTIONAL CONSTRUCTION FEATURE CALL DUTS.

	INCHES		MILLIMETERS	
DIM	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
ھ	0.020	0.039	0.51	0.99
u	0.012	0.029	0.30	0.74
5	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260		6.60	
E	0.380	0.420	9.65	10.67
E1	0.245	-	6.22	
e	0.100 BSC		SSC 2.54 BSC	
Ξ	0.575	0.625	14.60	15.88
٦	0.070	0.110	1.78	2.79
L1		0.066		1.68
L2		0.070		1.78
L3	0.010 BSC		0.25 BSC	
М	0*	8*	0*	8*

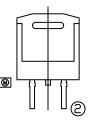


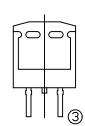


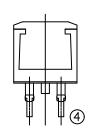




VIEW A-A







VIEW A-A

OPTIONAL CONSTRUCTIONS

XXXXXX = Specific Device Code

A = Assembly Location

WL = Wafer Lot Y = Year

WW = Work Week

W = Week Code (SSG)

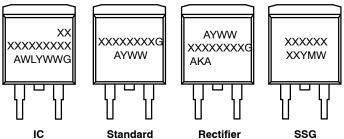
M = Month Code (SSG)

G = Pb-Free Package

AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " •", may or may not be present. Some products may not follow the Generic Marking.

GENERIC MARKING DIAGRAMS*



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DESCRIPTION:

D²PAK-3 (TO-263, 3-LEAD)

PAGE 1 OF 1

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