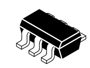
FAN6250M6X

Secondary Side Synchronous Rectifier Controller for Flyback Converters

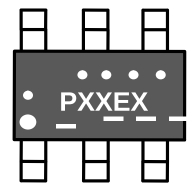
ON Semiconductor®

www.onsemi.com



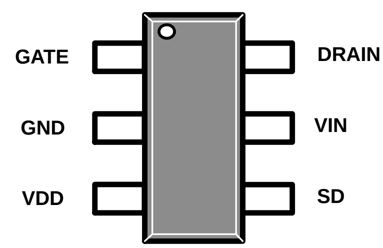
SOT−23, 6 Lead
CASE 527AJ

MARKING DIAGRAM



...	= Year Code
PXX	= 250 : FAN6250
E X	= Die Run Code
−−−	= Date Code

PIN CONNECTIONS



Description

The FAN6250M6X is a secondary−side synchronous rectifier (SR) controller for an isolated flyback converter operating in Discontinuous Conduction Mode (DCM). The adaptive dead time control algorithm minimizes the body diode conduction of SR MOSFET while guaranteeing stable and robust SR operation against noise and disturbance caused by the circuit parasitic.

Programmable thermal Shut−Down (SD) function that is informing primary side controller to shut−down the power system when pairing with PSR controller − FAN1080. The Dynamic Response Enhancement (DRE) function that minimizes system response time when pairing with PSR controller − FAN1080.

Features

- Works in Discontinuous Conduction Modes (DCM) and Boundary Conduction Modes (BCM)
- Adaptive Turn−off Trigger Blanking Time for Wide SR MOSFET Application
- Gate Turn−on Blanking Time (minimum Gate OFF Time)
- Dynamic Response Enhancement (DRE) Function that minimizes System Response Time
- Programmable Shut−Down (SD) Protection
- Minimum Turn−on Delay (20 ns)
- Input Voltage (VIN) Range for LDO Input: 3.25 V to 20 V
- Fewest External Components Allowed
- Accurate Turn Off Dead Time Regulation when working with PSR Power System
- Small Footprint: SOT−23 6 Pin
- This is a Pb−Free Device

Typical Applications

- Travel Adapter for Smart Phones, Feature Phones, and Tablet PCs
- AC−DC Adapters for Portable Devices that Require CV/CC Control

ORDERING INFORMATION

Part Number	Operating Temperature	Package	Packing Method†
FAN6250M6X	−40°C to 125°C	6 Lead, SOT23 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

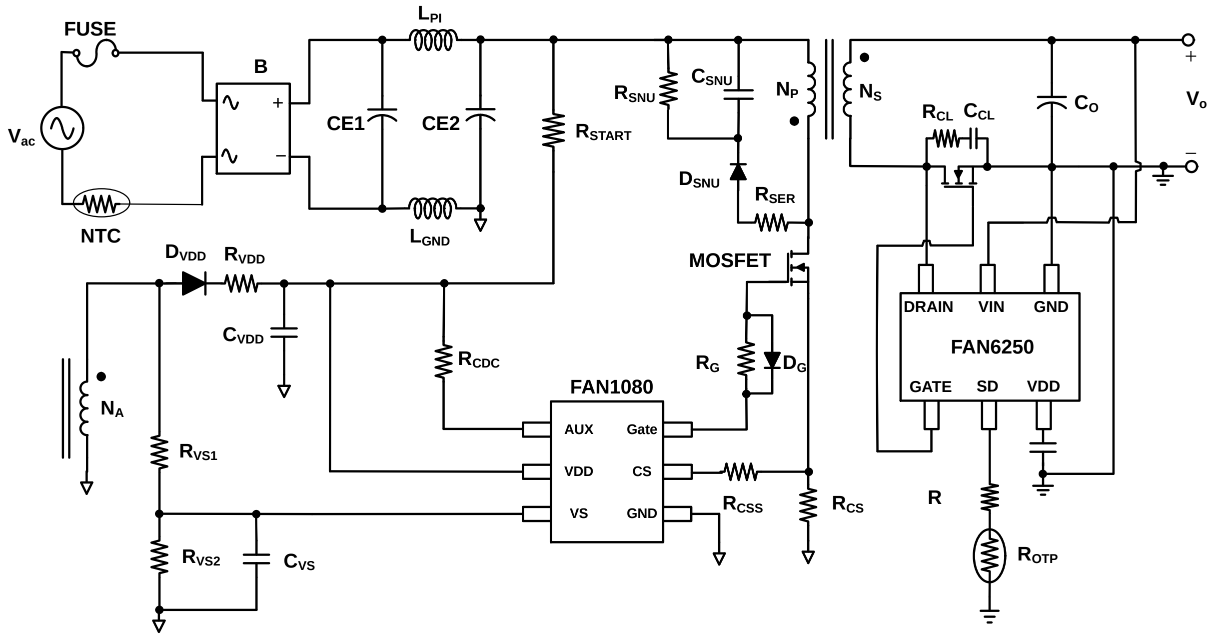


Figure 1. FAN6250 Typical Application Schematic

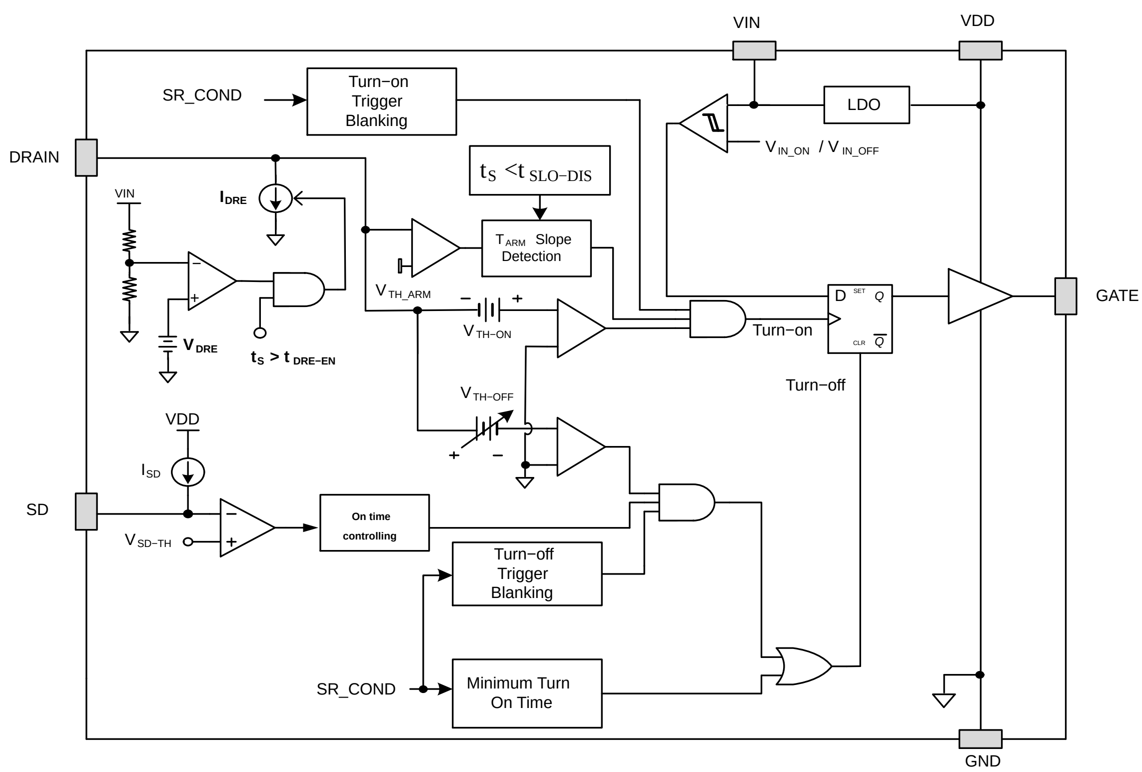


Figure 2. FAN6250 Function Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin #	Name	Description
1	GATE	Gate drive output
2	GND	Ground
3	VDD	Internal regulator 5 V output and gate drive power supply. Bypass with a 1uF capacitor to GND.
4	SD	Shut−Down pin. This pin is implemented for external over−temperature−protect by connecting the NTC thermistor.
5	VIN	Input Voltage Pin. This pin is connected to the output of the adaptor to monitor its output voltage and supply internal bias. IC operating current and MOSFET gate drive current is supplied through this pin.
6	DRAIN	Synchronous rectifier drain sense input.

Table 2. ABSOLUTE MAXIMUM RATINGS (Notes 1, 2, 3)

Parameter		Symbol	Value	Unit
Power Supply Input Pin Voltage		V_{IN}	−0.3 to 20	V
Internal Regulator Output Pin Voltage		V_{DD}	−0.3 to 6.5	V
Drain Sense Input Pin Voltage		V_{DRAIN}	−1 to 65	V
Gate Drive Output Pin Voltage		V_{GATE}	−0.3 to 6.5	V
Shut−Down Pin Voltage		V_{SD}	−0.3 to 6.5	V
Sense Pin Voltage		V_{SNS}	−0.3 to 6.5	V
Power Dissipation (T_A = 25°C)		P_D	0.446	W
Operating Junction Temperature		T_J	−40 to 125	°C
Storage Temperature Range		T_{STG}	−60 to 150	°C
Lead Temperature (Soldering) 10 Seconds		T_L	260	°C
Electrostatic Discharge Capability	Charged Device Model (CDM)	ESD	> 0.5	kV
	Human Body Model (HBM)		> 2	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. All voltage values, except differential voltages, are given with respect to the GND pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
3. Meets JEDEC standards JS−001−2012 and JESD 22−C101.

Table 3. THERMAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Min	Unit
Junction−to−Ambient Thermal Impedance	θ_{JA}	218.2	°C/W
Junction−to−Top Thermal Impedance	θ_{JT}	31.3	°C/W

Table 4. RECOMMENDED OPERATING RANGES

Parameter	Symbol	Min	Max	Unit
Drain Pin Voltage	V_{DRAIN}		60	V
VDD Pin Voltage	V_{DD}	3.1	5.5	V
VIN Pin Voltage	V_{IN}	3.25	20	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. ELECTRICAL CHARACTERISTICS
V_{IN} = 5.5 V and T_A = −40 to 125°C unless noted otherwise

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
VDD Section						
Turn−On Threshold	V_{IN} rising	V_{IN-ON}	3.06	3.15	3.25	V
Turn−Off Threshold	V_{IN} falling	V_{IN-OFF}	2.78	2.9	3.05	V
Operating Current	f_{SW} = 100 kHz, C_{GATE} = 3.3 nF, V_{IN} = 5 V	I_{IN-OP}		2.0	2.8	mA
Power Supply Section						
Internal LDO Output Voltage	V_{IN} = 20 V	V_{DD}	5.0	5.25	5.5	V
Dropout Voltage of LDO	I_{OUT} = 10 mA, V_{IN} = 3.3 V	V_{DO}			0.3	V
Drain Voltage Sensing Section						
Comparator Input Offset Voltage	Internal design suggestion	V_{OSI}(4)	−1	0	1	mV
Turn−On Threshold Voltage	R_{DRAIN} = 0 Ω (includes comparator input offset voltage)	V_{TH-ON}	−250	−200	−150	mV
Slope detection disable criteria		$t_{SLO-DIS}$(6)	53	58	63	μs
Slope detection disable criteria Hysteresis		$t_{SLO-HYS}$(4)		8		μs
Turn on delay	With 50 mV overdrive From V_{TH_ON} to Gate > 1 V	t_{ON-DLY}(4)		20		ns
Turn−Off Threshold Tuning Range 1		V_{TH-OFF}	−5		5	mV
Comparator delay for $V_{TH.OFF1}$	With 0mV overdrive From V_{TH_OFF} to Gate = 1 V	$t_{OFF-DLY}$(4)		20		ns
Gate Re−arming threshold	VIN = 5 V (Typically 0.7V_{DD})	V_{TH-ARM}	3.3	3.5	3.7	V
Gate Re−arming time for slope detection		t_{ARM}(4)	70	85	100	ns
Slope detection high threshold		V_{TH-HGH}(4)	0.4	0.5	0.6	V
Minimum On−Time and Minimum OFF−time Section						
Minimum On−Time		t_{ON-MIN}	2.16	2.4	2.64	μs
Minimum On−Time Upper at light load		$t_{ON-MIN-L}$	1.50	1.65	1.80	μs
Minimum t_{ON} cycles during start−up		$N_{ON-MIN-ST}$		3		cycles
Minimum Off−Time		$t_{OFF-MIN-L}$(5)	1.53	1.70	1.87	μs
Minimum Off−Time at light load (t_S > $t_{SLO-DIS}$)		$t_{OFF-MIN-H}$(5)	3.6	4	4.4	μs
Dead Time Control Section						
Dead time self−tuning target	From GATE OFF to V_{DRAIN} rising above 0.5 V	t_{DEAD}(4)	170	200	230	ns
DRE Section						
VIN pin DRE function trigger level		V_{DRE}(5)	4.68	4.78	4.85	V
Threshold voltage for DRE function		V_{DREI}	1.188	1.200	1.212	V
Drain Pin sinking current period when DRE triggered		t_{DREI}(4)	1.2	1.5	1.8	μs
DRE function enable period		t_{DRE-EN}	64	72	80	μs
IDRE re−arm period		t_{RE-ARM}		4		μs
Drain Pin sinking current when DRE triggered		I_{DRE}	50			mA

Table 5. ELECTRICAL CHARACTERISTICS (continued)
V_{IN} = 5.5 V and T_A = −40 to 125°C unless noted otherwise

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Shut−Down Section						
Threshold voltage for Shut−Down function triggered		V_{SD-TH}	0.97	1.00	1.03	V
Shut−Down current source		I_{SD-TH}	44	50	56	μA
Impedance for Shut−Down trigger		Z_{SD-TH}	18.48	20.00	21.68	kΩ
Denounce Cycles for Shut−Down		$N_{SD-Debounce}$		7		Cycles
Output Driver Section						
Output Voltage Low	V_{IN} = 6 V	V_{OL}			0.25	V
Output Voltage High	V_{IN} = 6 V	V_{OH}	4.9			V
Rise Time	V_{IN} = 6 V, C_L = 3300 pF, GATE = 1 V ~ 4 V	t_R			90	ns
Fall Time	V_{IN} = 6 V, C_L = 3300 pF, GATE = 4 V ~ 1 V	t_F			30	ns

4. Guaranteed by Design.
5. Specification operation temperature range −5°C ~ 85°C
6. Specification operation temperature range −5°C ~ 50°C

TYPICAL PERFORMANCE CHARACTERISTICS

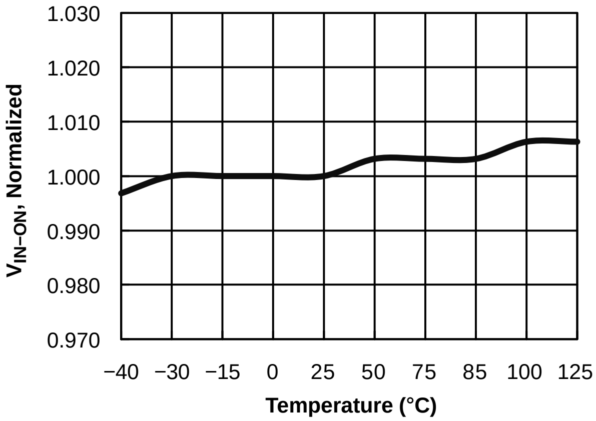


Figure 3. Turn−On Threshold Voltage (V_{IN-ON}) vs. Temperature

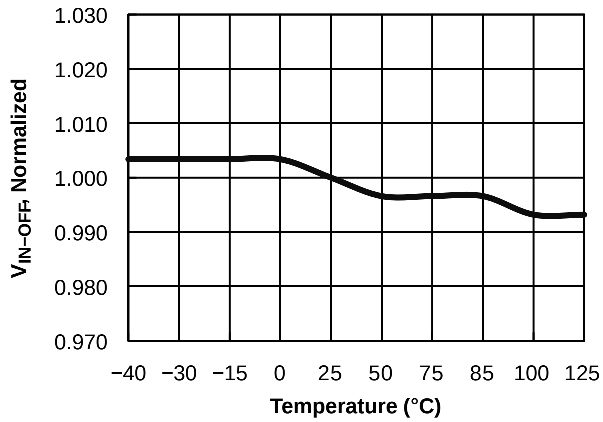


Figure 4. Turn−Off Threshold Voltage (V_{IN-OFF}) vs. Temperature

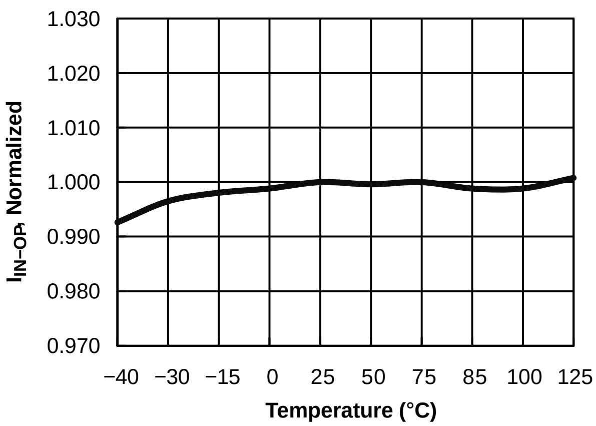


Figure 5. Operating Supply Current (I_{IN-OP}) vs. Temperature

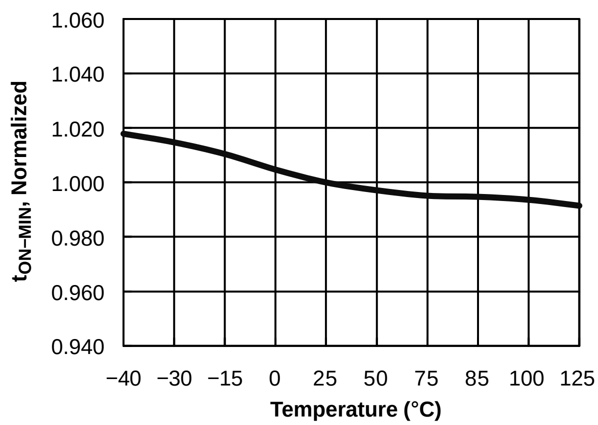


Figure 6. Minimum On Time (t_{ON-MIN}) vs. Temperature

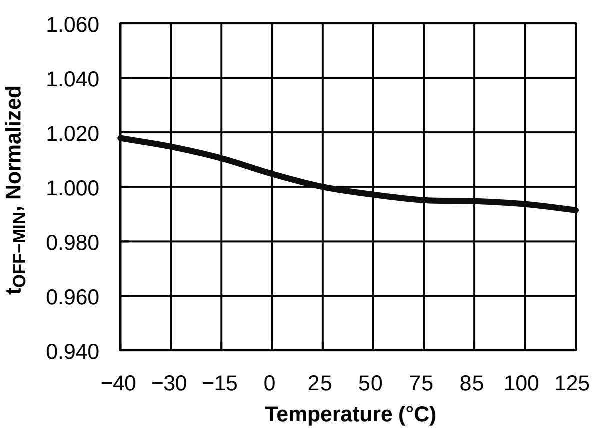


Figure 7. Minimum Gate Turn Off Time ($t_{OFF-MIN}$) vs. Temperature

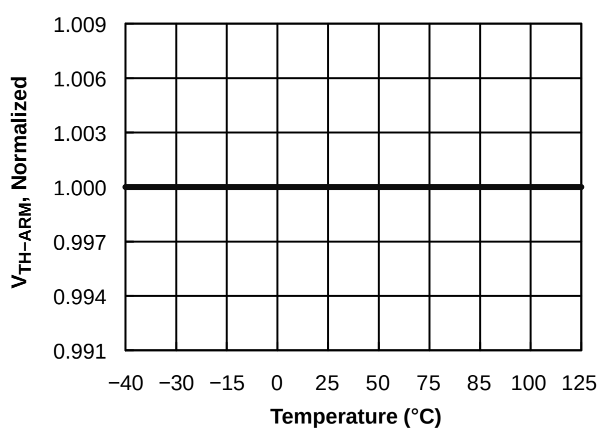


Figure 8. Gate Turn On Threshold Voltage (V_{TH-ARM}) vs. Temperature

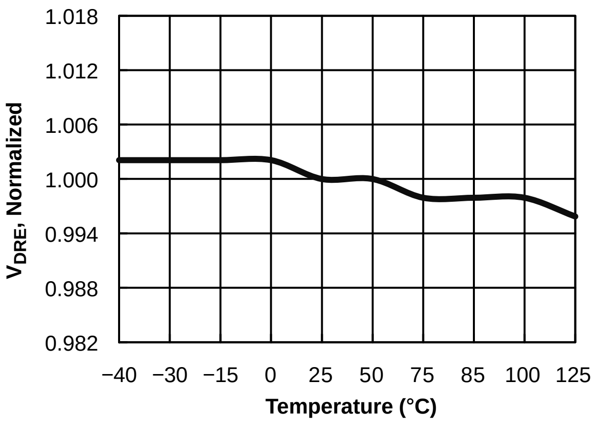


Figure 9. VIN Pin DRE Function Trigger Level (V_{DRE}) vs. Temperature

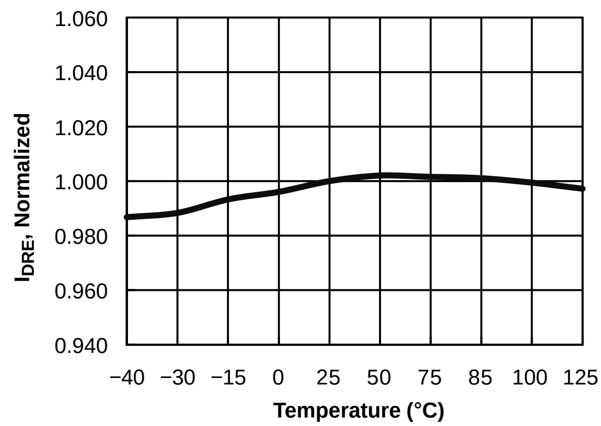


Figure 10. Drain Pin Sinking Current for DRE Triggered (I_{DRE}) vs. Temperature

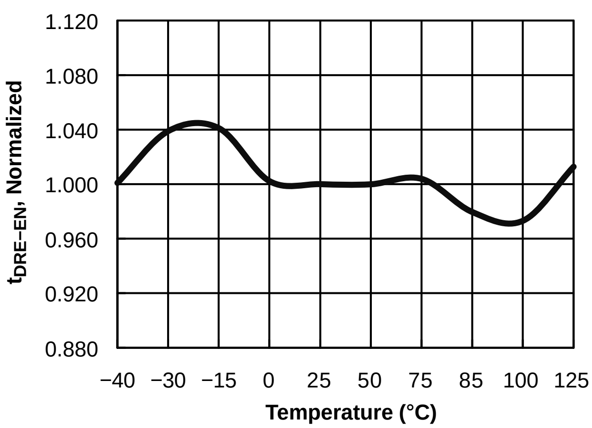


Figure 11. DRE Function Enable Period (t_{DRE-EN}) vs. Temperature

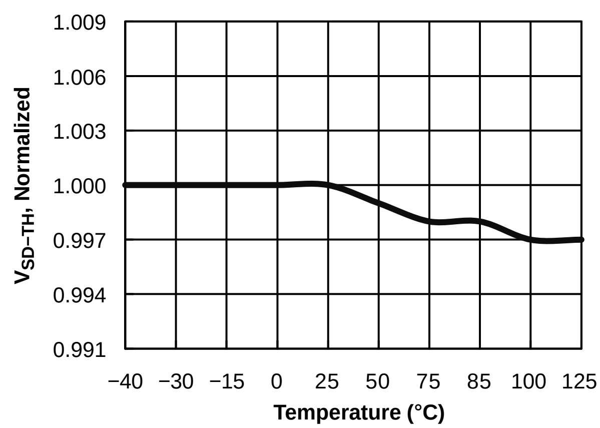


Figure 12. Shut−Down Threshold Voltage (V_{SD-TH}) vs. Temperature

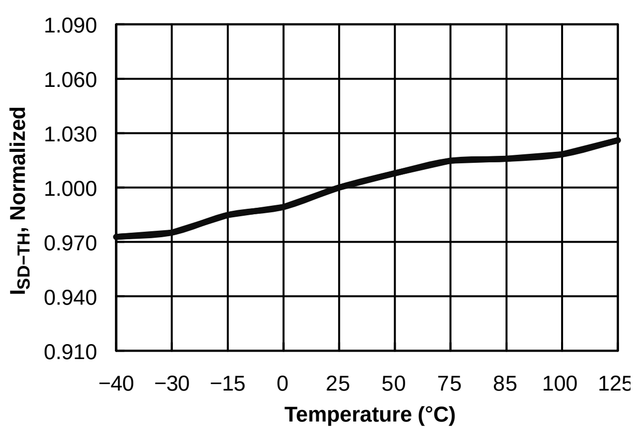


Figure 13. Shut−Down Current Source (I_{SD-TH}) vs. Temperature

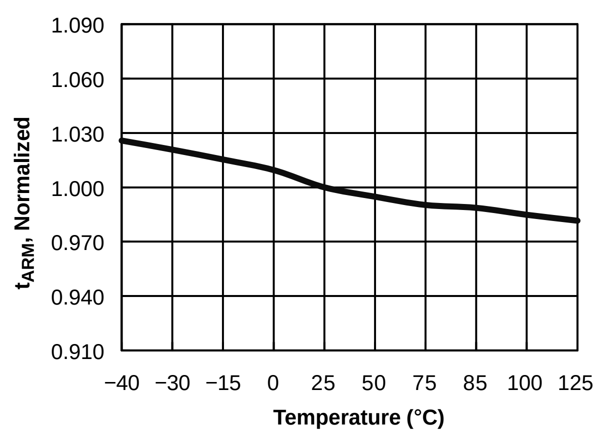
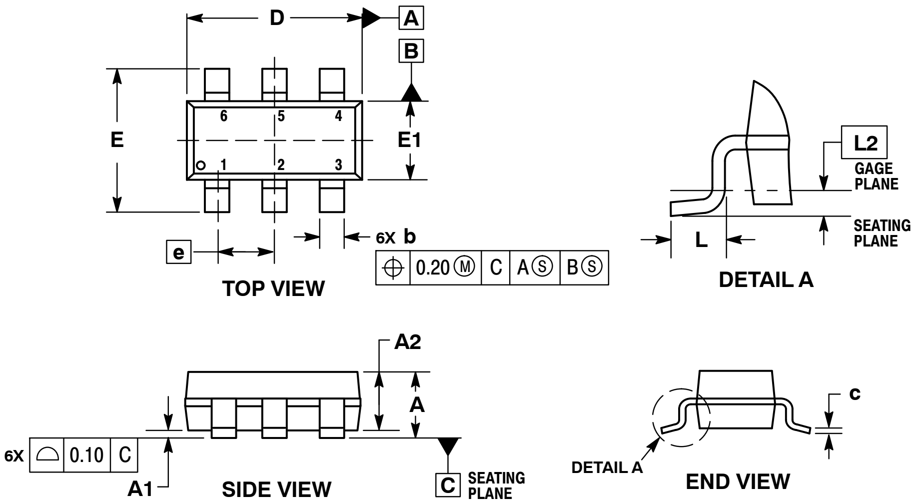


Figure 14. Gate Re−arming Time for Slope Detection (t_{ARM}) vs. Temperature

SOT−23, 6 Lead
CASE 527AJ
ISSUE B

DATE 29 FEB 2012

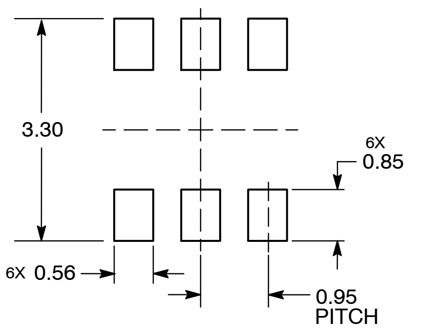
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DATUM C IS THE SEATING PLANE.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.20	0.50
c	0.08	0.26
D	2.70	3.00
E	2.50	3.10
E1	1.30	1.80
e	0.95 BSC	
L	0.20	0.60
L2	0.25 BSC	

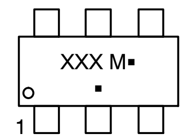
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	**98AON34321E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOT−23, 6 LEAD**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

◊