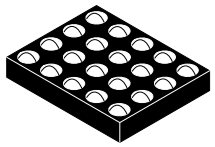
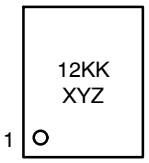
Two Low Input LDOs, Three High PSRR LDOs, Two General Purpose LDOs PMIC

FAN53870, FAN53871



WLCSP20 1.61x1.96x0.432
CASE 567YA

MARKING DIAGRAM



12	= Alphanumeric Device Marking
KK	= Lot Run Code
X	= Alphabetical Year Code
Y	= 2−weeks Date Code
Z	= Assembly Plant Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

General Description

The FAN53870 family are low Iq PMICs intended for mobile power application camera modules. The PMIC contains two high power LDOs which can operate with an input as low as 1.0 V for digital cores, three LDOs which are designed to have ultra low noise and high PSRR for sensitive analog/RF circuit loads, and two other general purpose LDOs which provide excellent overall performance.

The device is available in 20−bump, 0.35 mm pitch, Wafer−Level Chip−Scale Package (WLCSP).

Features

- LDO1 and LDO2:
  - 1 A and 1.2 A Output Current Capability Device Options
  - Programmable Output Voltage 0.8 V to 1.5 V in 8 mV Steps
  - 1.0 V to 2.0 V Input Voltage Range
  - 1.5% Accuracy
- LDO3, LDO4 and LDO5:
  - 300 mA Output Current Capability
  - Programmable Output Voltage 1.5 V to 3.4 V in 8 mV Steps
  - 1.9 V to 5.5 V Input Voltage Range
  - 14 μV (Typ) Noise
- LDO6 and LDO7:
  - 300 mA Output Current Capability
  - Programmable Output Voltage 1.5 V to 3.4 V in 8 mV Steps
  - 1.9 V to 5.5 V Input Voltage Range
- Operation Guaranteed with Battery Voltage Down to 2.5 V
- Soft−Start function (SS) to Limit Inrush Current
- Programmable Power Start−Up/Down Sequencing
- Current Limit to Protect Against Short Circuit
- I^2C Protection Fault (UVLO, OCP, UVP and OTP) Registers
- Thermal and Under Voltage Global Shutdown Protection
- I^2C Serial Control to Program Output Voltage and Features
- Small Footprint: 20−Bump WLCSP, 1.61 x 1.96 mm / 0.35 mm pitch
- Pb−Free Devices

Applications

- Smart Phones
- Wearables
- Smart Watch
- Health Monitoring
- Sensor Drive
- Energy Harvesting
- Utility and Safety Modules
- RF Modules

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ORDERING INFORMATION

Part Number	Marking	I/O Logic Level*	I²C Address	LDO1,2 I_{OUT} Capability**	LDO1,2 VOUT Default	LDO3,4 VOUT Default	LDO5 VOUT Default	LDO6,7 VOUT Default	Interrupt Pin Polarity	Temperature Range	Package	Shipping†
FAN53870UC00X	LX	1.8 V	7'h35	1.0 A	1.05 V	2.8 V	1.8 V	2.8 V	Active High: INT	−40°C to +85°C	20−Bump WLCSP (Pb−Free)	3000 / Tape & Reel
FAN53870UC12X	YF		7'h20	1.2 A								
FAN53871UC00X	LY	1.2 V	7'h20	1.0 A					Active Low: INT_B			
FAN53871UC12X	YG		7'h20	1.2 A								

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*RESET_B, SDA, SCL (open drain type pins).
** See Maximum Ratings table for Maximum Current on a Single Pin

APPLICATION CIRCUIT

Application Circuit Diagram

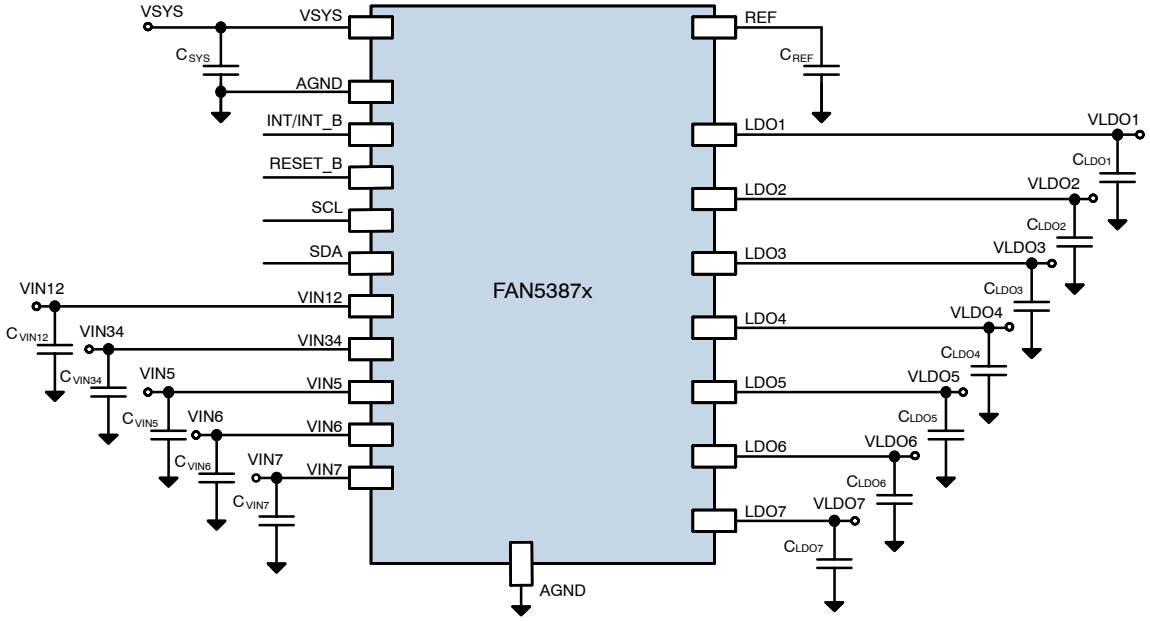

Figure 1. Application Circuit Diagram

Application Circuit Components

Table 1. RECOMMENDED EXTERNAL COMPONENTS

Component	Manufacturer	Part Number	Value	Case Size	Voltage Rating
C_{VIN12}, C_{VIN34}, C_{VIN5}, C_{VIN6}, C_{VIN7}, C_{SYS}	Murata	GRM033R61A105ME15	1.0 μF	0201/0603 (0.6 mm x 0.3 mm)	10 V
C_{LDO3}, C_{LDO4}, C_{LDO5}, C_{LDO6}, C_{LDO7}	Murata	GRM033R60J225ME47D	2.2 μF	0201/0603 (0.6 mm x 0.3 mm)	6.3 V
C_{LDO1}, C_{LDO2}	Taiyo Yuden	JMK105CBJ106MV−F	10 μF	0402/1005 (1.0 mm x 0.5 mm)	6.3 V
C_{REF}	Murata	GRM033R60J104KE19J	0.1 μF	0201/0603 (0.6 mm x 0.3 mm)	6.3 V

Table 2. RECOMMENDED ALTERNATIVE COMPONENTS

Component	Manufacturer	Part Number	Value	Case Size	Voltage Rating
C_{LDO3}, C_{LDO4}, C_{LDO5}, C_{LDO6}, C_{LDO7}	Semco	CLO3A225MQ3CRNC	2.2 μF	0201 (0.6 mm x 0.3 mm)	6.3 V

PRODUCT PIN ASSIGNMENTS

Pin Configuration

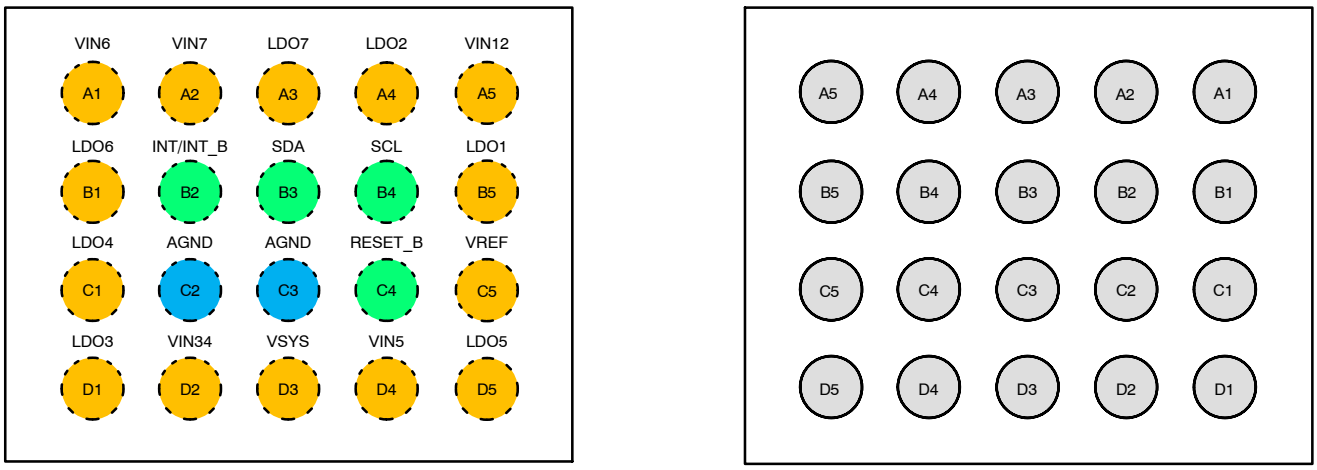

Figure 2. Pin Configuration

Pin Descriptions

PIN DEFINITIONS

Pin	Pin Name	Description
A1	VIN6	Input power pin for LDO6. Place C_{VIN6} as close to this pin as possible.
A2	VIN7	Input power pin for LDO7. Place C_{VIN7} as close to this pin as possible.
A3	LDO7	This is the output pin for LDO7. Place C_{LDO7} as close to this pin as possible.
A4	LDO2	This is the output pin for LDO2 Place C_{LDO2} as close to this pin as possible.
A5	VIN12	Input power pin for LDO1 and LDO2. Place C_{VIN12} as close to this pin as possible.
B1	LDO6	This is the output pin for LDO6. Place C_{LDO6} as close to this pin as possible.
B2	INT INT_B	Fault interrupt pin is a push−pull, active high configuration and pulls high to indicate an interrupt event has occurred. This pin returns to low when all I^2C interrupt bits are equal to 0. Fault interrupt pin is an open−drain configuration and pulls low to indicate an interrupt event has occurred. This pin returns to Hi−Z when all I^2C interrupt bits equal 0. An external pull−up resistor is required.
B3	SDA	I^2C Data pin. Node should be tied high through a pull up resistor.
B4	SCL	I^2C Clock pin. Node should be tied high through a pull up resistor.
B5	LDO1	This is the output pin for LDO1. Place C_{LDO1} as close to this pin as possible.
C1	LDO4	This is the output pin for LDO4. Place C_{LDO4} as close to this pin as possible.
C2	AGND	Digital/Analog ground connection. Tie to analog ground plane.
C3	AGND	Digital/Analog ground connection. Tie to analog ground plane.
C4	RESET_B	RESET_B pin is used to enable basic circuits necessary for controlling the PMIC. The RESET_B pin has an internal 4 MΩ (typ) pull−down and should not be left floating. When RESET_B pin is low, I^2C is not accessible.
C5	VREF	Reference bypass pin. If used, connect a 100 nF capacitor between this pin and analog ground.
D1	LDO3	This is the output pin for LDO3. Place C_{LDO3} as close to this pin as possible.
D2	VIN34	This is the input power pin for LDO3 and LDO4. Place C_{VIN34} as close to this pin as possible.
D3	VSYS	System power pin. Route trace from system to this pin. Connect the C_{SYS} capacitor as close to this pin as possible.
D4	VIN5	Input power pin for LDO5. Place C_{VIN5} as close to this pin as possible.
D5	LDO5	This is the output pin for LDO5. Place C_{LDO5} as close to this pin as possible.

PRODUCT BLOCK DIAGRAM

Block Diagram

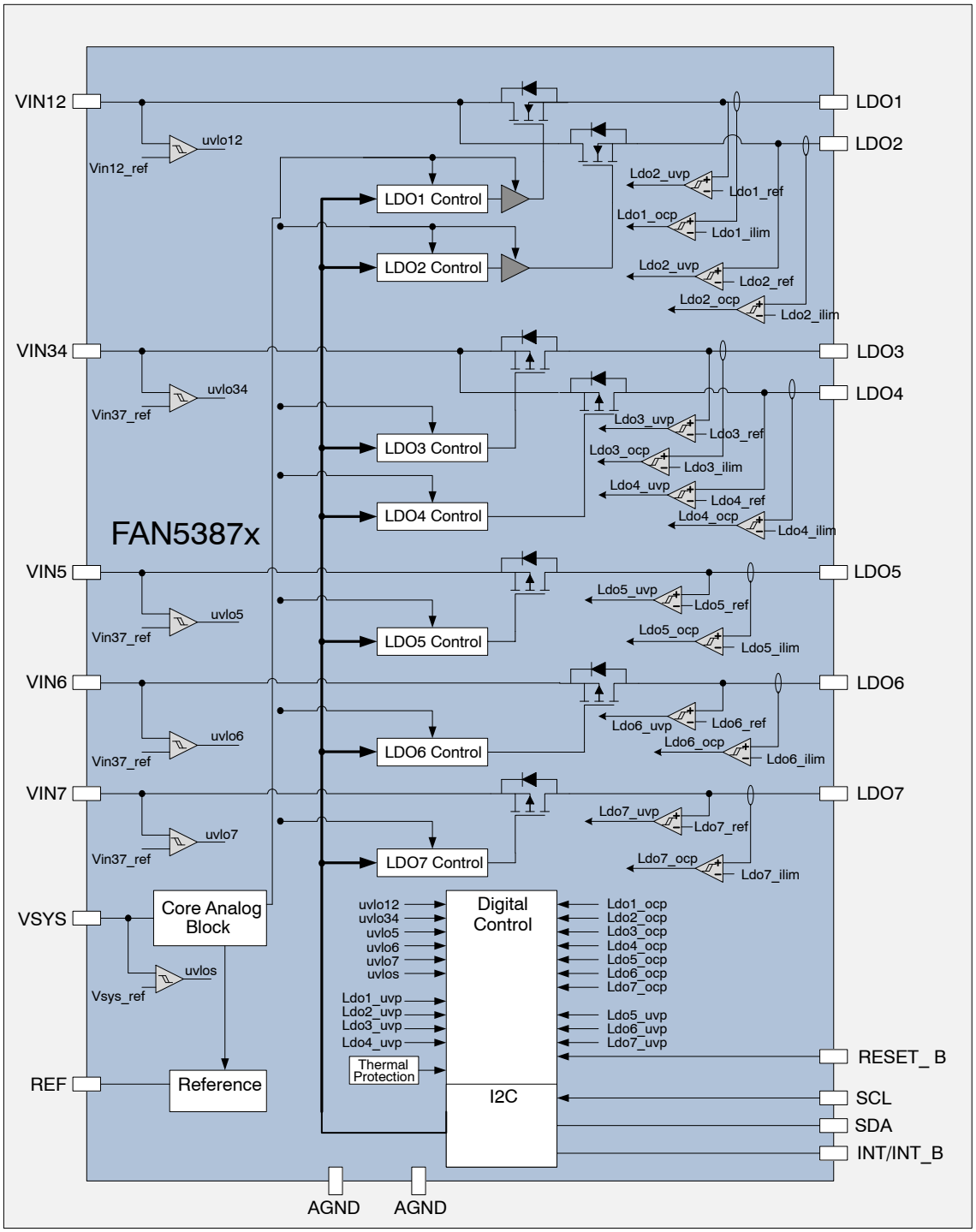

Figure 3. Block Diagram

MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{SYS}	System Input Voltage		−0.3	–	6	V
V_{IN12}	Low Voltage LDO Input		−0.3	–	6	V
V_{IN34}, V_{IN5}, V_{IN6}, V_{IN7}	Mid Voltage LDO Input		−0.3	–	6	V
V_{CTRL}	SDA, SCL and RESET_B Pins		− 0.3	–	6	V
V_{INT}	INT Pin		− 0.3	–	V_{SYS}	V
	INT_B Pin		− 0.3	–	6	
V_{LDO1-7}	Power Output Pins		− 0.3	–	6	V
Ipin_max	Maximum current on a single pin		–	–	1.5	A
ESD	Electrostatic Discharge Protection Level	Human Body Model	–	2.0	–	kV
ESD	Electrostatic Discharge Protection Level	Charged Device Model	–	1500	–	V
T_J	Junction Temperature		−40	–	+150	°C
T_{STG}	Storage Temp		−40	–	+150	°C
T_L	Soldering Temp (10 Seconds)		–	–	+260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS (Junction−to−ambient thermal resistance is a function of application and board layout. This data is measured with two−layer 2s2p boards with vias in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperature T_A.)

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
Q_{JA}	Junction −to−Ambient Thermal Resistance		–	40.4	–	°C/W

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{SYS}	Supply Voltage Range	V_{SYS}	2.5	–	5.5	V
V_{IN12}	Supply Voltage Range	V_{IN12}	1.0	–	2.0	V
V_{IN34}	Supply Voltage Range	V_{IN34}	1.9	–	5.5	V
V_{IN5}	Supply Voltage Range	V_{IN5}	1.9	–	5.5	V
V_{IN6}	Supply Voltage Range	V_{IN6}	1.9	–	5.5	V
V_{IN7}	Supply Voltage Range	V_{IN7}	1.9	–	5.5	V
P_D	Power Dissipation	PD = (125°C − 85°C) / 40.4°C/W = 0.99 W	–	–	0.99	W
T_A	Operating Ambient Temperature		−40	–	85	°C
T_J	Junction Temperature		−40	–	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (Minimum and maximum values are at V_{SYS} = 2.5 V to 5.5 V & ≥ $V_{OUT1/2}$ + 1.6 V; V_{IN12} = 1.0 V to 2.0 V & ≥ $V_{LDO1/2}$ + 200 mV, $V_{IN34/5/6/7}$ = 1.9 V to 5.5 V & ≥ $V_{LDO3/4/5/6/7}$ + 300 mV, T_J = −40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C, V_{SYS} = 3.8 V, V_{IN12} = 1.3 V, V_{IN34} = V_{IN6} = V_{IN7} = 3.8 V, V_{IN5} = 2.05 V, $V_{LDO1/2}$ = 1.05 V, $V_{LDO3/4}$ = 2.8 V, V_{LDO5} = 1.8 V and $V_{LDO6/7}$ = 2.8 V.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
POWER SUPPLY UVLO						
$V_{SYS\ UVLO\_RS}$	Under−Voltage Lockout Threshold	Rising V_{SYS}	2.30	2.35	2.40	V
$V_{SYS\ UVLO\_FL}$	Under−Voltage Lockout Threshold	Falling V_{SYS}	2.20	2.25	2.30	V
$V_{VIN12\ UVLO\_RS}$	Under−Voltage Lockout Threshold	Rising V_{IN12}	0.90	0.95	1.00	V
$V_{VIN12\ UVLO\_FL}$	Under−Voltage Lockout Threshold	Falling V_{IN12}	0.80	0.85	0.92	V
$V_{VIN\_H\ UVLO\_RS}$	Under−Voltage Lockout Threshold	Rising $V_{IN34/5/6/7}$	1.80	1.85	1.90	V
$V_{VIN\_H\ UVLO\_FL}$	Under−Voltage Lockout Threshold	Falling $V_{IN34/5/6/7}$	1.70	1.75	1.80	V
LDO1/2 QUIESCENT CURRENT						
IQ_{L12}	Quiescent Current, No Load	I_{OUT} = 0 A, total V_{SYS} and V_{IN12} current when either LDO1 or LDO2 is enabled and all other LDOs are disabled.	–	72	85	μA
OUTPUT VOLTAGE						
VO_{L12_ACC}	LDO1/2 Output Voltage Accuracy	I_{OUT} = 5 mA and 500 mA, V_{IN12} = 2.0 V, V_{SYS} = 3.8 V, V_{OUT} = 0.8 V to 1.5 V	−1.5	–	+1.5	%
$V_{L1/2\_DO}$	LDO1/2 Dropout Voltage	V_{OUT} = V_{OUT_TARGET} − 50 mV, I_{OUT} = 800 mA, V_{OUT_TARGET} = 1.05 V, V_{SYS} = 2.65 V	–	–	200	mV
CURRENT LIMIT						
I_{LIM_L12}	Current Limit (FAN53870UC00X, FAN53871UC00X)	V_{OUT} + 300 mV ≤ V_{IN12} and V_{IN12} = 1.0 V to 2.0 V, V_{SYS} = 2.5 V to 4.5 V and V_{SYS} ≥ V_{OUT} + 1.6 V	700	925	1100	mA
	Current Limit (FAN53870UC12X, FAN53871UC12X)		750	1100	1350	
I_{LIM_H12}	Current Limit (FAN53870UC00X, FAN53871UC00X)		1050	1250	1450	mA
	Current Limit (FAN53870UC12X, FAN53871UC12X)		1200	1500	1800	
OUTPUT PROTECTION						
UVP_{L12_FL}	LDO1/2 Falling UVP Output Threshold	V_{SYS} = 3.8 V, V_{OUT} = 1.05 V	86	90	94	% of V_Target
$UVP_{L1/2\_RS}$	LDO1/2 Rising UVP Output Threshold	V_{SYS} = 3.8 V, V_{OUT} = 1.05 V	91	95	98.5	% of V_Target
$R_{L1/2\_DCHG}$	Output Discharge Resistance		80	100	120	Ω
LDO3/4 QUIESCENT CURRENT						
IQ_{L34}	LDO3/4 Quiescent Current, No Load	I_{OUT} = 0 A, total V_{SYS} and V_{IN34} current when either LDO3 or LDO4 is enabled and all other LDOs disabled.	–	63	75	μA
OUTPUT VOLTAGE						
$VO_{L3/4\_ACC}$	LDO3/4 Output Voltage Accuracy	I_{OUT} = 5 mA and 300 mA, V_{IN34} = V_{SYS} = 3.8 V, V_{OUT} = 1.5 to 3.4 V	−2.0	–	+2.0	%

ELECTRICAL CHARACTERISTICS (Minimum and maximum values are at V_{SYS} = 2.5 V to 5.5 V & ≥ $V_{OUT1/2}$ + 1.6 V; V_{IN12} = 1.0 V to 2.0 V & ≥ $V_{LDO1/2}$ + 200 mV, $V_{IN34/5/6/7}$ = 1.9 V to 5.5 V & ≥ $V_{LDO3/4/5/6/7}$ + 300 mV, T_J = −40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C, V_{SYS} = 3.8 V, V_{IN12} = 1.3 V, V_{IN34} = V_{IN6} = V_{IN7} = 3.8 V, V_{IN5} = 2.05 V, $V_{LDO1/2}$ = 1.05 V, $V_{LDO3/4}$ = 2.8 V, V_{LDO5} = 1.8 V and $V_{LDO6/7}$ = 2.8 V.) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
OUTPUT VOLTAGE						
$V_{L3/4\_DO}$	LDO3/4 Dropout Voltage	V_{OUT} = V_{OUT_TARGET} − 100 mV, I_{OUT} = 300 mA, V_{OUT_TARGET} = 2.8 V, V_{SYS} = 3.8 V	–	–	200	mV
CURRENT LIMIT						
$I_{LIM\_L3/4}$	LDO3/4 Current Limit	V_{OUT} + 500 mV ≤ V_{IN34} and V_{IN34} = 2.0 V to 5.5 V, V_{SYS} = 3.8 V	300	400	500	mA
$I_{LIM\_H3/4}$	LDO3/4 Current Limit	V_{OUT} + 500 mV ≤ V_{IN34} and V_{IN34} = 2.0 V to 5.5 V, V_{SYS} = 3.8 V	525	650	775	mA
OUTPUT PROTECTION						
$UVP_{L3/4\_FL}$	LDO3/4 Falling UVP Output Threshold	V_{SYS} = 3.8 V, V_{OUT} = 2.8 V	78	80	84	% of V_Target
$UVP_{L3/4\_RS}$	LDO3/4 Rising UVP Output Threshold	V_{SYS} = 3.8 V, V_{OUT} = 2.8 V	88	90	94	% of V_Target
$R_{L3/4\_DCHG}$	Output Discharge Resistance		80	100	120	Ω
LDO5						
QUIESCENT CURRENT						
IQ_{L5}	Quiescent Current, No Load	I_{OUT} = 0 A, total V_{SYS} and V_{IN5} current when LDO5 is enabled and all other LDOs are disabled.	–	63	75	μA
OUTPUT VOLTAGE						
VO_{L5_ACC}	LDO5 Output Voltage Accuracy	I_{OUT} = 5 mA and 300 mA, V_{IN5} = V_{SYS} = 3.8 V, V_{OUT} = 1.5 V to 3.4 V	−2.0	–	+2.0	%
V_{L5_DO}	LDO5 Dropout Voltage	V_{OUT} = V_{OUT_TARGET} − 100 mV, I_{OUT} = 300 mA, V_{OUT_TARGET} = 1.8 V, V_{SYS} = 3.8 V	–	–	200	mV
CURRENT LIMIT						
I_{LIM_L5}	Current Limit	V_{OUT} + 500 mV ≤ V_{IN5} and V_{IN5} = 2.0 V to 5.5 V, V_{SYS} = 3.8 V	300	400	500	mA
I_{LIM_H5}	Current Limit	V_{OUT} + 500 mV ≤ V_{IN5} and V_{IN5} = 2.0 V to 5.5 V, V_{SYS} = 3.8 V	525	650	775	mA
OUTPUT PROTECTION						
UVP_{L5_FL}	LDO5 Falling UVP Output Threshold	V_{SYS} = 3.8 V, V_{OUT} = 2.8 V	78	80	84	% of V_Target
UVP_{L5_RS}	LDO5 Rising UVP Output Threshold	V_{SYS} = 3.8 V, V_{OUT} = 2.8 V	88	90	94	% of V_Target
R_{L5_DCHG}	Output Discharge Resistance		80	100	120	Ω
LDO6/7						
QUIESCENT CURRENT						
$IQ_{L6/7}$	Quiescent Current, No Load	I_{OUT} = 0 A, total current on V_{SYS} and V_{IN6} or V_{IN7} when LDO6 or LDO7 is enabled and all other LDOs are disabled.	–	63	75	μA
OUTPUT VOLTAGE						
$VO_{L6/7\_ACC}$	LDO6/7 Output Voltage Accuracy	I_{OUT} = 5 mA and 300 mA, $V_{IN6/7}$ = V_{SYS} = 3.8 V, V_{OUT} = 1.5 V to 3.4 V	−2.0	–	+2.0	%
$V_{L6/7\_DO}$	LDO6/7 Dropout Voltage	V_{OUT} = V_{OUT_TARGET} − 100 mV, I_{OUT} = 300 mA, V_{OUT_TARGET} = 2.8 V, V_{SYS} = 3.8 V	–	–	300	mV

ELECTRICAL CHARACTERISTICS (Minimum and maximum values are at V_{SYS} = 2.5 V to 5.5 V & ≥ $V_{OUT1/2}$ + 1.6 V; V_{IN12} = 1.0 V to 2.0 V & ≥ $V_{LDO1/2}$ + 200 mV, $V_{IN34/5/6/7}$ = 1.9 V to 5.5 V & ≥ $V_{LDO3/4/5/6/7}$ + 300 mV, T_J = −40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C, V_{SYS} = 3.8 V, V_{IN12} = 1.3 V, V_{IN34} = V_{IN6} = V_{IN7} = 3.8 V, V_{IN5} = 2.05 V, $V_{LDO1/2}$ = 1.05 V, $V_{LDO3/4}$ = 2.8 V, V_{LDO5} = 1.8 V and $V_{LDO6/7}$ = 2.8 V.) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CURRENT LIMIT						
$I_{LIM\_L6/7}$	LDO6/7 Current Limit	V_{OUT} + 500 mV ≤ $V_{IN6/7}$ and $V_{IN6/7}$ = 2.0 V to 5.5 V, V_{SYS} = 3.8 V	300	400	500	mA
$I_{LIM\_H6/7}$	LDO6/7 Current Limit	V_{OUT} + 500 mV ≤ $V_{IN6/7}$ and $V_{IN6/7}$ = 2.0 V to 5.5 V, V_{SYS} = 3.8 V	525	650	775	mA
OUTPUT PROTECTION						
$UVP_{L6/7\_FL}$	LDO6/7 Falling UVP Output Threshold	V_{SYS} = 3.8 V, V_{OUT} = 2.8 V	78	80	84	% of V_Target
$UVP_{L6/7\_RS}$	LDO6/7 Rising UVP Output Threshold	V_{SYS} = 3.8 V, V_{OUT} = 2.8 V	88	90	94	% of V_Target
$R_{L6/7\_DCHG}$	Output Discharge Resistance		80	100	120	Ω
I/O LEVELS						
V_{IL}	RESET_B Logic Low Threshold	FAN53870			0.4	V
		FAN53871			0.325	
V_{IH}	RESET_B Logic High Threshold	FAN53870	1.2		V_{IN}	
		FAN53871	0.825		V_{IN}	
V_{OL_INT}	Interrupt Pin Low Level	Isink = 5 mA	–	–	0.3	V
V_{OH_INT}	INT Pin (FAN53870) High Level	V_{SYS} = 2.5 V, I_{OUT} = 1 mA	1.7	–	1.9	V
I_{INT}	Interrupt Pin Leakage	V_{INT} = V_{INT_B} = 5.5 V	–	–	0.5	uA
IQ CONDITIONS						
$I_{Q\ VSYS\_SD}$	Shutdown Supply Current	Current on V_{SYS} when = 5.5 V and all xxx_EN bits = 0, xxx_SEQ bits = 000, RESET_B = SDA = SCL = Low, T_J = 85°C	–	–	3.0	μA
$I_{Q\ VIN12\_SD}$	Shutdown Supply Current	Total current on V_{IN12} when = 2.0 V and all xxx_EN bits = 0, xxx_SEQ bits = 000, RESET_B = SDA = SCL = Low, T_J = 85°C	–	–	1.5	μA
$I_{Q\ VIN34\_SD}$	Shutdown Supply Current	Current on V_{IN34} when = 5.5 V and all xxx_EN bits = 0, xxx_SEQ bits = 000, RESET_B = SDA = SCL = Low, TJ = 85°C	–	–	1.5	μA
$I_{Q\ VIN5/6/7\_SD}$	Shutdown Supply Current	Current on V_{IN5} or V_{IN6} or V_{IN7} when = 5.5 V and all xxx_EN bits = 0, xxx_SEQ bits = 000, RESET_B = SDA = SCL = Low, T_J = 85°C	–	–	1.5	μA
I_{Q_STBY}	Standby Supply Current – All LDOs enabled and no load.	Total current on V_{SYS} and all VINs when V_{SYS} = V_{IN34} = V_{IN5} = V_{IN6} = 5.5 V and V_{IN12} = 2.0 V, RESET_B = High, all xxx_EN bits = 1, xxx_SEQ = 000	–	380	425	μA
I_{SLP}	Sleep Supply Current	Total current on V_{SYS} and all VINs when V_{SYS} = V_{IN34} = V_{IN5} = V_{IN6} = 5.5 V and V_{IN12} = 2.0 V, RESET_B = High, all xxx_EN bits = 0, xxx_SEQ = 000, no I^2C activity	–	12	20	μA
I^2C TIMING AND PERFORMANCE *						
V_{IL}	SDA and SCL Logic Low threshold	FAN53870	−0.5	–	0.3 V_{DD}	V
		FAN53871	−0.5	–	0.325	
V_{IH}	SDA and SCL Logic High threshold	FAN53870	0.7 V_{DD}	–	5.5	V
		FAN53871	0.825	–	5.5	
V_{OL}	SDA Logic Low Output	3 mA Sink	–	–	0.4	V
I_{OL}	SDA Sink Current		20	–	–	mA

ELECTRICAL CHARACTERISTICS (Minimum and maximum values are at V_{SYS} = 2.5 V to 5.5 V & ≥ $V_{OUT1/2}$ + 1.6 V; V_{IN12} = 1.0 V to 2.0 V & ≥ $V_{LDO1/2}$ + 200 mV, $V_{IN34/5/6/7}$ = 1.9 V to 5.5 V & ≥ $V_{LDO3/4/5/6/7}$ + 300 mV, T_J = −40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C, V_{SYS} = 3.8 V, V_{IN12} = 1.3 V, V_{IN34} = V_{IN6} = V_{IN7} = 3.8 V, V_{IN5} = 2.05 V, $V_{LDO1/2}$ = 1.05 V, $V_{LDO3/4}$ = 2.8 V, V_{LDO5} = 1.8 V and $V_{LDO6/7}$ = 2.8 V.) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I²C TIMING AND PERFORMANCE *						
fSCL	SCL Clock Frequency	Fast Mode Plus	–	–	1000	kHz
tBUF	Bus−Free Time Between STOP and START Conditions	Fast Mode Plus	0.5	–	–	μs
tHD;STA	START or Repeated START Hold Time	Fast Mode Plus	260	–	–	ns
tLOW	SCL LOW Period	Fast Mode Plus	0.5	–	–	μs
tHIGH	SCL HIGH Period	Fast Mode Plus	260	–	–	ns
tSU;STA	Repeated START Setup Time	Fast Mode Plus	260	–	–	ns
tSU;DAT	Data Setup Time	Fast Mode Plus	50	–	–	ns
tVD;DAT	Data Valid Time	Fast Mode Plus	–	–	450	ns
tVD;ACK	Data Valid Acknowledge Time	Fast Mode Plus	–	–	450	ns
tR	SDA and SCL Rise Time	Fast Mode Plus	–	–	120	ns
tF	SDA and SCL Fall Time	Fast Mode Plus	20 x V_{DD} / 5.5 V	–	120	ns
tSU;STO	Stop Condition Setup Time	Fast Mode Plus	260	–	–	ns
Ci	SDA and SCL Input Capacitance		–	–	10	pF
Cb	Capacitive Load for SDA and SCL		–	–	550	pF
t_{SP}	Spike pulse width that input filter must be suppress	SCL, SDA only	0	–	50	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Guarantee Levels:
*Guaranteed by Design Only. Not Characterized or Production Tested.

SYSTEM CHARACTERISTICS (The following system specifications are guaranteed by design and are not performed in production testing. They reflect closed loop performance using the Recommended Layout and External Components. Minimum and maximum values are at V_{SYS} = 2.5 V to 5.5 V & ≥ $V_{LDO1/2}$ + 1.6 V, V_{IN12} = 1.0 V to 2.0 V & ≥ $V_{LDO1/2}$ + 200 mV, $V_{IN34/5/6/7}$ = 1.9 V to 5.5 V & $V_{IN34/5/6/7}$ ≥ $V_{LDO3/4/5/6/7}$ + 300 mV, T_A = −40°C to +85°C unless otherwise noted. Typical values are at T_A = 25°C, V_{SYS} = 3.8 V, V_{IN12} = 1.3 V, V_{IN34} = V_{IN6} = V_{IN7} = 3.8 V, V_{IN5} = 2.05 V, $V_{LDO1/2}$ = 1.05 V, $V_{LDO3/4}$ = 2.8 V, V_{LDO5} = 1.8 V and $V_{LDO6/7}$ = 2.8 V.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LDO1/2 SOFT START						
T_{SS_LDO12}	Startup Time	EN bit = 1 to 90% of V_{OUT} (1.05 V), I_{OUT} = 10 mA, COUT = 20 μF	–	400	–	μs
PSRR & NOISE						
$PSRR_{L1/2\_VIN}$	Power Supply Rejection Ratio on VIN12	V_{IN12} = 1.35 V, V_{OUT} = 1.2 V, I_{OUT} = 150 mA, C_{IN12} = 1.0 μF, $C_{OUT1/2}$ = 10 μF, FREQ = 1 kHz	–	68	–	dB
$PSRR_{L1/2\_VS}$	Power Supply Rejection Ratio on VSYS	V_{IN12} = 1.35 V, V_{OUT} = 1.2 V, I_{OUT} = 150 mA, C_{IN12} = 1.0 μF, $C_{OUT1/2}$ = 10 μF, FREQ = 1 kHz	–	70	–	dB
$PSRR_{L1/2\_VIN}$	Power Supply Rejection Ratio on VIN12	V_{IN12} = 1.35 V, V_{OUT} = 1.2 V, I_{OUT} = 150 mA, C_{IN12} = 1.0 μF, $C_{OUT1/2}$ = 10 μF, FREQ = 10 kHz	–	52	–	dB
$PSRR_{L1/2\_VS}$	Power Supply Rejection Ratio on VSYS	V_{IN12} = 1.35 V, V_{OUT} = 1.2 V, I_{OUT} = 150 mA, C_{IN12} = 1.0 μF, $C_{OUT1/2}$ = 10 μF, FREQ = 10 kHz	–	57	–	dB
$PSRR_{L1/2\_VIN}$	Power Supply Rejection Ratio on VIN12	V_{IN12} = 1.35 V, V_{OUT} = 1.2 V, I_{OUT} = 150 mA, C_{IN12} = 1.0 μF, $C_{OUT1/2}$ = 10 μF, FREQ = 100 kHz	–	34	–	dB
$PSRR_{L1/2\_VS}$	Power Supply Rejection Ratio on VSYS	V_{IN12} = 1.35 V, V_{OUT} = 1.2 V, I_{OUT} = 150 mA, C_{IN12} = 1.0 μF, $C_{OUT1/2}$ = 10 μF, FREQ = 100 kHz	–	41	–	dB
$PSRR_{L1/2\_VIN}$	Power Supply Rejection Ratio on VIN12	V_{IN12} = 1.35 V, V_{OUT} = 1.2 V, I_{OUT} = 150 mA, C_{IN12} = 1.0 μF, $C_{OUT1/2}$ = 10 μF, FREQ = 1 MHz	–	30	–	dB
$PSRR_{L1/2\_VS}$	Power Supply Rejection Ratio on VSYS	V_{IN12} = 1.35 V, V_{OUT} = 1.2 V, I_{OUT} = 150 mA, C_{IN12} = 1.0 μF, $C_{OUT1/2}$ = 10 μF, FREQ = 1 MHz	–	37	–	dB
$V_{N\_L1/2}$	LDO1/2 Output Noise	FREQ: 10 Hz to 100 kHz, I_{OUT} = 100 mA	–	18	–	uVrms
REGULATION & TRANSIENT PERFORMANCE						
$REG_{L1/2\_LD}$	LDO Load Regulation	I_{OUT} = 1 mA to 800 mA, V_{SYS} = 3.8 V	−0.001	–	+0.001	%/mA
$REG_{L1/2\_LN}$	LDO Line Regulation	V_{SYS} = 2.5 V to 4.5 V & V_{SYS} ≥ V_{OUT} + 1.6 V, V_{OUT} + 300 mV ≤ V_{IN12} ≤ 2.0 V, I_{OUT} = 50 mA	−0.10	–	+0.10	%
$V_{L1/2\ TR\_LD}$	LDO Load Transient	I_{OUT} = 1 mA ↔ 500 mA, 100 mA/μs, V_{SYS} ≥ V_{OUT} + 1.6 V	−40	–	+40	mV
SHORT CIRCUIT						
$T_{L12\ SC\_DEB}$	Default Short Circuit Debounce Timer		–	1.0	–	ms
$T_{L12\ SC\_RST}$	Period from Short Circuit Shutdown to Restart		–	20	–	ms
LDO3/4 SOFT START						
$T_{SS\_L3/4}$	Soft Start Time	LDO3_EN or LDO4_EN bit = 1 to 90% of V_{OUT} = 2.8 V, I_{OUT} = 10 mA, C_{IN} = 1 μF, C_{OUT} = 4.7 μF	–	100	–	μs

SYSTEM CHARACTERISTICS (The following system specifications are guaranteed by design and are not performed in production testing. They reflect closed loop performance using the Recommended Layout and External Components. Minimum and maximum values are at V_{SYS} = 2.5 V to 5.5 V & ≥ $V_{LDO1/2}$ + 1.6 V, V_{IN12} = 1.0 V to 2.0 V & ≥ $V_{LDO1/2}$ + 200 mV, $V_{IN34/5/6/7}$ = 1.9 V to 5.5 V & $V_{IN34/5/6/7}$ ≥ $V_{LDO3/4/5/6/7}$ + 300 mV, T_A = −40°C to +85°C unless otherwise noted. Typical values are at T_A = 25°C, V_{SYS} = 3.8 V, V_{IN12} = 1.3 V, V_{IN34} = V_{IN6} = V_{IN7} = 3.8 V, V_{IN5} = 2.05 V, $V_{LDO1/2}$ = 1.05 V, $V_{LDO3/4}$ = 2.8 V, V_{LDO5} = 1.8 V and $V_{LDO6/7}$ = 2.8 V.) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PSRR & NOISE						
$PSRR_{L3/4\_VIN}$	Power Supply Rejection Ratio on VIN34	I_{OUT} = 50 mA, C_{IN34} = 1.0 μF, $C_{OUT3/4}$ = 2.2 μF, FREQ = 1 kHz	–	89	–	dB
$PSRR_{L3/4\_VS}$	Power Supply Rejection Ratio on VSYS	I_{OUT} = 50 mA, C_{IN34} = 1.0 μF, $C_{OUT3/4}$ = 2.2 μF, FREQ = 1 kHz	–	85	–	dB
$PSRR_{L3/4\_VIN}$	Power Supply Rejection Ratio on VIN34	I_{OUT} = 50 mA, C_{IN34} = 1.0 μF, $C_{OUT3/4}$ = 2.2 μF, FREQ = 10 kHz	–	84	–	dB
$PSRR_{L3/4\_VS}$	Power Supply Rejection Ratio on VSYS	I_{OUT} = 50 mA, C_{IN34} = 1.0 μF, $C_{OUT3/4}$ = 2.2 μF, FREQ = 10 kHz	–	70	–	dB
$PSRR_{L34\_VIN}$	Power Supply Rejection Ratio on VIN34	I_{OUT} = 50 mA, C_{IN34} = 1.0 μF, $C_{OUT3/4}$ = 2.2 μF, FREQ = 100 kHz	–	57	–	dB
$PSRR_{L34\_VS}$	Power Supply Rejection Ratio on VSYS	I_{OUT} = 50 mA, C_{IN34} = 1.0 μF, $C_{OUT3/4}$ = 2.2 μF, FREQ = 100 kHz	–	52	–	dB
$PSRR_{L3/4\_VIN}$	Power Supply Rejection Ratio on VIN34	I_{OUT} = 50 mA, C_{IN34} = 1.0 μF, $C_{OUT3/4}$ = 2.2 μF, FREQ = 1 MHz	–	40	–	dB
$PSRR_{L3/4\_VS}$	Power Supply Rejection Ratio on VSYS	I_{OUT} = 50 mA, C_{IN34} = 1.0 μF, $C_{OUT3/4}$ = 2.2 μF, FREQ = 1 MHz	–	36	–	dB
V_{N_L34}	LDO3/4 Output Noise	FREQ: 10 Hz to 100 kHz, I_{OUT} = 300 mA	–	14	–	uVRMS
REGULATION & TRANSIENT PERFORMANCE						
$REG_{L3/4\_LD}$	LDO Load Regulation	I_{OUT} = 100 μA to 300 mA, V_{SYS} = VIN34 = 3.8 V, V_{OUT} = 2.8 V	−0.001	–	+0.001	%/mA
$REG_{L3/4\_LN}$	LDO Line Regulation	V_{SYS}, V_{IN34} = 2.5 to 5.5 V and V_{SYS}, V_{IN34} . V_{OUT} + 500 mV, I_{OUT} = 50 mA	−0.1	–	+0.1	%
		V_{SYS}, V_{IN34} = 2.5 to 5.5 V and V_{SYS}, V_{IN34} ≥ V_{OUT} + 500 mV, I_{OUT} = 300 mA	−0.1	–	+0.3	
$V_{L3/4\ TR\_LD}$	LDO Load Transient	I_{OUT} = 1 mA ↔ 200 mA, 100 mA/μs, V_{SYS} = V_{IN34} = 3.8 V	−40	–	+40	mV
SHORT CIRCUIT						
$T_{L3/4\ SC\_DEB}$	Short Circuit Debouncer Timer		–	1.0	–	ms
$T_{LDO34\ SC\_RST}$	Period from Short Circuit Shutdown to Restart		–	20	–	ms
LDO5 SOFT START						
T_{SS_L5}	Soft Start Time	LDO5_EN bit = 1 to 90% of V_{OUT} = 2.8 V, I_{OUT} = 10 mA, C_{IN} = 1 μF, C_{OUT} = 4.7 μF	–	100	–	μs
PSRR & NOISE						
$PSRR_{L5\_VIN}$	Power Supply Rejection Ratio on VIN5	FREQ = 1 kHz	–	72	–	dB
$PSRR_{L5\_VS}$	Power Supply Rejection Ratio on VSYS	FREQ = 1 kHz	–	81	–	dB
$PSRR_{L5\_HV\_VIN}$	Power Supply Rejection Ratio on VIN5	I_{OUT} = 150 mA, FREQ = 1 kHz, C_{IN} = 1.0 μF, C_{OUT} = 2.2 μF, V_{IN5} = 3.8 V, V_{OUT} = 1.8V	–	80	–	dB
$PSRR_{L5\_HV\_VS}$	Power Supply Rejection Ratio on VSYS	I_{OUT} = 150 mA, FREQ = 1 kHz, C_{IN} = 1.0 μF, C_{OUT} = 2.2 μF, V_{IN5} = 3.8 V, V_{OUT} = 1.8 V	–	82	–	dB
$PSRR_{L5\_VIN}$	Power Supply Rejection Ratio on VIN5	I_{OUT} = 150 mA, C_{IN5} = 1.0 μF, C_{OUT5} = 2.2 μF, FREQ = 10 kHz	–	60	–	dB

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PSRR & NOISE						
$PSRR_{L5\_VS}$	Power Supply Rejection Ratio on VSYS	I_{OUT} = 150 mA, C_{IN5} = 1.0 μF, C_{OUT5} = 2.2 μF, FREQ = 10 kHz	–	67	–	dB
$PSRR_{L5\_VIN}$	Power Supply Rejection Ratio on VIN5	I_{OUT} = 150 mA, C_{IN5} = 1.0 μF, C_{OUT5} = 2.2 μF, FREQ = 100 kHz	–	40	–	dB
$PSRR_{L5\_VS}$	Power Supply Rejection Ratio on VSYS	I_{OUT} = 150 mA, C_{IN5} = 1.0 μF, C_{OUT5} = 2.2 μF, FREQ = 100 kHz	–	57	–	dB
$PSRR_{L5\_VIN}$	Power Supply Rejection Ratio on VIN5	I_{OUT} = 150 mA, C_{IN5} = 1.0 μF, C_{OUT5} = 2.2 μF, FREQ = 1 MHz	–	26	–	dB
$PSRR_{L5\_VS}$	Power Supply Rejection Ratio on VSYS	I_{OUT} = 150 mA, C_{IN5} = 1.0 μF, C_{OUT5} = 2.2 μF, FREQ = 1 MHz	–	36	–	dB
V_{N_L5}	LDO5 Output Noise	FREQ: 10 Hz to 100 kHz, I_{OUT} = 300 mA	–	14	–	μVRMS
REGULATION & TRANSIENT PERFORMANCE						
REG_{L5_LD}	LDO Load Regulation	I_{OUT} = 100 μA to 300 mA, V_{SYS} = V_{IN5} = 3.8 V, V_{OUT} = 1.8 V	−0.001	–	+0.001	%/mA
REG_{L5_LN}	LDO Line Regulation	V_{SYS} = 2.5 V to 5.5 V, V_{IN5} = 2.0 V to 5.5 V, and V_{SYS}, V_{IN5} ≥ V_{OUT} + 500 mV, I_{OUT} = 50 mA	−0.1	–	+0.1	%
		V_{SYS} = 2.5 V to 5.5 V, V_{IN5} = 2.0 V to 5.5 V, and V_{SYS}, V_{IN5} ≥ V_{OUT} + 500 mV, I_{OUT} = 300 mA	−0.1	–	+0.4	
$V_{L5\ TR\_LD}$	LDO Load Transient	I_{OUT} = 1 mA ↔ 200 mA, 100 mA/μs, V_{SYS} = 3.8 V, V_{IN5} = 2.05 V, V_{OUT} = 1.8 V	−40	–	+40	mV
SHORT CIRCUIT						
$T_{L5\ SC\_DEB}$	Short Circuit Debouncer Timer		–	1.0	–	ms
$T_{LDO5\ SC\_RST}$	Period from Short Circuit Shutdown to Restart		–	20	–	ms
LDO6/7 SOFT START						
$T_{SS\_L6/7}$	Soft Start Time	LDO6_EN or LDO7_EN bit = 1 to 90% of V_{OUT} = 2.8 V, I_{OUT} = 10 mA, C_{IN} = 1 μF, C_{OUT} = 4.7 μF	–	100	–	μs
PSRR & NOISE						
$PSRR_{L6/7\_VIN}$	Power Supply Rejection Ratio on VIN6/7	I_{OUT} = 150 mA, FREQ = 1 kHz, C_{IN} = 1.0 μF, C_{OUT} = 2.2 μF, $V_{IN6/7}$ = 2.05 V, V_{SYS} = 3.8 V, V_{OUT} = 1.8 V	–	80	–	dB
$PSRR_{L6/7\_VS}$	Power Supply Rejection Ratio on VSYS	I_{OUT} = 150 mA, FREQ = 1 kHz, C_{IN} = 1.0 μF, C_{OUT} = 2.2 μF, $V_{IN6/7}$ = 2.05 V, V_{SYS} = 3.8 V, V_{OUT} = 1.8 V	–	72	–	dB
$PSRR_{L6/7\_HV\_VIN}$	Power Supply Rejection Ratio on VIN6/7	I_{OUT} = 150 mA, $C_{IN6/7}$ = 1.0 μF, $C_{OUT6/7}$ = 2.2 μF, FREQ = 1 kHz	–	75	–	dB
$PSRR_{L6/7\_HV\_VS}$	Power Supply Rejection Ratio on VSYS	I_{OUT} = 150 mA, $C_{IN6/7}$ = 1.0 μF, $C_{OUT6/7}$ = 2.2 μF, FREQ = 1 kHz	–	75	–	dB
$PSRR_{L6/7\_HV\_VIN}$	Power Supply Rejection Ratio on VIN6/7	I_{OUT} = 150 mA, $C_{IN6/7}$ = 1.0 μF, $C_{OUT6/7}$ = 2.2 μF, FREQ = 10 kHz	–	70	–	dB
$PSRR_{L6/7\_HV\_VS}$	Power Supply Rejection Ratio on VSYS	I_{OUT} = 150 mA, $C_{IN6/7}$ = 1.0 μF, $C_{OUT6/7}$ = 2.2 μF, FREQ = 10 kHz	–	70	–	dB

SYSTEM CHARACTERISTICS (The following system specifications are guaranteed by design and are not performed in production testing. They reflect closed loop performance using the Recommended Layout and External Components. Minimum and maximum values are at V_{SYS} = 2.5 V to 5.5 V & ≥ $V_{LDO1/2}$ + 1.6 V, V_{IN12} = 1.0 V to 2.0 V & ≥ $V_{LDO1/2}$ + 200 mV, $V_{IN34/5/6/7}$ = 1.9 V to 5.5 V & $V_{IN34/5/6/7}$ ≥ $V_{LDO3/4/5/6/7}$ + 300 mV, T_A = −40°C to +85°C unless otherwise noted. Typical values are at T_A = 25°C, V_{SYS} = 3.8 V, V_{IN12} = 1.3 V, V_{IN34} = V_{IN6} = V_{IN7} = 3.8 V, V_{IN5} = 2.05 V, $V_{LDO1/2}$ = 1.05 V, $V_{LDO3/4}$ = 2.8 V, V_{LDO5} = 1.8 V and $V_{LDO6/7}$ = 2.8 V.) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PSRR & NOISE						
$PSRR_{L6/7\_HV\_VIN}$	Power Supply Rejection Ratio on VIN6/7	I_{OUT} = 150 mA, $C_{IN6/7}$ = 1.0 μF, $C_{OUT6/7}$ = 2.2 μF, FREQ = 100 kHz	–	53	–	dB
$PSRR_{L6/7\_HV\_VS}$	Power Supply Rejection Ratio on VSYS	I_{OUT} = 150 mA, $C_{IN6/7}$ = 1.0 μF, $C_{OUT6/7}$ = 2.2 μF, FREQ = 100 kHz	–	46	–	dB
$PSRR_{L6/7\_HV\_VIN}$	Power Supply Rejection Ratio on VIN6/7	I_{OUT} = 150 mA, $C_{IN6/7}$ = 1.0 μF, $C_{OUT6/7}$ = 2.2 μF, FREQ = 1 MHz	–	40	–	dB
$PSRR_{L6/7\_HV\_VS}$	Power Supply Rejection Ratio on VSYS	I_{OUT} = 150 mA, $C_{IN6/7}$ = 1.0 μF, $C_{OUT6/7}$ = 2.2 μF, FREQ = 1 MHz	–	33	–	dB
$V_{N\_L6/7}$	LDO6/7 Output Noise	FREQ: 10 Hz to 100 kHz, I_{OUT} = 300 mA	–	40	–	μVRMS
REGULATION & TRANSIENT PERFORMANCE						
$REG_{L6/7\_LD}$	LDO Load Regulation	I_{OUT} = 100 μA to 300 mA, V_{SYS} = $V_{IN6/7}$ = 3.8 V, V_{OUT} = 2.8 V	−0.001	–	+0.001	%/mA
$REG_{L6/7\_LN}$	LDO Line Regulation	V_{SYS} = 2.5 V to 5.5 V, $V_{IN6/7}$ = 2.0 V to 5.5 V, and V_{SYS}, $V_{IN6/7}$ ≥ V_{OUT} + 500 mV, I_{OUT} = 50mA	−0.1	–	+0.1	%
		V_{SYS} = 2.5 V to 5.5 V, $V_{IN6/7}$ = 2.0 V to 5.5 V, and V_{SYS}, $V_{IN6/7}$ ≥ V_{OUT} + 500 mV, I_{OUT} = 300 mA	−0.1	–	+0.5	
$V_{L6/7\ TR\_LD}$	LDO Load Transient	I_{OUT} = 1 mA ↔ 200 mA, 100 mA/μs, V_{SYS} = $V_{IN6/7}$ = 3.8 V, V_{OUT} = 2.8 V	−40	–	+40	mV
SHORT CIRCUIT						
$T_{L6/7\ SC\_DEB}$	Short Circuit Debouncer Timer		–	1.0	–	ms
$T_{LDO6/7\ SC\_RST}$	Period from Short Circuit Shutdown to Restart		–	20	–	ms
THERMAL PROTECTION						
T_{WRN}	Thermal Warning		–	125	–	°C
T_{SD}	Thermal Shutdown		–	140	–	°C
T_{HYS}	Thermal Hysteresis for TSD and TWRN		–	15	–	°C

TYPICAL CHARACTERISTICS

(UNLESS OTHERWISE NOTED, T_A = 25°C, V_{SYS} = 3.8 V, V_{IN12} = 1.3 V, V_{IN34}, V_{IN6}, V_{IN7} = 3.8 V, V_{IN5} = 2.05 V, $V_{LDO1/2}$ = 1.05 V, $V_{LDO3/4}$ = 2.8 V, V_{LDO5} = 1.8 V AND $V_{LDO6/7}$ = 2.8 V, RECOMMENDED LAYOUT AND EXTERNAL COMPONENTS.)

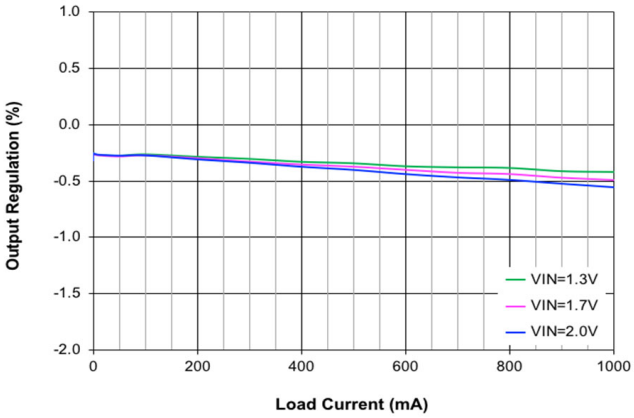


Figure 4. LDO1/2 Output Regulation vs. Load Current and Input Voltage, V_{OUT} = 1.05 V

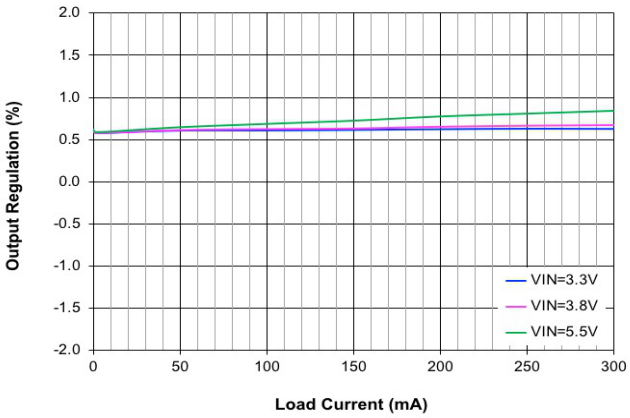


Figure 5. LDO3/4 Output Regulation vs. Load Current and Input Voltage, V_{OUT} = 2.8 V

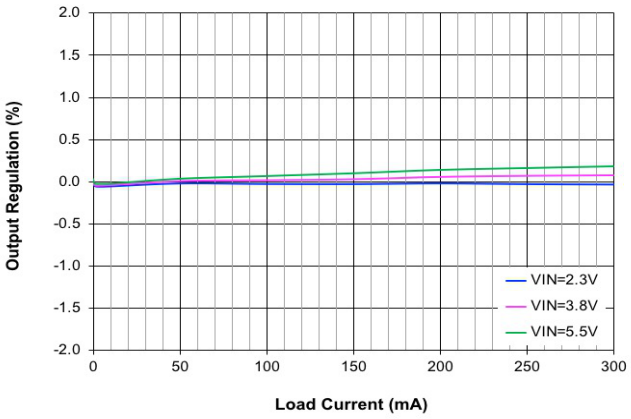


Figure 6. LDO5 Output Regulation vs. Load Current and Input Voltage, V_{OUT} = 1.8 V

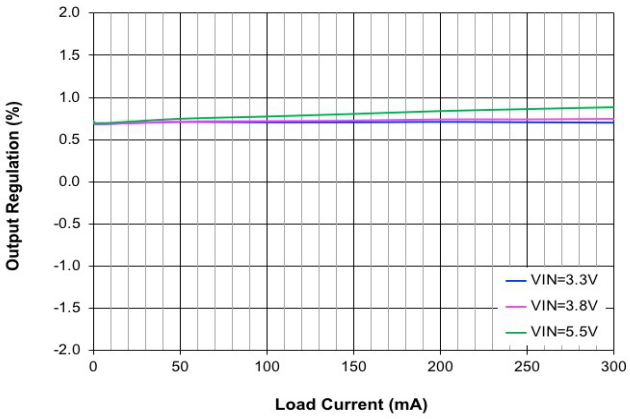


Figure 7. LDO6/7 Output Regulation vs. Load Current and Input Voltage, V_{OUT} = 2.8 V

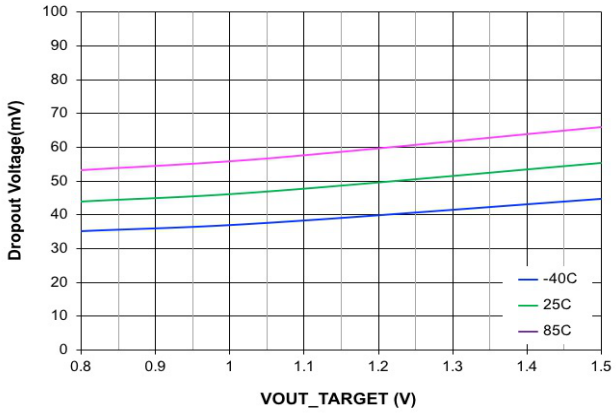


Figure 8. LDO1/2 Dropout Voltage vs. Target Output Voltage and Temperature, I_{OUT} = 800 mA

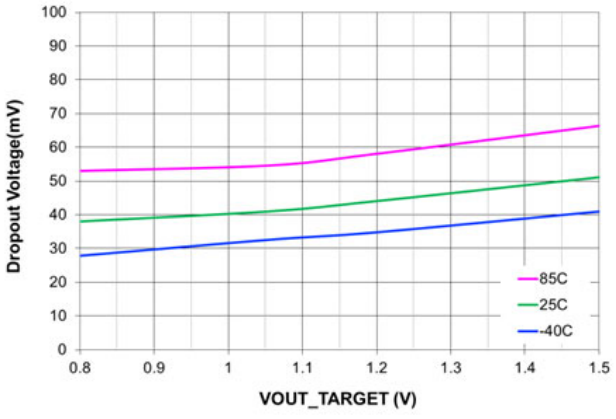


Figure 9. LDO1/2 Dropout Voltage vs. Target Output Voltage and Temperature, I_{OUT} = 1000 mA

TYPICAL CHARACTERISTICS (continued)

(Unless otherwise noted, T_A = 25°C, V_{SYS} = 3.8 V, V_{IN12} = 1.3 V, V_{IN34}, V_{IN6}, V_{IN7} = 3.8 V, V_{IN5} = 2.05 V, $V_{LDO1/2}$ = 1.05 V, $V_{LDO3/4}$ = 2.8 V, V_{LDO5} = 1.8 V and $V_{LDO6/7}$ = 2.8 V, Recommended Layout and External Components.)

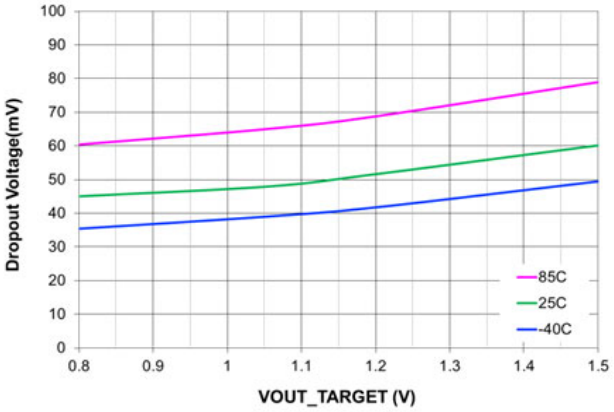


Figure 10. LDO1/2 Dropout Voltage vs. Target Output Voltage and Temperature, I_{OUT} = 1200 mA

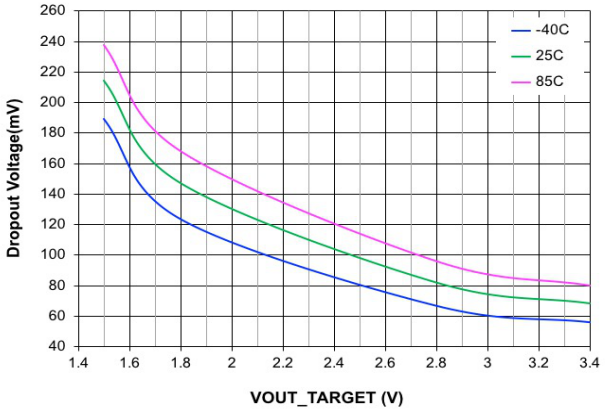


Figure 11. LDO3/4/5 Dropout Voltage vs. Target Output Voltage and Temperature, I_{OUT} = 300 mA

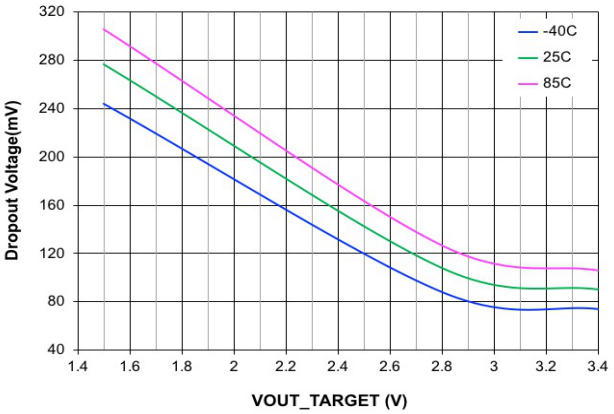


Figure 12. LDO6/7 Dropout Voltage vs. Target Output Voltage and Temperature, I_{OUT} = 300 mA

Figure 13. LDO1/2 PSRR vs. Frequency, 150 mA Load

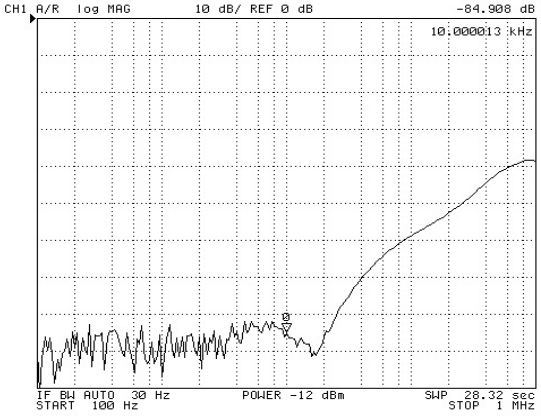


Figure 14. LDO3/4 PSRR vs. Frequency, 50 mA Load

Figure 15. LDO5 PSRR vs. Frequency, 150 mA Load

TYPICAL CHARACTERISTICS (continued)

(Unless otherwise noted, T_A = 25°C, V_{SYS} = 3.8 V, V_{IN12} = 1.3 V, V_{IN34}, V_{IN6}, V_{IN7} = 3.8 V, V_{IN5} = 2.05 V, $V_{LDO1/2}$ = 1.05 V, $V_{LDO3/4}$ = 2.8 V, V_{LDO5} = 1.8 V and $V_{LDO6/7}$ = 2.8 V, Recommended Layout and External Components.)

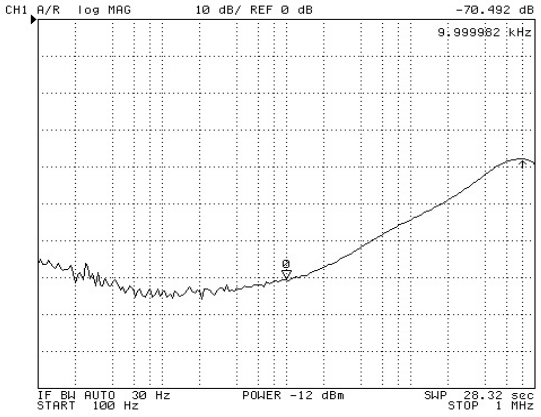


Figure 16. LDO6/7 PSRR vs. Frequency, 150 mA Load

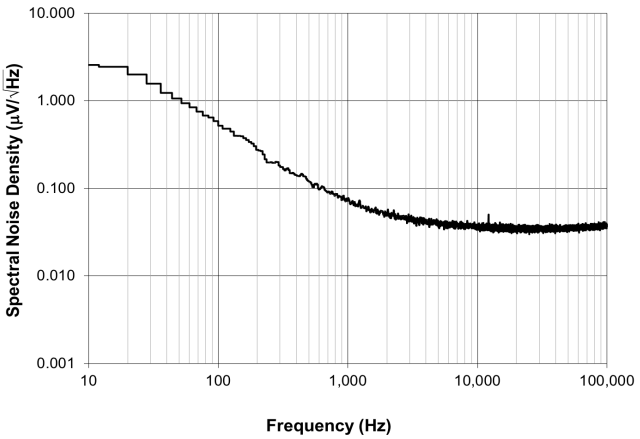


Figure 17. LDO1/2 Output Noise vs. Frequency, 100 mA Load

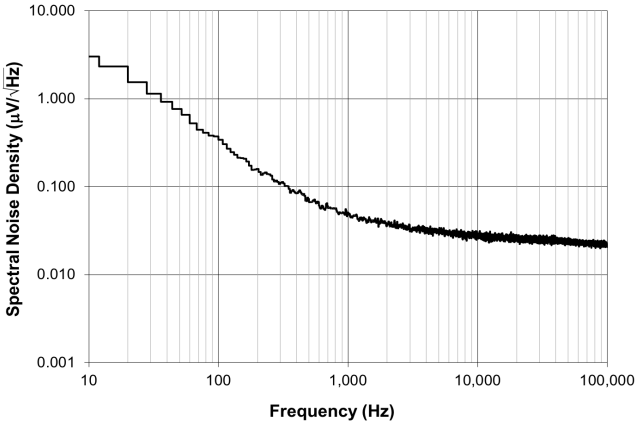


Figure 18. LDO3/4 Output Noise vs. Frequency, 300 mA Load

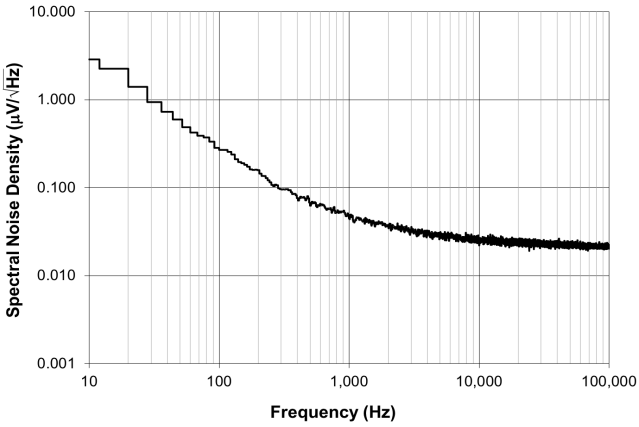


Figure 19. LDO5 Output Noise vs. Frequency, 300 mA Load

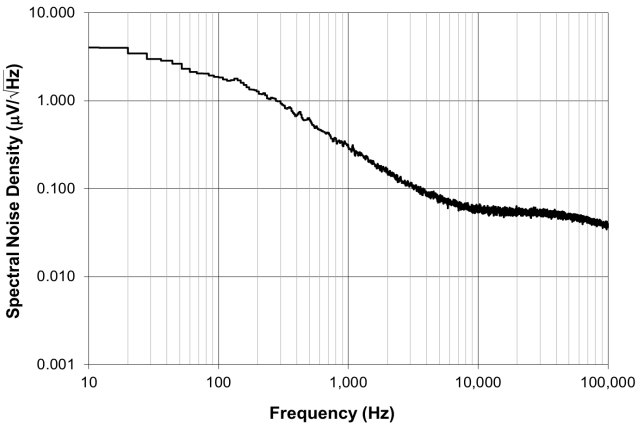


Figure 20. LDO6/7 Output Noise vs. Frequency, 300 mA Load

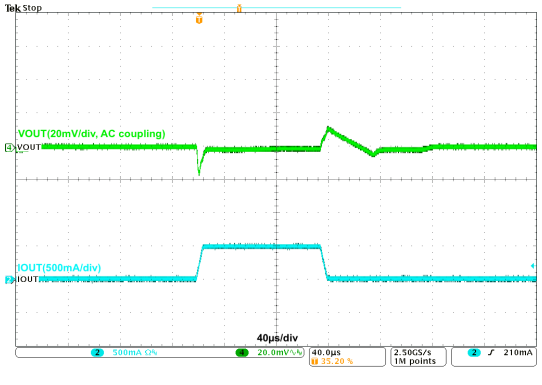


Figure 21. LDO1/2 Load Transient, V_{IN} = 1.3 V, V_{OUT} = 1.05 V, 1 mA ↔ 500 mA, 5 µs Edge

TYPICAL CHARACTERISTICS (continued)

(UNLESS OTHERWISE NOTED, T_A = 25°C, V_{SYS} = 3.8 V, V_{IN12} = 1.3 V, V_{IN34}, V_{IN6}, V_{IN7} = 3.8 V, V_{IN5} = 2.05 V, $V_{LDO1/2}$ = 1.05 V, $V_{LDO3/4}$ = 2.8 V, V_{LDO5} = 1.8 V AND $V_{LDO6/7}$ = 2.8 V, RECOMMENDED LAYOUT AND EXTERNAL COMPONENTS.)

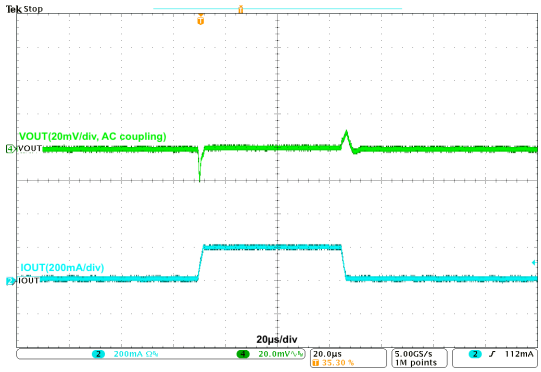


Figure 22. LDO3/4 Load Transient, V_{IN} = 3.8 V, V_{OUT} = 2.8 V, 1 mA ↔ 200 mA, 2 µs Edge

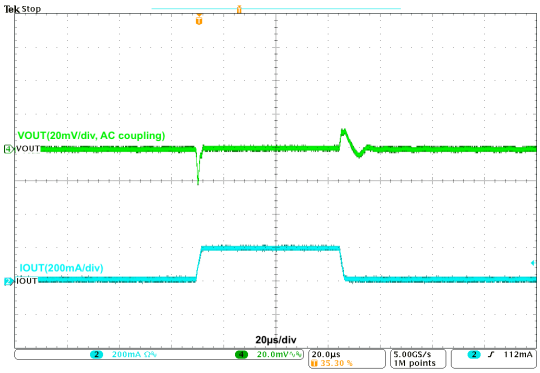


Figure 23. LDO5 Load Transient, V_{IN} = 2.05 V, V_{OUT} = 1.8 V, 1 mA ↔ 200 mA, 2 µs Edge

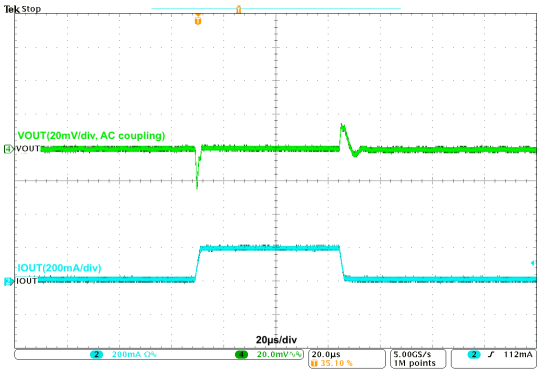


Figure 24. LDO6/7 Load Transient, V_{IN} = 3.8 V, V_{OUT} = 2.8 V, 1 mA ↔ 200 mA, 2 µs Edge

FUNCTIONAL SPECIFICATIONS

Device Operation

Overview

The FAN53870 micro Power Management IC(PMIC) is optimized to supply different sub systems of battery powered mobile applications. It integrates seven low−dropout regulators: two high current LDOs, three ultra low noise / high PSRR LDOs, two general purpose LDOs.

The features of the FAN53870 can be programmed through an I^2C interface.

Under Voltage Lockout (UVLO)

When enabling, if VSYS is above Power−On Reset (POR) voltage but below its UVLO rising threshold, or if VINs of the LDOs are below their UVLO rising threshold, the assigned UVLO interrupt bit and UVLO status bit will be set, and the Interrupt pin asserted. The UVLO status bit remains set as long as the input voltage is below its UVLO rising threshold.

When VSYS or VINs fall below their UVLO falling threshold, the LDO(s) will shut down, an UVLO interrupt will be declared. The UVLO status bit remains set until the input voltage rises above its UVLO rising threshold, and the LDO(s) performs startup immediately.

The suspend bits will be set upon shutdown. The LDO(s) will stay in shutdown for a minimum of 20 ms and then attempt a restart if VSYS or VINs have risen above their UVLO rising threshold. The suspend bits are cleared upon restart. The LDO(s) will be disabled permanently after the 4th UVLO fault.

Thermal Management

When the die temperature rises to a nominal 125°C, the thermal Warning status bit will be set to “1” and remain set until the die temperature drops to a nominal 110°C.

If the die temperature continues to rise to a nominal 140°C, a Thermal Shutdown event is activated, all the LDOs are disabled, the Thermal Shutdown interrupt bit is set but I^2C communication remains. The Thermal Shutdown status bit is also set and will remain set as long as the device is above the Thermal Warning temperature. The chip suspend bit is set upon shutdown.

After the die temperature falls below the Thermal Warning threshold, the Thermal Shutdown status and chip suspend bits will be cleared, and the device will return to the operating conditions prior to the thermal shutdown event.

Enabling / Disabling

The FAN53870 LDOs can be enabled and disabled independently with the LDOx_EN bits in the ENABLE register.

To enable FAN53870 LDOs, with RESET_B pin high, set the LDOx_EN bits to “1”. The FAN53870 LDOs have internal soft−start, which limits the inrush current to the ILIM setting. The LDOs will ignore faults during the first 1.5 ms at startup. After 1.5 ms, if the LDO output fails to reach the UVP rising threshold, an UVP fault will be declared.

To disable the FAN53870 LDOs, set the LDOx_EN bits to “0”. The active discharge feature is enabled by default, with which, an 100 Ω resister is connected between VOUT and GND to discharge the output capacitors when the LDOx_en bits are set to “0”.

To do a global shutdown of all LDOs, set RESET_B pin low.

Over−current Protection (OCP)

The LDOs are protected from excessive load and short−circuit. The current limit level can be programmed through the I^2C interface.

When an over−load event occurs, the current is automatically limited to the programmed current limit. And once the current limit is detected, the associated OCP status bit is set, and if the LDO remains in current limit for more than 1 ms, the OCP interrupt bit will be set, and the Interrupt pin asserted. Then the LDO will shut down permanently without attempting any restart, meanwhile the associated suspend bit is set and status bit is cleared.

The OCP debounce timer is programmable through I^2C. Hiccup mode option is also available for OCP, which can be accommodated by contacting an **onsemi** representative.

Under Voltage Protection (UVP)

If the output voltage falls approximately 20% (10% for LDO1/2) below the target VOUT, the associated UVP status bit will be set. If the fault persists for more than 50 μs, the UVP interrupt bit will be set, and the Interrupt pin asserted. The LDO will then be disabled, the associated status bit is cleared and the suspend bit is set. The interrupt bit will be cleared upon a read of the bit.

The LDO will attempt a restart in 20 ms and the suspend bit will be reset to “0” upon restart. And after the 4th UVP fault, the LDO shuts down permanently.

4−Fault Shutdown

To prevent repetitive starting and faulting of an LDO or of the IC itself, detection of 4 failures will result in a permanent shutdown of the LDO, or if it is a system fault, the entire IC will shut down permanently.

Individual LDO Fault: the LDO will be latched−off after the 4th individual LDO fault (any combination of UVP, and/or OCP, and/or VINx UVLO), and the LDOx_EN bit will be cleared. In order to clear the latch−off and re−enable the LDOs, set the LDOx_EN bits to “1”.

Chip Fault: all the LDOs will be latched−off after the 4th chip fault (any combination of Thermal Shutdown, and/or VSYS UVLO) with all the LDOx_EN bits cleared. In order to clear the latch−off, RESET_B pin needs to be pulled low.

Reset

When the RESET_B pin is pulled LOW, the INTERRUPTx and STATUSx bits will be cleared. All the other registers will remain set to their programmed values, but I²C communication with the device is disabled. Additionally, all internal fault counters will reset to 0.

When the RESET_B pin is pulled HIGH, the I²C block is turned on. The Reset_B pin should not be asserted high while there is data transmission on the I²C bus. This will ensure the FAN53870 doesn't mis−interpret a logic low on SDA as a falling edge and inadvertently create a "Start" condition, and unintended data written to the FAN53870 registers. It is recommended that the FAN53870 is enabled when there is a brief break in I²C data transmissions.

The SOFT_RESET bits in the RESET register can be used to clear all registers to their default values.

Power Up/Down Sequence

Power up and power down sequence can be programmed and controlled with the dedicated registers xxxx_SEQ and SEQUENCING.

If an LDO faults during a start−up sequence, the other LDOs will still be starting up in their assigned time slot. The xxxx_SEQ register bits for the faulted LDO will remain set to the previously values. The system can then attempt to start the faulted LDO in another sequence by setting the SEQ_CONTROL bits to "01" or by clearing the xxxx_SEQ bits to "000" and writing a "1" to the enable bit for the faulted LDO.

No Fault Shutdown

FAN53870 provides a "No Fault Shutdown" feature, which prevents LDOs from shutting down during an OCP or UVP event . It is activated by setting the FLT_SD_B bit in RESET register to "1".

By setting FLT_SD_B to "1", it prevents the shutdown during an OCP or UVP event, but not during LDO VIN UVLO event. With FLT_SD_B=1, when LDO VIN UVLO, OCP or OVP event occurs, the interrupt and status bits will still indicate the fault has occurred, but the fault counter will not be incremented.

I²C Functionality

I²C Interface

The FAN53870 serial interface is compatible with Standard, Fast and Fast Plus Mode I²C Bus specifications. The SCL line is an input and its SDA line is a bi−directional open−drain output; it can only pull down the bus when active. The SDA line only pulls LOW during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

Please refer to the *Reset* section for guidance on RESET_B LOW to HIGH pin timing for proper enabling of the I²C block.

I2C Slave Address

The default I²C slave address is shown in Table 3. The LSB of the address byte is used as the read/write bit and is not included in the 7 bit Hex, Decimal or Binary value as shown in Table 3. Table 4 is an example (using the FAN53870) to show the location of the R/W bit.

The I²C address can also be changed by setting in the I2C_ADDR_SEL register.

Other default slave addresses can be accommodated by contacting an **onsemi** representative.

Table 3. I²C SLAVE ADDRESS

Device	Hex	Decimal	7 bit Binary
FAN53870	7'h35	53d	011 0101
FAN53871	7'h20	32d	010 0000

Table 4. I²C (7 bit) SLAVE ADDRESS BYTE

7	6	5	4	3	2	1	0
0	1	1	0	1	0	1	R/W

Bus Timing

As shown in Figure 25, data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow ample time for the data to set up before the next SCL rising edge.

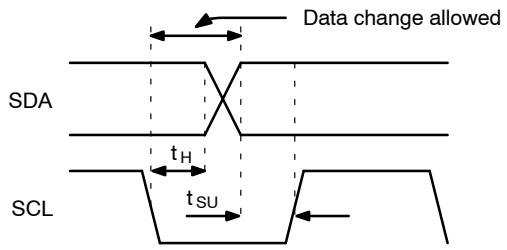


Figure 25. Data Transfer Timing

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown in Figure 26.

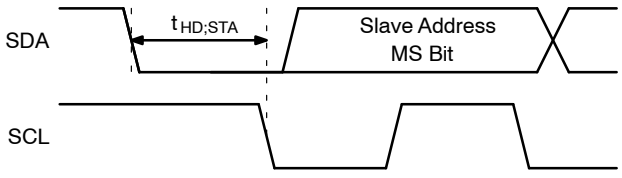


Figure 26. Start Bit

Transactions end with a STOP condition, which is SDA transitioning from 0 to 1 with SCL HIGH, as shown in Figure 27.

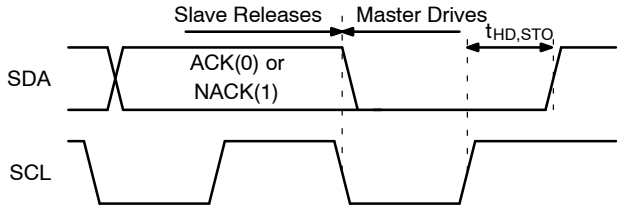


Figure 27. Stop Bit

During a read from the FAN53870, the master issues a Repeated Start after sending the register address and before resending the slave address. The Repeated Start is a 1−to−0 transition on SDA while SCL is HIGH, as shown in Figure 28.

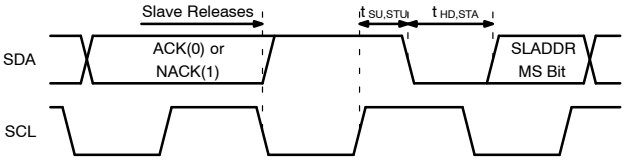


Figure 28. Repeated Start Timing

Read and Write Transactions

The figures below outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as Master Drives Bus and Slave Drives Bus. All addresses and data are MSB first.

Multi−Byte (Sequential) Read and Write Transactions

Sequential Write (Figure 31)

The Slave Address, Reg Addr address, and the first data byte are transmitted to the FAN53870 in the same way as in a single−byte write (Figure 29). However, instead of generating a Stop condition, the master transmits additional bytes that are written to consecutive sequential registers after the falling edge of the eighth bit. After the last byte written and its ACK bit received, the master issues a STOP bit. The IC contains an 8−bit counter that increments the address pointer after each byte is written.

Sequential Read (Figure 32)

Sequential reads are initiated in the same way as a single−byte read (Figure 30), except that once the slave transmits the first data byte, the master issues an acknowledge instead of a STOP condition. This directs the slave's I^2C logic to transmit the next sequentially addressed 8−bit word. The FAN53870 contains an 8−bit counter that increments the address pointer after each byte is read, which allows the entire memory contents to be read during one I^2C transaction.

Figure 29. Single−Byte Write Transaction

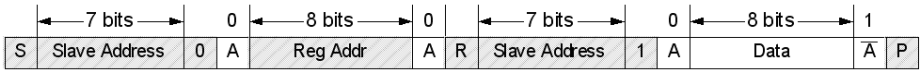


Figure 30. Single−Byte Read Transaction

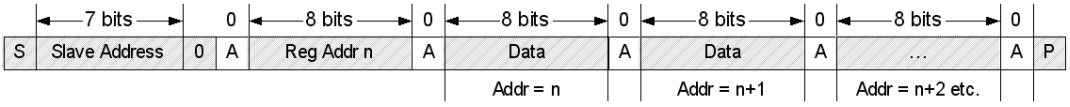


Figure 31. Multi−Byte (Sequential) Write Transaction

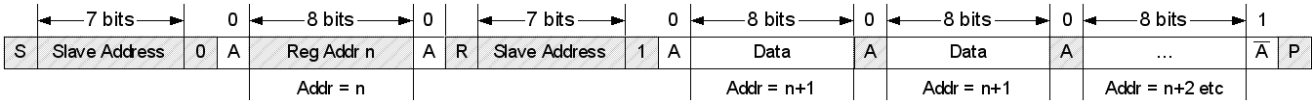


Figure 32. Multi−Byte (Sequential) Read Transaction

REGISTER MAPPING TABLE

Table 5. REGISTER MAPPING

					Read Only	Write Only	Read / Write	Read / Clear	Write / Clear
Address	**Name**	**Bit[7]**	**Bit[6]**	**Bit[5]**	**Bit[4]**	**Bit[3]**	**Bit[2]**	**Bit[1]**	**Bit[0]**
0x00	PRODUCT ID	Product ID							
0x01	SILICON REV ID	Revision							
0x02	IOUT	0	LDO7_ILIM	LDO6_ILIM	LDO5_ILIM	LDO4_ILIM	LDO3_ILIM	LDO2_ILIM	LDO1_ILIM
0x03	ENABLE	0	LDO7_EN	LDO6_EN	LDO5_EN	LDO4_EN	LDO3_EN	LDO2_EN	LDO1_EN
0x04	LDO1	LDO1_VOUT							
0x05	LDO2	LDO2_VOUT							
0x06	LDO3	LDO3_VOUT							
0x07	LDO4	LDO4_VOUT							
0x08	LDO5	LDO5_VOUT							
0x09	LDO6	LDO6_VOUT							
0x0A	LDO7	LDO7_VOUT							
0x0B	LDO12_SEQ	0		LDO2_SEQ			LDO1_SEQ		
0x0C	LDO34_SEQ	0		LDO4_SEQ			LDO3_SEQ		
0x0D	LDO56_SEQ	0		LDO6_SEQ			LDO5_SEQ		
0x0E	LDO7_SEQ	0					LDO7_SEQ		
0x0F	SEQUENCING	SEQ_SPEED		SEQ_CONTROL		SEQ_ON	SEQ_COUNT		
0x10	DISCHARGE	0	LDO1_DIS	LDO2_DIS	LDO3_DIS	LDO4_DIS	LDO5_DIS	LDO6_DIS	LDO7_DIS
0x11	RESET	SOFT_RESET				0	OCP_TIMER		FLT_SD_B
0x12	I2C_ADDR	0						I2C_ADDR_SEL	
0x13	LDO_COMP0	LDO4_COMP_SEL		LDO3_COMP_SEL		LDO2_COMP_SEL		LDO1_COMP_SEL	
0x14	LDO_COMP1	0		LDO7_COMP_SEL		LDO6_COMP_SEL		LDO5_COMP_SEL	
0x15	INTERRUPT1	0	LDO7_UVP_INT	LDO6_UVP_INT	LDO5_UVP_INT	LDO4_UVP_INT	LDO3_UVP_INT	LDO2_UVP_INT	LDO1_UVP_INT
0x16	INTERRUPT2	0	LDO7_OCP_INT	LDO6_OCP_INT	LDO5_OCP_INT	LDO4_OCP_INT	LDO3_OCP_INT	LDO2_OCP_INT	LDO1_OCP_INT
0x17	INTERRUPT3	TSD_INT	TSD_WRN_INT	VSYS_UVLO_INT	LDO7_UVLO_INT	LDO6_UVLO_INT	LDO5_UVLO_INT	LDO34_UVLO_INT	LDO12_UVLO_INT
0x18	STATUS1	0	LDO7_UVP_STAT	LDO6_UVP_STAT	LDO5_UVP_STAT	LDO4_UVP_STAT	LDO3_UVP_STAT	LDO2_UVP_STAT	LDO1_UVP_STAT
0x19	STATUS2	0	LDO7_OCP_STAT	LDO6_OCP_STAT	LDO5_OCP_STAT	LDO4_OCP_STAT	LDO3_OCP_STAT	LDO2_OCP_STAT	LDO1_OCP_STAT
0x1A	STATUS3	TSD_STAT	TSD_WRN_STAT	VSYS_UVLO_STAT	LDO7_UVLO_STAT	LDO6_UVLO_STAT	LDO5_UVLO_STAT	LDO34_UVLO_STAT	LDO12_UVLO_STAT
0x1B	STATUS4	CHIP_SUSD	LDO7_SUSD	LDO6_SUSD	LDO5_SUSD	LDO4_SUSD	LDO3_SUSD	LDO2_SUSD	LDO1_SUSD
0x1C	MINT1	0	MASK_LDO7_UVP	MASK_LDO6_UVP	MASK_LDO5_UVP	MASK_LDO4_UVP	MASK_LDO3_UVP	MASK_LDO2_UVP	MASK_LDO1_UVP
0x1D	MINT2	0	MASK_LDO7_OCP	MASK_LDO6_OCP	MASK_LDO5_OCP	MASK_LDO4_OCP	MASK_LDO3_OCP	MASK_LDO2_OCP	MASK_LDO1_OCP
0x1E	MINT3	MASK_TSD	MASK_TSD_WRN	MASK_VSYS_UVLO	MASK_LDO7_UVLO	MASK_LDO6_UVLO	MASK_LDO5_UVLO	MASK_LDO34_UVLO	MASK_LDO12_UVLO

REGISTER DETAILS

Table 6. REGISTER DETAILS – 0x00 PRODUCT ID

0x00 PRODUCT ID				Default = 00000001	
Bit	**Name**	**Default**	**Type**	**Description**	
7:0	Product ID	00000001	Read	Identifies vendor and device type	
				Code	**Product**
				00000001	FAN53870

Table 7. REGISTER DETAILS – 0x01 SILICON REV ID

0x01 SILICON REV ID				Default = 00000001
Bit	**Name**	**Default**	**Type**	**Description**
7:0	Revision	00000001	Read	Identifies silicon revision

Table 8. REGISTER DETAILS – 0x02 IOUT

0x02 IOUT				Default = 01111111	
Bit	**Name**	**Default**	**Type**	**Description**	
7	UNUSED				
6	LDO7_ILIM	1	R/W	**Code**	**Current Limit**
				0	400 mA
				1	650 mA
5	LDO6_ILIM	1	R/W	**Code**	**Current Limit**
				0	400 mA
				1	650 mA
4	LDO5_ILIM	1	R/W	**Code**	**Current Limit**
				0	400 mA
				1	650 mA
3	LDO4_ILIM	1	R/W	**Code**	**Current Limit**
				0	400 mA
				1	650 mA
2	LDO3_ILIM	1	R/W	**Code**	**Current Limit**
				0	400 mA
				1	650 mA
1	LDO2_ILIM	1	R/W	**Code**	**Current Limit**
				0	925 mA
				1	1250 mA
0	LDO1_ILIM	1	R/W	**Code**	**Current Limit**
				0	925 mA
				1	1250 mA

Table 9. REGISTER DETAILS – 0x03 ENABLE

0x03 ENABLE				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7	UNUSED				
6	LDO7_EN	0	R/W	Enable bit for LDO7. This bit only controls the state of LDO7 if LDO7_SEQ = 000.	
				Code	**Status of LDO**
				0	Disabled
				1	Enabled
5	LDO6_EN	0	R/W	Enable bit for LDO6. This bit only controls the state of LDO6 if LDO6_SEQ = 000.	
				Code	**Status of LDO**
				0	Disabled
				1	Enabled
4	LDO5_EN	0	R/W	Enable bit for LDO5. This bit only controls the state of LDO5 if LDO5_SEQ = 000.	
				Code	**Status of LDO**
				0	Disabled
				1	Enabled
3	LDO4_EN	0	R/W	Enable bit for LDO4. This bit only controls the state of LDO4 if LDO4_SEQ = 000.	
				Code	**Status of LDO**
				0	Disabled
				1	Enabled
2	LDO3_EN	0	R/W	Enable bit for LDO3. This bit only controls the state of LDO3 if LDO3_SEQ = 000.	
				Code	**Status of LDO**
				0	Disabled
				1	Enabled
1	LDO2_EN	0	R/W	Enable bit for LDO2. This bit only controls the state of LDO2 if LDO2_SEQ = 000.	
				Code	**Status of LDO**
				0	Disabled
				1	Enabled
0	LDO1_EN	0	R/W	Enable bit for LDO1. This bit only controls the state of LDO1 if LDO1_SEQ = 000.	
				Code	**Status of LDO**
				0	Disabled
				1	Enabled

Table 10. REGISTER DETAILS – 0x04 LDO1

0x04 LDO1				Default = 00000000							
Bit	**Name**	**Default**	**Type**	**Description**							
7:0	LDO1_VOUT	00000000	R/W	Sets LDO1 regulation target voltage. Equation: Vout = 0.800 V + [(d – 99) x 8 mV], where d is the decimal value of the register							
				Hex	**VOUT**	**Hex**	**VOUT**	**Hex**	**VOUT**	**Hex**	**VOUT**
				00	**DEFAULT**	40	Reserved	80	1.032 V	C0	Reserved
				01	Reserved	41	Reserved	81	1.040 V	C1	Reserved
				02	Reserved	42	Reserved	82	1.048 V	C2	Reserved
				03	Reserved	43	Reserved	83	1.056 V	C3	Reserved
				04	Reserved	44	Reserved	84	1.064 V	C4	Reserved
				05	Reserved	45	Reserved	85	1.072 V	C5	Reserved
				06	Reserved	46	Reserved	86	1.080 V	C6	Reserved
				07	Reserved	47	Reserved	87	1.088 V	C7	Reserved
				08	Reserved	48	Reserved	88	1.096 V	C8	Reserved
				09	Reserved	49	Reserved	89	1.104 V	C9	Reserved
				0A	Reserved	4A	Reserved	8A	1.112 V	CA	Reserved
				0B	Reserved	4B	Reserved	8B	1.120 V	CB	Reserved
				0C	Reserved	4C	Reserved	8C	1.128 V	CC	Reserved
				0D	Reserved	4D	Reserved	8D	1.136 V	CD	Reserved
				0E	Reserved	4E	Reserved	8E	1.144 V	CE	Reserved
				0F	Reserved	4F	Reserved	8F	1.152 V	CF	Reserved
				10	Reserved	50	Reserved	90	1.160 V	D0	Reserved
				11	Reserved	51	Reserved	91	1.168 V	D1	Reserved
				12	Reserved	52	Reserved	92	1.176 V	D2	Reserved
				13	Reserved	53	Reserved	93	1.184 V	D3	Reserved
				14	Reserved	54	Reserved	94	1.192 V	D4	Reserved
				15	Reserved	55	Reserved	95	1.200 V	D5	Reserved
				16	Reserved	56	Reserved	96	1.208 V	D6	Reserved
				17	Reserved	57	Reserved	97	1.216 V	D7	Reserved
				18	Reserved	58	Reserved	98	1.224 V	D8	Reserved
				19	Reserved	59	Reserved	99	1.232 V	D9	Reserved
				1A	Reserved	5A	Reserved	9A	1.240 V	DA	Reserved
				1B	Reserved	5B	Reserved	9B	1.248 V	DB	Reserved
				1C	Reserved	5C	Reserved	9C	1.256 V	DC	Reserved
				1D	Reserved	5D	Reserved	9D	1.264 V	DD	Reserved
				1E	Reserved	5E	Reserved	9E	1.272 V	DE	Reserved
				1F	Reserved	5F	Reserved	9F	1.280 V	DF	Reserved
				20	Reserved	60	Reserved	A0	1.288 V	E0	Reserved
				21	Reserved	61	Reserved	A1	1.296 V	E1	Reserved
				22	Reserved	62	Reserved	A2	1.304 V	E2	Reserved
				23	Reserved	63	0.800 V	A3	1.312 V	E3	Reserved
				24	Reserved	64	0.808 V	A4	1.320 V	E4	Reserved

Table 10. REGISTER DETAILS – 0x04 LDO1 (continued)

0x04 LDO1				Default = 00000000							
Bit	Name	Default	Type	Description							
				Hex	VOUT	Hex	VOUT	Hex	VOUT	Hex	VOUT
				25	Reserved	65	0.816 V	A5	1.328 V	E5	Reserved
				26	Reserved	66	0.824 V	A6	1.336 V	E6	Reserved
				27	Reserved	67	0.832 V	A7	1.344 V	E7	Reserved
				28	Reserved	68	0.840 V	A8	1.352 V	E8	Reserved
				29	Reserved	69	0.848 V	A9	1.360 V	E9	Reserved
				2A	Reserved	6A	0.856 V	AA	1.368 V	EA	Reserved
				2B	Reserved	6B	0.864 V	AB	1.376 V	EB	Reserved
				2C	Reserved	6C	0.872 V	AC	1.384 V	EC	Reserved
				2D	Reserved	6D	0.880 V	AD	1.392 V	ED	Reserved
				2E	Reserved	6E	0.888 V	AE	1.400 V	EE	Reserved
				2F	Reserved	6F	0.896 V	AF	1.408 V	EF	Reserved
				30	Reserved	70	0.904 V	B0	1.416 V	F0	Reserved
				31	Reserved	71	0.912 V	B1	1.424 V	F1	Reserved
				32	Reserved	72	0.920 V	B2	1.432 V	F2	Reserved
				33	Reserved	73	0.928 V	B3	1.440 V	F3	Reserved
				34	Reserved	74	0.936 V	B4	1.448 V	F4	Reserved
				35	Reserved	75	0.944 V	B5	1.456 V	F5	Reserved
				36	Reserved	76	0.952 V	B6	1.464 V	F6	Reserved
				37	Reserved	77	0.960 V	B7	1.472 V	F7	Reserved
				38	Reserved	78	0.968 V	B8	1.480 V	F8	Reserved
				39	Reserved	79	0.976 V	B9	1.488 V	F9	Reserved
				3A	Reserved	7A	0.984 V	BA	1.496 V	FA	Reserved
				3B	Reserved	7B	0.992 V	BB	1.504 V	FB	Reserved
				3C	Reserved	7C	1.000 V	BC	Reserved	FC	Reserved
				3D	Reserved	7D	1.008 V	BD	Reserved	FD	Reserved
				3E	Reserved	7E	1.016 V	BE	Reserved	FE	Reserved
				3F	Reserved	7F	1.024 V	BF	Reserved	FF	Reserved

Table 11. REGISTER DETAILS – 0x05 LDO2

0x05 LDO2				Default = 00000000							
Bit	**Name**	**Default**	**Type**	**Description**							
7:0	LDO2_VOUT	00000000	R/W	Sets LDO2 regulation target voltage. Equation: Vout = 0.800 V + [(d – 99) x 8 mV], where d is the decimal value of the register							
				Hex	**VOUT**	**Hex**	**VOUT**	**Hex**	**VOUT**	**Hex**	**VOUT**
				00	**DEFAULT**	40	Reserved	80	1.032 V	C0	Reserved
				01	Reserved	41	Reserved	81	1.040 V	C1	Reserved
				02	Reserved	42	Reserved	82	1.048 V	C2	Reserved
				03	Reserved	43	Reserved	83	1.056 V	C3	Reserved
				04	Reserved	44	Reserved	84	1.064 V	C4	Reserved
				05	Reserved	45	Reserved	85	1.072 V	C5	Reserved
				06	Reserved	46	Reserved	86	1.080 V	C6	Reserved
				07	Reserved	47	Reserved	87	1.088 V	C7	Reserved
				08	Reserved	48	Reserved	88	1.096 V	C8	Reserved
				09	Reserved	49	Reserved	89	1.104 V	C9	Reserved
				0A	Reserved	4A	Reserved	8A	1.112 V	CA	Reserved
				0B	Reserved	4B	Reserved	8B	1.120 V	CB	Reserved
				0C	Reserved	4C	Reserved	8C	1.128 V	CC	Reserved
				0D	Reserved	4D	Reserved	8D	1.136 V	CD	Reserved
				0E	Reserved	4E	Reserved	8E	1.144 V	CE	Reserved
				0F	Reserved	4F	Reserved	8F	1.152 V	CF	Reserved
				10	Reserved	50	Reserved	90	1.160 V	D0	Reserved
				11	Reserved	51	Reserved	91	1.168 V	D1	Reserved
				12	Reserved	52	Reserved	92	1.176 V	D2	Reserved
				13	Reserved	53	Reserved	93	1.184 V	D3	Reserved
				14	Reserved	54	Reserved	94	1.192 V	D4	Reserved
				15	Reserved	55	Reserved	95	1.200 V	D5	Reserved
				16	Reserved	56	Reserved	96	1.208 V	D6	Reserved
				17	Reserved	57	Reserved	97	1.216 V	D7	Reserved
				18	Reserved	58	Reserved	98	1.224 V	D8	Reserved
				19	Reserved	59	Reserved	99	1.232 V	D9	Reserved
				1A	Reserved	5A	Reserved	9A	1.240 V	DA	Reserved
				1B	Reserved	5B	Reserved	9B	1.248 V	DB	Reserved
				1C	Reserved	5C	Reserved	9C	1.256 V	DC	Reserved
				1D	Reserved	5D	Reserved	9D	1.264 V	DD	Reserved
				1E	Reserved	5E	Reserved	9E	1.272 V	DE	Reserved
				1F	Reserved	5F	Reserved	9F	1.280 V	DF	Reserved
				20	Reserved	60	Reserved	A0	1.288 V	E0	Reserved
				21	Reserved	61	Reserved	A1	1.296 V	E1	Reserved
				22	Reserved	62	Reserved	A2	1.304 V	E2	Reserved
				23	Reserved	63	0.800 V	A3	1.312 V	E3	Reserved
				24	Reserved	64	0.808 V	A4	1.320 V	E4	Reserved

Table 11. REGISTER DETAILS – 0x05 LDO2 (continued)

0x05 LDO2				Default = 00000000							
Bit	Name	Default	Type	Description							
				Hex	VOUT	Hex	VOUT	Hex	VOUT	Hex	VOUT
				25	Reserved	65	0.816 V	A5	1.328 V	E5	Reserved
				26	Reserved	66	0.824 V	A6	1.336 V	E6	Reserved
				27	Reserved	67	0.832 V	A7	1.344 V	E7	Reserved
				28	Reserved	68	0.840 V	A8	1.352 V	E8	Reserved
				29	Reserved	69	0.848 V	A9	1.360 V	E9	Reserved
				2A	Reserved	6A	0.856 V	AA	1.368 V	EA	Reserved
				2B	Reserved	6B	0.864 V	AB	1.376 V	EB	Reserved
				2C	Reserved	6C	0.872 V	AC	1.384 V	EC	Reserved
				2D	Reserved	6D	0.880 V	AD	1.392 V	ED	Reserved
				2E	Reserved	6E	0.888 V	AE	1.400 V	EE	Reserved
				2F	Reserved	6F	0.896 V	AF	1.408 V	EF	Reserved
				30	Reserved	70	0.904 V	B0	1.416 V	F0	Reserved
				31	Reserved	71	0.912 V	B1	1.424 V	F1	Reserved
				32	Reserved	72	0.920 V	B2	1.432 V	F2	Reserved
				33	Reserved	73	0.928 V	B3	1.440 V	F3	Reserved
				34	Reserved	74	0.936 V	B4	1.448 V	F4	Reserved
				35	Reserved	75	0.944 V	B5	1.456 V	F5	Reserved
				36	Reserved	76	0.952 V	B6	1.464 V	F6	Reserved
				37	Reserved	77	0.960 V	B7	1.472 V	F7	Reserved
				38	Reserved	78	0.968 V	B8	1.480 V	F8	Reserved
				39	Reserved	79	0.976 V	B9	1.488 V	F9	Reserved
				3A	Reserved	7A	0.984 V	BA	1.496 V	FA	Reserved
				3B	Reserved	7B	0.992 V	BB	1.504 V	FB	Reserved
				3C	Reserved	7C	1.000 V	BC	Reserved	FC	Reserved
				3D	Reserved	7D	1.008 V	BD	Reserved	FD	Reserved
				3E	Reserved	7E	1.016 V	BE	Reserved	FE	Reserved
				3F	Reserved	7F	1.024 V	BF	Reserved	FF	Reserved

Table 12. REGISTER DETAILS – 0x06 LDO3

0x06 LDO3				Default = 00000000							
Bit	**Name**	**Default**	**Type**	**Description**							
7:0	LDO3_VOUT	00000000	R/W	Sets LDO3 regulation target voltage. Equation: Vout = 1.500 V + [(d – 16) x 8 mV], where d is the decimal value of the register							
				Hex	**VOUT**	**Hex**	**VOUT**	**Hex**	**VOUT**	**Hex**	**VOUT**
				00	**DEFAULT**	40	1.884 V	80	2.396 V	C0	2.908 V
				01	Reserved	41	1.892 V	81	2.404 V	C1	2.916 V
				02	Reserved	42	1.900 V	82	2.412 V	C2	2.924 V
				03	Reserved	43	1.908 V	83	2.420 V	C3	2.932 V
				04	Reserved	44	1.916 V	84	2.428 V	C4	2.940 V
				05	Reserved	45	1.924 V	85	2.436 V	C5	2.948 V
				06	Reserved	46	1.932 V	86	2.444 V	C6	2.956 V
				07	Reserved	47	1.940 V	87	2.452 V	C7	2.964 V
				08	Reserved	48	1.948 V	88	2.460 V	C8	2.972 V
				09	Reserved	49	1.956 V	89	2.468 V	C9	2.980 V
				0A	Reserved	4A	1.964 V	8A	2.476 V	CA	2.988 V
				0B	Reserved	4B	1.972 V	8B	2.484 V	CB	2.996 V
				0C	Reserved	4C	1.980 V	8C	2.492 V	CC	3.004 V
				0D	Reserved	4D	1.988 V	8D	2.500 V	CD	3.012 V
				0E	Reserved	4E	1.996 V	8E	2.508 V	CE	3.020 V
				0F	Reserved	4F	2.004 V	8F	2.516 V	CF	3.028 V
				10	1.500 V	50	2.012 V	90	2.524 V	D0	3.036 V
				11	1.508 V	51	2.020 V	91	2.532 V	D1	3.044 V
				12	1.516 V	52	2.028 V	92	2.540 V	D2	3.052 V
				13	1.524 V	53	2.036 V	93	2.548 V	D3	3.060 V
				14	1.532 V	54	2.044 V	94	2.556 V	D4	3.068 V
				15	1.540 V	55	2.052 V	95	2.564 V	D5	3.076 V
				16	1.548 V	56	2.060 V	96	2.572 V	D6	3.084 V
				17	1.556 V	57	2.068 V	97	2.580 V	D7	3.092 V
				18	1.564 V	58	2.076 V	98	2.588 V	D8	3.100 V
				19	1.572 V	59	2.084 V	99	2.596 V	D9	3.108 V
				1A	1.580 V	5A	2.092 V	9A	2.604 V	DA	3.116 V
				1B	1.588 V	5B	2.100 V	9B	2.612 V	DB	3.124 V
				1C	1.596 V	5C	2.108 V	9C	2.620 V	DC	3.132 V
				1D	1.604 V	5D	2.116 V	9D	2.628 V	DD	3.140 V
				1E	1.612 V	5E	2.124 V	9E	2.636 V	DE	3.148 V
				1F	1.620 V	5F	2.132 V	9F	2.644 V	DF	3.156 V
				20	1.628 V	60	2.140 V	A0	2.652 V	E0	3.164 V
				21	1.636 V	61	2.148 V	A1	2.660 V	E1	3.172 V
				22	1.644 V	62	2.156 V	A2	2.668 V	E2	3.180 V
				23	1.652 V	63	2.164 V	A3	2.676 V	E3	3.188 V
				24	1.660 V	64	2.172 V	A4	2.684 V	E4	3.196 V

Table 12. REGISTER DETAILS – 0x06 LDO3 (continued)

0x06 LDO3				Default = 00000000							
Bit	Name	Default	Type	Description							
				Hex	VOUT	Hex	VOUT	Hex	VOUT	Hex	VOUT
				25	1.668 V	65	2.180 V	A5	2.692 V	E5	3.204 V
				26	1.676 V	66	2.188 V	A6	2.700 V	E6	3.212 V
				27	1.684 V	67	2.196 V	A7	2.708 V	E7	3.220 V
				28	1.692 V	68	2.204 V	A8	2.716 V	E8	3.228 V
				29	1.700 V	69	2.212 V	A9	2.724 V	E9	3.236 V
				2A	1.708 V	6A	2.220 V	AA	2.732 V	EA	3.244 V
				2B	1.716 V	6B	2.228 V	AB	2.740 V	EB	3.252 V
				2C	1.724 V	6C	2.236 V	AC	2.748 V	EC	3.260 V
				2D	1.732 V	6D	2.244 V	AD	2.756 V	ED	3.268 V
				2E	1.740 V	6E	2.252 V	AE	2.764 V	EE	3.276 V
				2F	1.748 V	6F	2.260 V	AF	2.772 V	EF	3.284 V
				30	1.756 V	70	2.268 V	B0	2.780 V	F0	3.292 V
				31	1.764 V	71	2.276 V	B1	2.788 V	F1	3.300 V
				32	1.772 V	72	2.284 V	B2	2.796 V	F2	3.308 V
				33	1.780 V	73	2.292 V	B3	2.804 V	F3	3.316 V
				34	1.788 V	74	2.300 V	B4	2.812 V	F4	3.324 V
				35	1.796 V	75	2.308 V	B5	2.820 V	F5	3.332 V
				36	1.804 V	76	2.316 V	B6	2.828 V	F6	3.340 V
				37	1.812 V	77	2.324 V	B7	2.836 V	F7	3.348 V
				38	1.820 V	78	2.332 V	B8	2.844 V	F8	3.356 V
				39	1.828 V	79	2.340 V	B9	2.852 V	F9	3.364 V
				3A	1.836 V	7A	2.348 V	BA	2.860 V	FA	3.372 V
				3B	1.844 V	7B	2.356 V	BB	2.868 V	FB	3.380 V
				3C	1.852 V	7C	2.364 V	BC	2.876 V	FC	3.388 V
				3D	1.860 V	7D	2.372 V	BD	2.884 V	FD	3.396 V
				3E	1.868 V	7E	2.380 V	BE	2.892 V	FE	3.404 V
				3F	1.876 V	7F	2.388 V	BF	2.900 V	FF	3.412 V

Table 13. REGISTER DETAILS – 0x07 LDO4

0x07 LDO4				Default = 00000000							
Bit	**Name**	**Default**	**Type**	**Description**							
7:0	LDO4_VOUT	00000000	R/W	Sets LDO4 regulation target voltage. Equation: Vout = 1.500 V + [(d – 16) x 8 mV], where d is the decimal value of the register							
				Hex	**VOUT**	**Hex**	**VOUT**	**Hex**	**VOUT**	**Hex**	**VOUT**
				00	**DEFAULT**	40	1.884 V	80	2.396 V	C0	2.908 V
				01	Reserved	41	1.892 V	81	2.404 V	C1	2.916 V
				02	Reserved	42	1.900 V	82	2.412 V	C2	2.924 V
				03	Reserved	43	1.908 V	83	2.420 V	C3	2.932 V
				04	Reserved	44	1.916 V	84	2.428 V	C4	2.940 V
				05	Reserved	45	1.924 V	85	2.436 V	C5	2.948 V
				06	Reserved	46	1.932 V	86	2.444 V	C6	2.956 V
				07	Reserved	47	1.940 V	87	2.452 V	C7	2.964 V
				08	Reserved	48	1.948 V	88	2.460 V	C8	2.972 V
				09	Reserved	49	1.956 V	89	2.468 V	C9	2.980 V
				0A	Reserved	4A	1.964 V	8A	2.476 V	CA	2.988 V
				0B	Reserved	4B	1.972 V	8B	2.484 V	CB	2.996 V
				0C	Reserved	4C	1.980 V	8C	2.492 V	CC	3.004 V
				0D	Reserved	4D	1.988 V	8D	2.500 V	CD	3.012 V
				0E	Reserved	4E	1.996 V	8E	2.508 V	CE	3.020 V
				0F	Reserved	4F	2.004 V	8F	2.516 V	CF	3.028 V
				10	1.500 V	50	2.012 V	90	2.524 V	D0	3.036 V
				11	1.508 V	51	2.020 V	91	2.532 V	D1	3.044 V
				12	1.516 V	52	2.028 V	92	2.540 V	D2	3.052 V
				13	1.524 V	53	2.036 V	93	2.548 V	D3	3.060 V
				14	1.532 V	54	2.044 V	94	2.556 V	D4	3.068 V
				15	1.540 V	55	2.052 V	95	2.564 V	D5	3.076 V
				16	1.548 V	56	2.060 V	96	2.572 V	D6	3.084 V
				17	1.556 V	57	2.068 V	97	2.580 V	D7	3.092 V
				18	1.564 V	58	2.076 V	98	2.588 V	D8	3.100 V
				19	1.572 V	59	2.084 V	99	2.596 V	D9	3.108 V
				1A	1.580 V	5A	2.092 V	9A	2.604 V	DA	3.116 V
				1B	1.588 V	5B	2.100 V	9B	2.612 V	DB	3.124 V
				1C	1.596 V	5C	2.108 V	9C	2.620 V	DC	3.132 V
				1D	1.604 V	5D	2.116 V	9D	2.628 V	DD	3.140 V
				1E	1.612 V	5E	2.124 V	9E	2.636 V	DE	3.148 V
				1F	1.620 V	5F	2.132 V	9F	2.644 V	DF	3.156 V
				20	1.628 V	60	2.140 V	A0	2.652 V	E0	3.164 V
				21	1.636 V	61	2.148 V	A1	2.660 V	E1	3.172 V
				22	1.644 V	62	2.156 V	A2	2.668 V	E2	3.180 V
				23	1.652 V	63	2.164 V	A3	2.676 V	E3	3.188 V
				24	1.660 V	64	2.172 V	A4	2.684 V	E4	3.196 V

Table 13. REGISTER DETAILS – 0x07 LDO4 (continued)

0x07 LDO4				Default = 00000000							
Bit	Name	Default	Type	Description							
				Hex	VOUT	Hex	VOUT	Hex	VOUT	Hex	VOUT
				25	1.668 V	65	2.180 V	A5	2.692 V	E5	3.204 V
				26	1.676 V	66	2.188 V	A6	2.700 V	E6	3.212 V
				27	1.684 V	67	2.196 V	A7	2.708 V	E7	3.220 V
				28	1.692 V	68	2.204 V	A8	2.716 V	E8	3.228 V
				29	1.700 V	69	2.212 V	A9	2.724 V	E9	3.236 V
				2A	1.708 V	6A	2.220 V	AA	2.732 V	EA	3.244 V
				2B	1.716 V	6B	2.228 V	AB	2.740 V	EB	3.252 V
				2C	1.724 V	6C	2.236 V	AC	2.748 V	EC	3.260 V
				2D	1.732 V	6D	2.244 V	AD	2.756 V	ED	3.268 V
				2E	1.740 V	6E	2.252 V	AE	2.764 V	EE	3.276 V
				2F	1.748 V	6F	2.260 V	AF	2.772 V	EF	3.284 V
				30	1.756 V	70	2.268 V	B0	2.780 V	F0	3.292 V
				31	1.764 V	71	2.276 V	B1	2.788 V	F1	3.300 V
				32	1.772 V	72	2.284 V	B2	2.796 V	F2	3.308 V
				33	1.780 V	73	2.292 V	B3	2.804 V	F3	3.316 V
				34	1.788 V	74	2.300 V	B4	2.812V	F4	3.324 V
				35	1.796 V	75	2.308 V	B5	2.820 V	F5	3.332 V
				36	1.804 V	76	2.316 V	B6	2.828 V	F6	3.340 V
				37	1.812 V	77	2.324 V	B7	2.836 V	F7	3.348 V
				38	1.820 V	78	2.332 V	B8	2.844 V	F8	3.356 V
				39	1.828 V	79	2.340 V	B9	2.852 V	F9	3.364 V
				3A	1.836 V	7A	2.348 V	BA	2.860 V	FA	3.372 V
				3B	1.844 V	7B	2.356 V	BB	2.868 V	FB	3.380 V
				3C	1.852 V	7C	2.364 V	BC	2.876 V	FC	3.388 V
				3D	1.860 V	7D	2.372 V	BD	2.884 V	FD	3.396 V
				3E	1.868 V	7E	2.380 V	BE	2.892 V	FE	3.404 V
				3F	1.876 V	7F	2.388 V	BF	2.900 V	FF	3.412 V

Table 14. REGISTER DETAILS – 0x08 LDO5

0x08 LDO5				Default = 00000000							
Bit	**Name**	**Default**	**Type**	**Description**							
7:0	LDO5_VOUT	00000000	R/W	Sets LDO5 regulation target voltage. Equation: Vout = 1.500 V + [(d – 16) x 8 mV], where d is the decimal value of the register							
				Hex	**VOUT**	**Hex**	**VOUT**	**Hex**	**VOUT**	**Hex**	**VOUT**
				00	DEFAULT	40	1.884 V	80	2.396 V	C0	2.908 V
				01	Reserved	41	1.892 V	81	2.404 V	C1	2.916 V
				02	Reserved	42	1.900 V	82	2.412 V	C2	2.924 V
				03	Reserved	43	1.908 V	83	2.420 V	C3	2.932 V
				04	Reserved	44	1.916 V	84	2.428 V	C4	2.940 V
				05	Reserved	45	1.924 V	85	2.436 V	C5	2.948 V
				06	Reserved	46	1.932 V	86	2.444 V	C6	2.956 V
				07	Reserved	47	1.940 V	87	2.452 V	C7	2.964 V
				08	Reserved	48	1.948 V	88	2.460 V	C8	2.972 V
				09	Reserved	49	1.956 V	89	2.468 V	C9	2.980 V
				0A	Reserved	4A	1.964 V	8A	2.476 V	CA	2.988 V
				0B	Reserved	4B	1.972 V	8B	2.484 V	CB	2.996 V
				0C	Reserved	4C	1.980 V	8C	2.492 V	CC	3.004 V
				0D	Reserved	4D	1.988 V	8D	2.500 V	CD	3.012 V
				0E	Reserved	4E	1.996 V	8E	2.508 V	CE	3.020 V
				0F	Reserved	4F	2.004 V	8F	2.516 V	CF	3.028 V
				10	1.500 V	50	2.012 V	90	2.524 V	D0	3.036 V
				11	1.508 V	51	2.020 V	91	2.532 V	D1	3.044 V
				12	1.516 V	52	2.028 V	92	2.540 V	D2	3.052 V
				13	1.524 V	53	2.036 V	93	2.548 V	D3	3.060 V
				14	1.532 V	54	2.044 V	94	2.556 V	D4	3.068 V
				15	1.540 V	55	2.052 V	95	2.564 V	D5	3.076 V
				16	1.548 V	56	2.060 V	96	2.572 V	D6	3.084 V
				17	1.556 V	57	2.068 V	97	2.580 V	D7	3.092 V
				18	1.564 V	58	2.076 V	98	2.588 V	D8	3.100 V
				19	1.572 V	59	2.084 V	99	2.596 V	D9	3.108 V
				1A	1.580 V	5A	2.092 V	9A	2.604 V	DA	3.116 V
				1B	1.588 V	5B	2.100 V	9B	2.612 V	DB	3.124 V
				1C	1.596 V	5C	2.108 V	9C	2.620 V	DC	3.132 V
				1D	1.604 V	5D	2.116 V	9D	2.628 V	DD	3.140 V
				1E	1.612 V	5E	2.124 V	9E	2.636 V	DE	3.148 V
				1F	1.620 V	5F	2.132 V	9F	2.644 V	DF	3.156 V
				20	1.628 V	60	2.140 V	A0	2.652 V	E0	3.164 V
				21	1.636 V	61	2.148 V	A1	2.660 V	E1	3.172 V
				22	1.644 V	62	2.156 V	A2	2.668 V	E2	3.180 V
				23	1.652 V	63	2.164 V	A3	2.676 V	E3	3.188 V
				24	1.660 V	64	2.172 V	A4	2.684 V	E4	3.196 V

Table 14. REGISTER DETAILS – 0x08 LDO5 (continued)

0x08 LDO5				Default = 00000000							
Bit	Name	Default	Type	Description							
				Hex	VOUT	Hex	VOUT	Hex	VOUT	Hex	VOUT
				25	1.668 V	65	2.180 V	A5	2.692 V	E5	3.204 V
				26	1.676 V	66	2.188 V	A6	2.700 V	E6	3.212 V
				27	1.684 V	67	2.196V	A7	2.708 V	E7	3.220 V
				28	1.692 V	68	2.204 V	A8	2.716 V	E8	3.228 V
				29	1.700 V	69	2.212 V	A9	2.724 V	E9	3.236 V
				2A	1.708 V	6A	2.220 V	AA	2.732 V	EA	3.244 V
				2B	1.716 V	6B	2.228V	AB	2.740 V	EB	3.252 V
				2C	1.724 V	6C	2.236 V	AC	2.748 V	EC	3.260 V
				2D	1.732 V	6D	2.244 V	AD	2.756 V	ED	3.268 V
				2E	1.740 V	6E	2.252 V	AE	2.764 V	EE	3.276 V
				2F	1.748 V	6F	2.260 V	AF	2.772 V	EF	3.284 V
				30	1.756 V	70	2.268 V	B0	2.780 V	F0	3.292 V
				31	1.764 V	71	2.276 V	B1	2.788 V	F1	3.300 V
				32	1.772 V	72	2.284 V	B2	2.796 V	F2	3.308 V
				33	1.780 V	73	2.292 V	B3	2.804 V	F3	3.316 V
				34	1.788 V	74	2.300 V	B4	2.812 V	F4	3.324 V
				35	1.796 V	75	2.308 V	B5	2.820 V	F5	3.332 V
				36	1.804 V	76	2.316V	B6	2.828 V	F6	3.340 V
				37	1.812 V	77	2.324 V	B7	2.836 V	F7	3.348 V
				38	1.820 V	78	2.332 V	B8	2.844 V	F8	3.356 V
				39	1.828 V	79	2.340 V	B9	2.852 V	F9	3.364 V
				3A	1.836 V	7A	2.348 V	BA	2.860 V	FA	3.372 V
				3B	1.844 V	7B	2.356 V	BB	2.868 V	FB	3.380 V
				3C	1.852 V	7C	2.364 V	BC	2.876 V	FC	3.388 V
				3D	1.860 V	7D	2.372 V	BD	2.884 V	FD	3.396 V
				3E	1.868 V	7E	2.380 V	BE	2.892 V	FE	3.404 V
				3F	1.876 V	7F	2.388 V	BF	2.900 V	FF	3.412 V

Table 15. REGISTER DETAILS – 0x09 LDO6

0x09 LDO6				Default = 00000000							
Bit	**Name**	**Default**	**Type**	**Description**							
7:0	LDO6_VOUT	00000000	R/W	Sets LDO6 regulation target voltage. Equation: Vout = 1.500 V + [(d – 16) x 8 mV], where d is the decimal value of the register							
				Hex	**VOUT**	**Hex**	**VOUT**	**Hex**	**VOUT**	**Hex**	**VOUT**
				00	**DEFAULT**	40	1.884 V	80	2.396 V	C0	2.908 V
				01	Reserved	41	1.892 V	81	2.404 V	C1	2.916 V
				02	Reserved	42	1.900 V	82	2.412 V	C2	2.924 V
				03	Reserved	43	1.908 V	83	2.420 V	C3	2.932 V
				04	Reserved	44	1.916 V	84	2.428 V	C4	2.940 V
				05	Reserved	45	1.924 V	85	2.436 V	C5	2.948 V
				06	Reserved	46	1.932 V	86	2.444 V	C6	2.956 V
				07	Reserved	47	1.940 V	87	2.452 V	C7	2.964 V
				08	Reserved	48	1.948 V	88	2.460 V	C8	2.972 V
				09	Reserved	49	1.956 V	89	2.468 V	C9	2.980 V
				0A	Reserved	4A	1.964 V	8A	2.476 V	CA	2.988 V
				0B	Reserved	4B	1.972 V	8B	2.484 V	CB	2.996 V
				0C	Reserved	4C	1.980 V	8C	2.492 V	CC	3.004 V
				0D	Reserved	4D	1.988 V	8D	2.500 V	CD	3.012 V
				0E	Reserved	4E	1.996 V	8E	2.508 V	CE	3.020 V
				0F	Reserved	4F	2.004 V	8F	2.516 V	CF	3.028 V
				10	1.500 V	50	2.012 V	90	2.524 V	D0	3.036 V
				11	1.508 V	51	2.020 V	91	2.532 V	D1	3.044 V
				12	1.516 V	52	2.028 V	92	2.540 V	D2	3.052 V
				13	1.524 V	53	2.036 V	93	2.548 V	D3	3.060 V
				14	1.532 V	54	2.044 V	94	2.556 V	D4	3.068 V
				15	1.540 V	55	2.052 V	95	2.564 V	D5	3.076 V
				16	1.548 V	56	2.060 V	96	2.572 V	D6	3.084 V
				17	1.556 V	57	2.068 V	97	2.580 V	D7	3.092 V
				18	1.564 V	58	2.076 V	98	2.588 V	D8	3.100 V
				19	1.572 V	59	2.084 V	99	2.596 V	D9	3.108 V
				1A	1.580 V	5A	2.092 V	9A	2.604 V	DA	3.116 V
				1B	1.588 V	5B	2.100 V	9B	2.612 V	DB	3.124 V
				1C	1.596 V	5C	2.108 V	9C	2.620 V	DC	3.132 V
				1D	1.604 V	5D	2.116 V	9D	2.628 V	DD	3.140 V
				1E	1.612 V	5E	2.124 V	9E	2.636 V	DE	3.148 V
				1F	1.620 V	5F	2.132 V	9F	2.644 V	DF	3.156 V
				20	1.628 V	60	2.140 V	A0	2.652 V	E0	3.164 V
				21	1.636 V	61	2.148 V	A1	2.660 V	E1	3.172 V
				22	1.644 V	62	2.156 V	A2	2.668 V	E2	3.180 V
				23	1.652 V	63	2.164 V	A3	2.676 V	E3	3.188 V
				24	1.660 V	64	2.172 V	A4	2.684 V	E4	3.196 V

Table 15. REGISTER DETAILS – 0x09 LDO6 (continued)

0x09 LDO6				Default = 00000000							
Bit	Name	Default	Type	Description							
				Hex	VOUT	Hex	VOUT	Hex	VOUT	Hex	VOUT
				25	1.668 V	65	2.180 V	A5	2.692 V	E5	3.204 V
				26	1.676 V	66	2.188V	A6	2.700 V	E6	3.212 V
				27	1.684 V	67	2.196 V	A7	2.708 V	E7	3.220 V
				28	1.692 V	68	2.204 V	A8	2.716 V	E8	3.228 V
				29	1.700 V	69	2.212 V	A9	2.724 V	E9	3.236 V
				2A	1.708 V	6A	2.220 V	AA	2.732 V	EA	3.244 V
				2B	1.716 V	6B	2.228 V	AB	2.740 V	EB	3.252 V
				2C	1.724 V	6C	2.236 V	AC	2.748 V	EC	3.260 V
				2D	1.732 V	6D	2.244 V	AD	2.756 V	ED	3.268 V
				2E	1.740 V	6E	2.252 V	AE	2.764 V	EE	3.276 V
				2F	1.748 V	6F	2.260 V	AF	2.772 V	EF	3.284 V
				30	1.756 V	70	2.268 V	B0	2.780 V	F0	3.292 V
				31	1.764 V	71	2.276 V	B1	2.788 V	F1	3.300 V
				32	1.772 V	72	2.284 V	B2	2.796 V	F2	3.308 V
				33	1.780 V	73	2.292 V	B3	2.804 V	F3	3.316 V
				34	1.788 V	74	2.300 V	B4	2.812 V	F4	3.324 V
				35	1.796 V	75	2.308 V	B5	2.820 V	F5	3.332 V
				36	1.804 V	76	2.316 V	B6	2.828 V	F6	3.340 V
				37	1.812 V	77	2.324 V	B7	2.836 V	F7	3.348 V
				38	1.820 V	78	2.332 V	B8	2.844 V	F8	3.356 V
				39	1.828 V	79	2.340 V	B9	2.852 V	F9	3.364 V
				3A	1.836 V	7A	2.348 V	BA	2.860 V	FA	3.372 V
				3B	1.844 V	7B	2.356 V	BB	2.868 V	FB	3.380 V
				3C	1.852 V	7C	2.364 V	BC	2.876 V	FC	3.388 V
				3D	1.860 V	7D	2.372 V	BD	2.884 V	FD	3.396 V
				3E	1.868 V	7E	2.380 V	BE	2.892 V	FE	3.404 V
				3F	1.876 V	7F	2.388 V	BF	2.900 V	FF	3.412 V

Table 16. REGISTER DETAILS – 0x0A LDO7

0x0A LDO7				Default = 00000000							
Bit	**Name**	**Default**	**Type**	**Description**							
7:0	LDO7_VOUT	00000000	R/W	Sets LDO7 regulation target voltage. Equation: Vout = 1.500 V + [(d – 16) x 8 mV];, where d is the decimal value of the register							
				Hex	**VOUT**	**Hex**	**VOUT**	**Hex**	**VOUT**	**Hex**	**VOUT**
				00	**DEFAULT**	40	1.884 V	80	2.396 V	C0	2.908 V
				01	Reserved	41	1.892 V	81	2.404 V	C1	2.916 V
				02	Reserved	42	1.900 V	82	2.412 V	C2	2.924 V
				03	Reserved	43	1.908 V	83	2.420 V	C3	2.932 V
				04	Reserved	44	1.916 V	84	2.428 V	C4	2.940 V
				05	Reserved	45	1.924 V	85	2.436 V	C5	2.948 V
				06	Reserved	46	1.932 V	86	2.444 V	C6	2.956 V
				07	Reserved	47	1.940 V	87	2.452 V	C7	2.964 V
				08	Reserved	48	1.948 V	88	2.460 V	C8	2.972 V
				09	Reserved	49	1.956 V	89	2.468 V	C9	2.980 V
				0A	Reserved	4A	1.964 V	8A	2.476 V	CA	2.988 V
				0B	Reserved	4B	1.972 V	8B	2.484 V	CB	2.996 V
				0C	Reserved	4C	1.980 V	8C	2.492 V	CC	3.004 V
				0D	Reserved	4D	1.988 V	8D	2.500 V	CD	3.012 V
				0E	Reserved	4E	1.996 V	8E	2.508 V	CE	3.020 V
				0F	Reserved	4F	2.004 V	8F	2.516 V	CF	3.028 V
				10	1.500 V	50	2.012 V	90	2.524 V	D0	3.036 V
				11	1.508 V	51	2.020 V	91	2.532 V	D1	3.044 V
				12	1.516 V	52	2.028 V	92	2.540 V	D2	3.052 V
				13	1.524 V	53	2.036 V	93	2.548 V	D3	3.060 V
				14	1.532 V	54	2.044 V	94	2.556 V	D4	3.068 V
				15	1.540 V	55	2.052 V	95	2.564 V	D5	3.076 V
				16	1.548 V	56	2.060 V	96	2.572 V	D6	3.084 V
				17	1.556 V	57	2.068 V	97	2.580 V	D7	3.092 V
				18	1.564 V	58	2.076 V	98	2.588 V	D8	3.100 V
				19	1.572 V	59	2.084 V	99	2.596 V	D9	3.108 V
				1A	1.580 V	5A	2.092 V	9A	2.604 V	DA	3.116 V
				1B	1.588 V	5B	2.100 V	9B	2.612 V	DB	3.124 V
				1C	1.596 V	5C	2.108 V	9C	2.620 V	DC	3.132 V
				1D	1.604 V	5D	2.116 V	9D	2.628 V	DD	3.140 V
				1E	1.612 V	5E	2.124 V	9E	2.636 V	DE	3.148 V
				1F	1.620 V	5F	2.132 V	9F	2.644 V	DF	3.156 V
				20	1.628 V	60	2.140 V	A0	2.652 V	E0	3.164 V
				21	1.636 V	61	2.148 V	A1	2.660 V	E1	3.172 V
				22	1.644 V	62	2.156 V	A2	2.668 V	E2	3.180 V
				23	1.652 V	63	2.164 V	A3	2.676 V	E3	3.188 V
				24	1.660 V	64	2.172 V	A4	2.684 V	E4	3.196 V

Table 16. REGISTER DETAILS – 0x0A LDO7 (continued)

0x0A LDO7				Default = 00000000							
Bit	Name	Default	Type	Description							
				Hex	VOUT	Hex	VOUT	Hex	VOUT	Hex	VOUT
				25	1.668 V	65	2.180 V	A5	2.692 V	E5	3.204 V
				26	1.676 V	66	2.188 V	A6	2.700 V	E6	3.212 V
				27	1.684 V	67	2.196 V	A7	2.708 V	E7	3.220 V
				28	1.692 V	68	2.204 V	A8	2.716 V	E8	3.228 V
				29	1.700 V	69	2.212 V	A9	2.724 V	E9	3.236 V
				2A	1.708 V	6A	2.220 V	AA	2.732 V	EA	3.244 V
				2B	1.716 V	6B	2.228 V	AB	2.740 V	EB	3.252 V
				2C	1.724 V	6C	2.236 V	AC	2.748 V	EC	3.260 V
				2D	1.732 V	6D	2.244 V	AD	2.756 V	ED	3.268 V
				2E	1.740 V	6E	2.252 V	AE	2.764 V	EE	3.276 V
				2F	1.748 V	6F	2.260 V	AF	2.772 V	EF	3.284 V
				30	1.756 V	70	2.268 V	B0	2.780 V	F0	3.292 V
				31	1.764 V	71	2.276 V	B1	2.788 V	F1	3.300 V
				32	1.772 V	72	2.284 V	B2	2.796 V	F2	3.308 V
				33	1.780 V	73	2.292 V	B3	2.804 V	F3	3.316 V
				34	1.788 V	74	2.300 V	B4	2.812 V	F4	3.324 V
				35	1.796 V	75	2.308 V	B5	2.820 V	F5	3.332 V
				36	1.804V	76	2.316 V	B6	2.828 V	F6	3.340 V
				37	1.812 V	77	2.324 V	B7	2.836 V	F7	3.348 V
				38	1.820 V	78	2.332 V	B8	2.844 V	F8	3.356 V
				39	1.828 V	79	2.340 V	B9	2.852 V	F9	3.364 V
				3A	1.836 V	7A	2.348 V	BA	2.860 V	FA	3.372 V
				3B	1.844 V	7B	2.356 V	BB	2.868 V	FB	3.380 V
				3C	1.852 V	7C	2.364 V	BC	2.876 V	FC	3.388 V
				3D	1.860 V	7D	2.372 V	BD	2.884 V	FD	3.396 V
				3E	1.868 V	7E	2.380 V	BE	2.892 V	FE	3.404 V
				3F	1.876 V	7F	2.388 V	BF	2.900 V	FF	3.412 V

Table 17. REGISTER DETAILS – 0x0B LDO12_SEQ

0x0B LDO12_SEQ				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7:6	UNUSED				
5:3	LDO2_SEQ	000	R/W	The LDO2 sequencing is selected by setting bits [5:3].	
				Code	**Slot Selected**
				000	Controlled through I^2C by setting the LDO2_EN bit
				001	Selects slot 1 for the LDO2 to be enabled in at power up
				010	Selects slot 2 for the LDO2 to be enabled in at power up
				011	Selects slot 3 for the LDO2 to be enabled in at power up
				100	Selects slot 4 for the LDO2 to be enabled in at power up
				101	Selects slot 5 for the LDO2 to be enabled in at power up
				110	Selects slot 6 for the LDO2 to be enabled in at power up
				111	Selects slot 7 for the LDO2 to be enabled in at power up
2:0	LDO1_SEQ	000	R/W	The LDO1 sequencing is selected by setting bits [2:0].	
				Code	**Slot Selected**
				000	Controlled through I^2C by setting the LDO1_EN bit
				001	Selects slot 1 for the LDO1 to be enabled in at power up
				010	Selects slot 2 for the LDO1 to be enabled in at power up
				011	Selects slot 3 for the LDO1 to be enabled in at power up
				100	Selects slot 4 for the LDO1 to be enabled in at power up
				101	Selects slot 5 for the LDO1 to be enabled in at power up
				110	Selects slot 6 for the LDO1 to be enabled in at power up
				111	Selects slot 7 for the LDO1 to be enabled in at power up

Table 18. REGISTER DETAILS – 0x0C LDO34_SEQ

0x0x0C LDO34_SEQ				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7:6	UNUSED				
5:3	LDO4_SEQ	000	R/W	The LDO4 sequencing is selected by setting bits [5:3].	
				Code	**Slot Selected**
				000	Controlled through I^2C by setting the LDO4_EN bit.
				001	Selects slot 1 for the LDO4 to be enabled in at power up.
				010	Selects slot 2 for the LDO4 to be enabled in at power up.
				011	Selects slot 3 for the LDO4 to be enabled in at power up.
				100	Selects slot 4 for the LDO4to be enabled in at power up.
				101	Selects slot 5 for the LDO4 to be enabled in at power up.
				110	Selects slot 6 for the LDO4 to be enabled in at power up.
				111	Selects slot 7 for the LDO4 to be enabled in at power up.
2:0	LDO3_SEQ	000	R/W	The LDO3 sequencing is selected by setting bits [2:0].	
				Code	**Slot Selected**
				000	Controlled through I^2C by setting the LDO3_EN bit.
				001	Selects slot 1 for the LDO3 to be enabled in at power up.
				010	Selects slot 2 for the LDO3 to be enabled in at power up.
				011	Selects slot 3 for the LDO3 to be enabled in at power up.
				100	Selects slot 4 for the LDO3 to be enabled in at power up.
				101	Selects slot 5 for the LDO3 to be enabled in at power up.
				110	Selects slot 6 for the LDO3 to be enabled in at power up.
				111	Selects slot 7 for the LDO3 to be enabled in at power up.

Table 19. REGISTER DETAILS – 0x0D LDO56_SEQ

0x0D LDO56_SEQ				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7:6	UNUSED				
5:3	LDO6_SEQ	000	R/W	The LDO6 sequencing is selected by setting bits [5:3].	
				Code	**Slot Selected**
				000	Controlled through I^2C by setting the LDO6_EN bit.
				001	Selects slot 1 for the LDO6 to be enabled in at power up.
				010	Selects slot 2 for the LDO6 to be enabled in at power up.
				011	Selects slot 3 for the LDO6 to be enabled in at power up.
				100	Selects slot 4 for the LDO6 to be enabled in at power up.
				101	Selects slot 5 for the LDO6 to be enabled in at power up.
				110	Selects slot 6 for the LDO6 to be enabled in at power up.
				111	Selects slot 7 for the LDO6 to be enabled in at power up.
2:0	LDO5_SEQ	000	R/W	The LDO5 sequencing is selected by setting bits [2:0].	
				Code	**Slot Selected**
				Code	Slot Selected
				000	Controlled through I^2C by setting the LDO5_EN bit.
				001	Selects slot 1 for the LDO5 to be enabled in at power up.
				010	Selects slot 2 for the LDO5 to be enabled in at power up.
				011	Selects slot 3 for the LDO5 to be enabled in at power up.
				100	Selects slot 4 for the LDO5 to be enabled in at power up.
				101	Selects slot 5 for the LDO5 to be enabled in at power up.
				110	Selects slot 6 for the LDO5 to be enabled in at power up.
				111	Selects slot 7 for the LDO5 to be enabled in at power up.

Table 20. REGISTER DETAILS – 0x0E LDO7_SEQ

0x0E LDO7_SEQ				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7:3	UNUSED				
2:0	LDO7_SEQ	000	R/W	The LDO7 sequencing is selected by setting bits [2:0].	
				Code	**Slot Selected**
				000	Controlled through I^2C by setting the LDO7_EN bit.
				001	Selects slot 1 for the LDO7 to be enabled in at power up.
				010	Selects slot 2 for the LDO7 to be enabled in at power up.
				011	Selects slot 3 for the LDO7 to be enabled in at power up.
				100	Selects slot 4 for the LDO7 to be enabled in at power up.
				101	Selects slot 5 for the LDO7 to be enabled in at power up.
				110	Selects slot 6 for the LDO7 to be enabled in at power up.
				111	Selects slot 7 for the LDO7 to be enabled in at power up.

Table 21. REGISTER DETAILS – 0x0F SEQUENCING

0x0F SEQUENCING				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7:6	SEQ_SPEED	00	R/W	**Code**	**Period per Slot**
				00	500 μs
				01	1.0 ms
				10	1.5 ms
				11	2.0 ms
5:4	SEQ_CONTROL	00	W/CLR	**Code**	**Initialize Power Up or Power Down**
				00	Default
				01	Starts an LDO power up sequence.
				10	Starts an LDO shutdown sequence.
				11	Bit configuration is ignored.
3	SEQ_ON	0	Read	**Code**	**State of Sequence**
				0	Indicates that the sequencing is not in process.
				1	Indicates that the sequencing is executing and somewhere between the start of slot 1 and the end of slot 7. The bit remains a 1 until slot 7 has completed at start−up or slot 1 has finished at shutdown, regardless of what slots are used.
2:0	SEQ_COUNT	000	Read	**Code**	**Present Slot**
				000	Indicates sequencing has completed or not started.
				001	Indicates was in slot 1 during register read.
				010	Indicates was in slot 2 during register read.
				011	Indicates was in slot 3 during register read.
				100	Indicates was in slot 4 during register read.
				101	Indicates was in slot 5 during register read.
				110	Indicates was in slot 6 during register read.
				111	Indicates was in slot 7 during register read.

Table 22. REGISTER DETAILS – 0x10 DISCHARGE

0x10 DISCHARGE				Default = 01111111	
Bit	**Name**	**Default**	**Type**	**Description**	
7	UNUSED				
6	LDO1_DIS	1	R/W	**Code**	**Discharge Enabled/Disabled**
				0	LDO1 Active Discharge feature is disabled. Pull−down will not be activated when LDO1 is disabled by any event.
				1	LDO1 Active Discharge feature is enabled. Pull−down will be activated when LDO1 is disabled by RESET_B going low or LDO1_EN = 0 or a sequenced shutdown or in an UVP event.
5	LDO2_DIS	1	R/W	**Code**	**Discharge Enabled/Disabled**
				0	LDO2 Active Discharge feature is disabled. Pull−down will not be activated when LDO2 is disabled by any event.
				1	LDO2 Active Discharge feature is enabled. Pull−down will be activated when LDO2 is disabled by RESET_B going low or LDO2_EN = 0 or a sequenced shutdown or in an UVP event.
4	LDO3_DIS	1	R/W	**Code**	**Discharge Enabled/Disabled**
				0	LDO3 Active Discharge feature is disabled. Pull−down will not be activated when LDO3 is disabled by any event.
				1	LDO3 Active Discharge feature is enabled. Pull−down will be activated when LDO3 is disabled by RESET_B going low or LDO3_EN = 0 or a sequenced shutdown or in an UVP event.
3	LDO4_DIS	1	R/W	**Code**	**Discharge Enabled/Disabled**
				0	LDO4 Active Discharge feature is disabled. Pull−down will not be activated when LDO4 is disabled by any event.
				1	LDO4 Active Discharge feature is enabled. Pull−down will be activated when LDO4 is disabled by RESET_B going low or LDO4_EN = 0 or a sequenced shutdown or in an UVP event.
2	LDO5_DIS	1	R/W	**Code**	**Discharge Enabled/Disabled**
				0	LDO5 Active Discharge feature is disabled. Pull−down will not be activated when LDO5 is disabled by any event.
				1	LDO5 Active Discharge feature is enabled. Pull−down will be activated when LDO5 is disabled by RESET_B going low or LDO5_EN = 0 or a sequenced shutdown or in an UVP event.
1	LDO6_DIS	1	R/W	**Code**	**Discharge Enabled/Disabled**
				0	LDO6 Active Discharge feature is disabled. Pull−down will not be activated when LDO6 is disabled by any event.
				1	LDO6 Active Discharge feature is enabled. Pull−down will be activated when LDO6 is disabled by RESET_B going low or LDO6_EN = 0 or a sequenced shutdown or in an UVP event.
0	LDO7_DIS	1	R/W	**Code**	**Discharge Enabled/Disabled**
				0	LDO7 Active Discharge feature is disabled. Pull−down will not be activated when LDO7 is disabled by any event.
				1	LDO7 Active Discharge feature is enabled. Pull−down will be activated when LDO7 is disabled by RESET_B going low or LDO7_EN = 0 or a sequenced shutdown or in an UVP event.

Table 23. REGISTER DETAILS – 0x11 RESET

0x11 RESET				Default = 00000110	
Bit	**Name**	**Default**	**Type**	**Description**	
7:4	SOFT_RESET	0000	Write	**Code**	**Software Reset**
				1011	Writing a ”1011” begins a soft reset of the device I2C registers to their default values. This bit is cleared upon the execution of the reset function.
					Any other value than “1011” will be ignored.
3	UNUSED				
2:1	OCP_TIMER	11	R/W	Option bits to control the length of the deglitch timer for current limit on all LDOs before a fault is triggered.	
				Code	**Deglitch Timer**
				00	125 μs
				01	250 μs
				10	500 μs
				11	1 ms
0	FLT_SD_B	0	R/W	**Code**	**Prevents Shutdown when a Fault Occurs**
				0	LDO shuts down if a UVP or OCP event occurs or if the LDO’s input VIN12, VIN34, VIN5, VIN6 or VIN7 have a UVLO event.
				1	LDO does not shut down if a UVP or OCP event occurs. If the LDO’s input VIN12, VIN34, VIN5, VIN6 or VIN7 have a UVLO event, the associated LDO will shut down until the supply returns, but the fault will not be counted.
				NOTE: If this bit function is desired, FLT_SD_B should be set to ”1” prior to enabling any LDOs after a Power−On−Reset.	

Table 24. REGISTER DETAILS – 0x12 I2C_ADDR

0x12 I2C_ADDR				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7:2	UNUSED				
1:0	I2C_ADDR_SEL	01	R/W	**Code**	**I^2C Address Settings**
				00	0x20
				01	0x35
				10	0x61
				11	0x72

Table 25. REGISTER DETAILS – 0x13 LDO_COMP0

0x13 LDO_COMP0				Default = 00000101		
Bit	**Name**	**Default**	**Type**	**Description**		
7:6	LDO4_COMP_SEL	00	R/W	The LDO4 Compensation is selected by modifying these bits to account for different COUT values. The Cout_min and Cout_max values are nominal 0DCV bias capacitance values utilized with the following DC de−rating:		
				Code	**Cout_min**	**Cout_max**
				00	1.0 μF	<4.7 μF
				01	4.7 μF	<15 μF
				10	15 μF	<47 μF
				11	NA	NA
5:4	LDO3_COMP_SEL	00	R/W	The LDO3 Compensation is selected by modifying these bits to account for different COUT value. The Cout_min and Cout_max values are nominal 0DCV bias capacitance values utilized with the following DC de−rating:		
				Code	**Cout_min**	**Cout_max**
				00	1.0 μF	<4.7 μF
				01	4.7 μF	<15 μF
				10	15 μF	<47 μF
				11	NA	NA
3:2	LDO2_COMP_SEL	01	R/W	The LDO2 Compensation is selected by modifying these bits to account for different COUT value.		
				Code	**COUT_MIN**	**COUT_MAX**
				00	–	<5.5 μF
				01	5.5 μF	<17 μF
				10	17 μF	<34 μF
				11	34 μF	–
1:0	LDO1_COMP_SEL	01	R/W	The LDO1 Compensation is selected by modifying these bits to account for different COUT value.		
				Code	**COUT_MIN**	**COUT_MAX**
				00	–	<5.5 μF
				01	5.5 μF	<17 μF
				10	17 μF	<34 μsF
				11	34 μF	–

Table 26. REGISTER DETAILS – 0x14 LDO_COMP1

<table>
<tr><th colspan="4">0x14 LDO_COMP1</th><th colspan="3">Default = 00000000</th></tr>
<tr><th>Bit</th><th>Name</th><th>Default</th><th>Type</th><th colspan="3">Description</th></tr>
<tr><td>7:6</td><td>UNUSED</td><td></td><td></td><td colspan="3"></td></tr>
<tr><td rowspan="6">5:4</td><td rowspan="6">LDO7_COMP_SEL</td><td rowspan="6">00</td><td rowspan="6">R/W</td><td colspan="3">The LDO7 Compensation is selected by modifying these bits to account for different COUT value.
The Cout_min and Cout_max values are nominal 0DCV bias capacitance values utilized with the following DC de−rating:</td></tr>
<tr><td>Code</td><td>Cout_min</td><td>Cout_max</td></tr>
<tr><td>00</td><td>1.0 μF</td><td><4.7 μF</td></tr>
<tr><td>01</td><td>4.7 μF</td><td><15 μF</td></tr>
<tr><td>10</td><td>15 μF</td><td><47 μF</td></tr>
<tr><td>11</td><td>NA</td><td>NA</td></tr>
<tr><td rowspan="6">3:2</td><td rowspan="6">LDO6_COMP_SEL</td><td rowspan="6">00</td><td rowspan="6">R/W</td><td colspan="3">The LDO6 Compensation is selected by modifying these bits to account for different COUT value.
The Cout_min and Cout_max values are nominal 0DCV bias capacitance values utilized with the following DC de−rating:</td></tr>
<tr><td>Code</td><td>Cout_min</td><td>Cout_max</td></tr>
<tr><td>00</td><td>1.0 μF</td><td><4.7 μF</td></tr>
<tr><td>01</td><td>4.7 μF</td><td><15 μF</td></tr>
<tr><td>10</td><td>15 μF</td><td><47 μF</td></tr>
<tr><td>11</td><td>NA</td><td>NA</td></tr>
<tr><td rowspan="6">1:0</td><td rowspan="6">LDO5_COMP_SEL</td><td rowspan="6">00</td><td rowspan="6">R/W</td><td colspan="3">The LDO5 Compensation is selected by modifying these bits to account for different COUT value.
The Cout_min and Cout_max values are nominal 0DCV bias capacitance values utilized with the following DC de−rating:</td></tr>
<tr><td>Code</td><td>Cout_min</td><td>Cout_max</td></tr>
<tr><td>00</td><td>1.0 μF</td><td><4.7 μF</td></tr>
<tr><td>01</td><td>4.7 μF</td><td><15 μF</td></tr>
<tr><td>10</td><td>15 μF</td><td><47 μF</td></tr>
<tr><td>11</td><td>NA</td><td>NA</td></tr>
</table>

Table 27. REGISTER DETAILS – 0x15 INTERRUPT1

0x15 INTERRUPT1				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7	UNUSED				
6	LDO7_UVP_INT	0	R/CLR	**Code**	**LDO7 UVP Interrupt**
				0	Clear
				1	Under−Voltage event occurred on LDO7 output.
5	LDO6_UVP_INT	0	R/CLR	**Code**	**LDO6 UVP Interrupt**
				0	Clear
				1	Under−Voltage event occurred on LDO6 output.
4	LDO5_UVP_INT	0	R/CLR	**Code**	**LDO5 UVP Interrupt**
				0	Clear
				1	Under−Voltage event occurred on LDO5 output.
3	LDO4_UVP_INT	0	R/CLR	**Code**	**LDO4 UVP Interrupt**
				0	Clear
				1	Under−Voltage event occurred on LDO4 output.
2	LDO3_UVP_INT	0	R/CLR	**Code**	**LDO3 UVP Interrupt**
				0	Clear
				1	Under−Voltage event occurred on LDO3 output.
1	LDO2_UVP_INT	0	R/CLR	**Code**	**LDO2 UVP Interrupt**
				0	Clear
				1	Under−Voltage event occurred on LDO2 output.
0	LDO1_UVP_INT	0	R/CLR	**Code**	**LDO1 UVP Interrupt**
				0	Clear
				1	Under−Voltage event occurred on LDO1 output.

Table 28. REGISTER DETAILS – 0x16 INTERRUPT2

0x16 INTERRUPT2				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7	UNUSED				
6	LDO7_OCP_INT	0	R/CLR	**Code**	**LDO7 OCP Interrupt**
				0	Clear
				1	Over−Current event detected on LDO7 output.
5	LDO6_OCP_INT	0	R/CLR	**Code**	**LDO6 OCP Interrupt**
				0	Clear
				1	Over−Current event detected on LDO6 output.
4	LDO5_OCP_INT	0	R/CLR	**Code**	**LDO5 OCP Interrupt**
				0	Clear
				1	Over−Current event detected on LDO5 output.
3	LDO4_OCP_INT	0	R/CLR	**Code**	**LDO4 OCP Interrupt**
				0	Clear
				1	Over−Current event detected on LDO4 output.
2	LDO3_OCP_INT	0	R/CLR	**Code**	**LDO3 OCP Interrupt**
				0	Clear
				1	Over−Current event detected on LDO3 output.
1	LDO2_OCP_INT	0	R/CLR	**Code**	**LDO2 OCP Interrupt**
				0	Clear
				1	Over−Current event detected on LDO2 output.
0	LDO1_OCP_INT	0	R/CLR	**Code**	**LDO1 OCP Interrupt**
				0	Clear
				1	Over−Current event detected on LDO1 output.

Table 29. REGISTER DETAILS – 0x17 INTERRUPT3

0x17 INTERRUPT3				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7	TSD_INT	0	R/CLR	**Code**	**Thermal Shutdown Interrupt**
				0	Clear
				1	A Thermal Shutdown event detected or that the temperature has fallen below the hysteresis level.
6	TSD_WRN_INT	0	R/CLR	**Code**	**Thermal Warning Interrupt**
				0	Clear
				1	Thermal Shutdown Warning threshold was surpassed or that the temperature has fallen below the hysteresis level.
5	VSYS_UVLO_INT	0	R/CLR	**Code**	**VSYS Under−Voltage−Lock−Out Interrupt**
				0	Clear
				1	VSYS fell below the UVLO falling threshold or that VSYS have risen above the UVLO rising threshold after a UVLO fault.
				Reading the the associated status bit provides present state of the input voltage.	
4	LDO7_UVLO_INT	0	R/CLR	**Code**	**VIN7 Under−Voltage−Lock−Out Interrupt**
				0	Clear
				1	VIN7 fell below the UVLO falling threshold while LDO7 was enabled or that VIN7 has risen above the UVLO rising threshold after a UVLO fault.
				Reading the associated status bit provides present state of the input voltage.	
3	LDO6_UVLO_INT	0	R/CLR	**Code**	**VIN6 Under−Voltage−Lock−Out Interrupt**
				0	Clear
				1	VIN6 fell below the UVLO falling threshold while LDO6 was enabled or that VIN6 has risen above the UVLO rising threshold after a UVLO fault.
				Reading the associated status bit provides present state of the input voltage.	
2	LDO5_UVLO_INT	0	R/CLR	**Code**	**VIN5 Under−Voltage−Lock−Out Interrupt**
				0	Clear
				1	VIN5 fell below the UVLO falling threshold while LDO5 was enabled or that VIN5 has risen above the UVLO rising threshold after a UVLO fault.
				Reading the associated status bit provides present state of the input voltage.	
1	LDO34_UVLO_INT	0	R/CLR	**Code**	**VIN34 Under−Voltage−Lock−Out Interrupt**
				0	Clear
				1	VIN34 fell below the UVLO falling threshold while LDO3 and/or LDO4 were enabled or that VIN34 has risen above the rising UVLO thresholds after a UVLO fault.
				Reading the associated status bit provides present state of the input voltage.	
0	LDO12_UVLO_INT	0	R/CLR	**Code**	**VIN12 Under−Voltage−Lock−Out Interrupt**
				0	Clear
				1	VIN12 fell below the UVLO falling threshold while LDO1 and/or LDO2 were enabled or that VIN12 has risen above the UVLO rising threshold after a UVLO fault.
				Reading the associated status bit provides present state of the input voltage.	

Table 30. REGISTER DETAILS – 0x18 STATUS1

0x18 STATUS1				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7	UNUSED				
6	LDO7_UVP_STAT	0	Read	**Code**	**LDO7 UVP Status**
				0	Normal Operation
				1	An Under−Voltage condition exists on LDO7 output.
5	LDO6_UVP_STAT	0	Read	**Code**	**LDO6 UVP Status**
				0	Normal Operation
				1	An Under−Voltage condition exists on LDO6 output.
4	LDO5_UVP_STAT	0	Read	**Code**	**LDO5 UVP Status**
				0	Normal Operation
				1	An Under−Voltage condition exists on LDO5 output.
3	LDO4_UVP_STAT	0	Read	**Code**	**LDO4 UVP Status**
				0	Normal Operation
				1	An Under−Voltage condition exists on LDO4 output.
2	LDO3_UVP_STAT	0	Read	**Code**	**LDO3 UVP Status**
				0	Normal Operation
				1	An Under−Voltage condition exists on LDO3 output.
1	LDO2_UVP_STAT	0	Read	**Code**	**LDO2 UVP Status**
				0	Normal Operation
				1	An Under−Voltage condition exists on LDO2 output.
0	LDO1_UVP_STAT	0	Read	**Code**	**LDO1 UVP Status**
				0	Normal Operation
				1	An Under−Voltage condition exists on LDO1 output.

Table 31. REGISTER DETAILS – 0x19 STATUS2

0x19 STATUS2				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7	UNUSED				
6	LDO7_OCP_STAT	0	Read	**Code**	**LDO7 OCP Status**
				0	Normal Operation
				1	An Over−Current condition exists on LDO7 output.
5	LDO6_OCP_STAT	0	Read	**Code**	**LDO6 OCP Status**
				0	Normal Operation
				1	An Over−Current condition exists on LDO6 output.
4	LDO5_OCP_STAT	0	Read	**Code**	**LDO5 OCP Status**
				0	Normal Operation
				1	An Over−Current condition exists on LDO5 output.
3	LDO4_OCP_STAT	0	Read	**Code**	**LDO4 OCP Status**
				0	Normal Operation
				1	An Over−Current condition exists on LDO4 output.
2	LDO3_OCP_STAT	0	Read	**Code**	**LDO3 OCP Status**
				0	Normal Operation
				1	An Over−Current condition exists on LDO3 output.
1	LDO2_OCP_STAT	0	Read	**Code**	**LDO2 OCP Status**
				0	Normal Operation
				1	An Over−Current condition exists on LDO2 output.
0	LDO1_OCP_STAT	0	Read	**Code**	**LDO1 OCP Status**
				0	Normal Operation
				1	An Over−Current condition exists on LDO1 output.

Table 32. REGISTER DETAILS – 0x1A STATUS3

0x1AB STATUS3				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7	TSD_STAT	0	Read	**Code**	**Thermal Shutdown Status**
				0	Normal Operation
				1	Device is in Thermal Shutdown.
6	TSD_WRN_STAT	0	Read	**Code**	**Thermal Warning Status**
				0	Normal Operation
				1	The temperature is above the Thermal Warning level and shutdown is impending.
5	VSYS_UVLO_STAT	0	Read	**Code**	**VSYS Under−Voltage−Lock−Out Status**
				0	Normal Operation
				1	VSYS is below the UVLO threshold.
4	LDO7_UVLO_STAT	0	Read	**Code**	**VIN7 Under−Voltage−Lock−Out Status**
				0	Normal Operation
				1	VIN7 is below the UVLO threshold while LDO7 is enabled.
3	LDO6_UVLO_STAT	0	Read	**Code**	**VIN6 Under−Voltage−Lock−Out Status**
				0	Normal Operation
				1	VIN6 is below the UVLO threshold while LDO6 is enabled.
2	LDO5_UVLO_STAT	0	Read	**Code**	**VIN5 Under−Voltage−Lock−Out Status**
				0	Normal Operation
				1	VIN5 is below the UVLO threshold while LDO5 is enabled.
1	LDO34_UVLO_STAT	0	Read	**Code**	**VIN34 Under−Voltage−Lock−Out Status**
				0	Normal Operation
				1	VIN34 is below the UVLO threshold while LDO3 and/or LDO4 are enabled.
0	LDO12_UVLO_STAT	0	Read	**Code**	**VIN12 Under−Voltage−Lock−Out Status**
				0	Normal Operation
				1	VIN12 is below the UVLO threshold while LDO1 and/or LDO2 are enabled.

Table 33. REGISTER DETAILS – 0x1B STATUS4

0x1B STATUS4				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
6	CHIP_SUSD	0	Read	**Code**	**Chip Suspension**
				0	Chip in normal state
				1	The entire chip has been suspended due to a global fault condition.
6	LDO7_SUSD	0	Read	**Code**	**LDO7 Output Suspended**
				0	LDO7 in normal state
				1	LDO7 has been suspended due to a fault condition.
5	LDO6_SUSD	0	Read	**Code**	**LDO6 Output Suspended**
				0	LDO6 in normal state
				1	LDO6 has been suspended due to a fault condition.
4	LDO5_SUSD	0	Read	**Code**	**LDO5 Output Suspended**
				0	LDO5 in normal state
				1	LDO5 has been suspended due to a fault condition.
3	LDO4_SUSD	0	Read	**Code**	**LDO4 Output Suspended**
				0	LDO4 in normal state
				1	LDO4 has been suspended due to a fault condition.
2	LDO3_SUSD	0	Read	**Code**	**LDO3 Output Suspended**
				0	LDO3 in normal state
				1	LDO3 has been suspended due to a fault condition.
1	LDO2_SUSD	0	Read	**Code**	**LDO2 Output Suspended**
				0	LDO2 in normal state
				1	LDO2 has been suspended due to a fault condition.
0	LDO1_SUSD	0	Read	**Code**	**LDO1 Output Suspended**
				0	LDO1 in normal state
				1	LDO1 has been suspended due to a fault condition.

Table 34. REGISTER DETAILS – 0x1C MINT1

0x1C MINT1				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7	UNUSED				
6	MASK_LDO7_UVP	0	R/W	**Code**	**LDO7 UVP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO7 Under−Voltage interrupt occurs.
5	MASK_LDO6_UVP	0	R/W	**Code**	**LDO6 UVP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO6 Under−Voltage interrupt occurs.
4	MASK_LDO5_UVP	0	R/W	**Code**	**LDO5 UVP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO5 Under−Voltage interrupt occurs.
3	MASK_LDO4_UVP	0	R/W	**Code**	**LDO4 UVP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO4 Under−Voltage interrupt occurs.
2	MASK_LDO3_UVP	0	R/W	**Code**	**LDO3 UVP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO3 Under−Voltage interrupt occurs.
1	MASK_LDO2_UVP	0	R/W	**Code**	**LDO2 UVP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO2 Under−Voltage interrupt occurs.
0	MASK_LDO1_UVP	0	R/W	**Code**	**LDO1 UVP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO1 Under−Voltage interrupt occurs.

Table 35. REGISTER DETAILS – 0x1D MINT2

0x1D MINT2				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7	UNUSED				
6	MASK_LDO7_OCP	0	R/W	**Code**	**LDO7 OCP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO7 Over−Current interrupt occurs
5	MASK_LDO6_OCP	0	R/W	**Code**	**LDO6 OCP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO6 Over−Current interrupt occurs
4	MASK_LDO5_OCP	0	R/W	**Code**	**LDO5 OCP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO5 Over−Current interrupt occurs
3	MASK_LDO4_OCP	0	R/W	**Code**	**LDO4 OCP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO4 Over−Current interrupt occurs
2	MASK_LDO3_OCP	0	R/W	**Code**	**LDO3 OCP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO3 Over−Current interrupt occurs
1	MASK_LDO2_OCP	0	R/W	**Code**	**LDO2 OCP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO2 Over−Current interrupt occurs
0	MASK_LDO1_OCP	0	R/W	**Code**	**LDO1 OCP MASK**
				0	No masking of interrupt
				1	INT pin will not change states when LDO1 Over−Current interrupt occurs

Table 36. REGISTER DETAILS – 0x1E MINT3

0x1E MINT3				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7	MASK_TSD	0	R/W	**Code**	**Thermal Shutdown MASK**
				0	No masking of interrupt
				1	INT pin will not change states when a Thermal Shutdown interrupt occurs.
6	MASK_TSD_WRN	0	R/W	**Code**	**Thermal Warning MASK**
				0	No masking of interrupt
				1	INT pin will not change states when a Thermal Warning interrupt occurs.
5	MASK_VSYS_UVLO	0	R/W	**Code**	**VSYS UVLO MASK**
				0	No masking of interrupt
				1	INT pin will not change states when VSYS Input Power Under−Voltage interrupt occurs.
4	MASK_LDO7_UVLO	0	R/W	**Code**	**LDO7 UVLO MASK**
				0	No masking of interrupt
				1	INT pin will not change states when VIN7 Input Power Under−Voltage interrupt occurs.
3	MASK_LDO6_UVLO	0	R/W	**Code**	**VIN6 UVLO MASK**
				0	No masking of interrupt
				1	INT pin will not change states when VIN6 Input Power Under−Voltage interrupt occurs.
2	MASK_LDO5_UVLO	0	R/W	**Code**	**VIN5 UVLO MASK**
				0	No masking of interrupt
				1	INT pin will not change states when VIN5 Input Power Under−Voltage interrupt occurs.
1	MASK_LDO34_UVLO	0	R/W	**Code**	**VIN34 UVLO MASK**
				0	No masking of interrupt
				1	INT pin will not change states when VIN34 Input Power Under−Voltage interrupt occurs.
0	MASK_LDO12_UVLO	0	R/W	**Code**	**VIN12 UVLO MASK**
				0	No masking of interrupt
				1	INT pin will not change states when VIN12 Input Power Under−Voltage interrupt occurs.

APPLICATION GUIDELINES

LDO Input Capacitor Considerations

If long wires are used to bring power to an evaluation board, additional “bulk” capacitance (electrolytic or tantalum) should be placed (on the evaluation board) between C_{IN} and the power source lead to reduce ringing that can occur between the inductance of the power source leads and C_{IN}. Use only X5R and X7R ceramic capacitors with adequate voltage rating for the input capacitors.

The effective capacitance value decreases as the voltage across the capacitor increases due to DC bias effects. Adding additional capacitance to the minimum recommended ensures reliable operation.

LDO Output Capacitor Considerations

FAN53870 LDOs are initially set at the factory for a range of 5.5 to 17 μF (unbiased) on LDO1 and LDO2, and a range of 1.0 to 4.7 μF (unbiased) on LDO3−7. All LDOs can be trimmed at the factory for up to 47 μF total (unbiased) capacitance. When evaluating and ordering the FAN53870, to ensure optimum performance and stability, specify the amount of capacitance each LDO output will have with an **onsemi** representative.

Use only X5R and X7R ceramic capacitors with adequate voltage rating for the output capacitors.

PCB Layout Recommendations

Input and output capacitors should be placed as close to the associated power pin. The ground terminal of the capacitor should be connected to a good ground plane – preferably on the surface of the board. Input power should be routed to the input capacitor first and then to the input pin of the IC. For power from layers other than the layer on which the capacitor sits, should be routed to the capacitor layer with vias in pad or close to the positive terminal of the capacitor. Power traces from the LDO output should be routed to the output capacitor first and then to (if necessary) other layers.

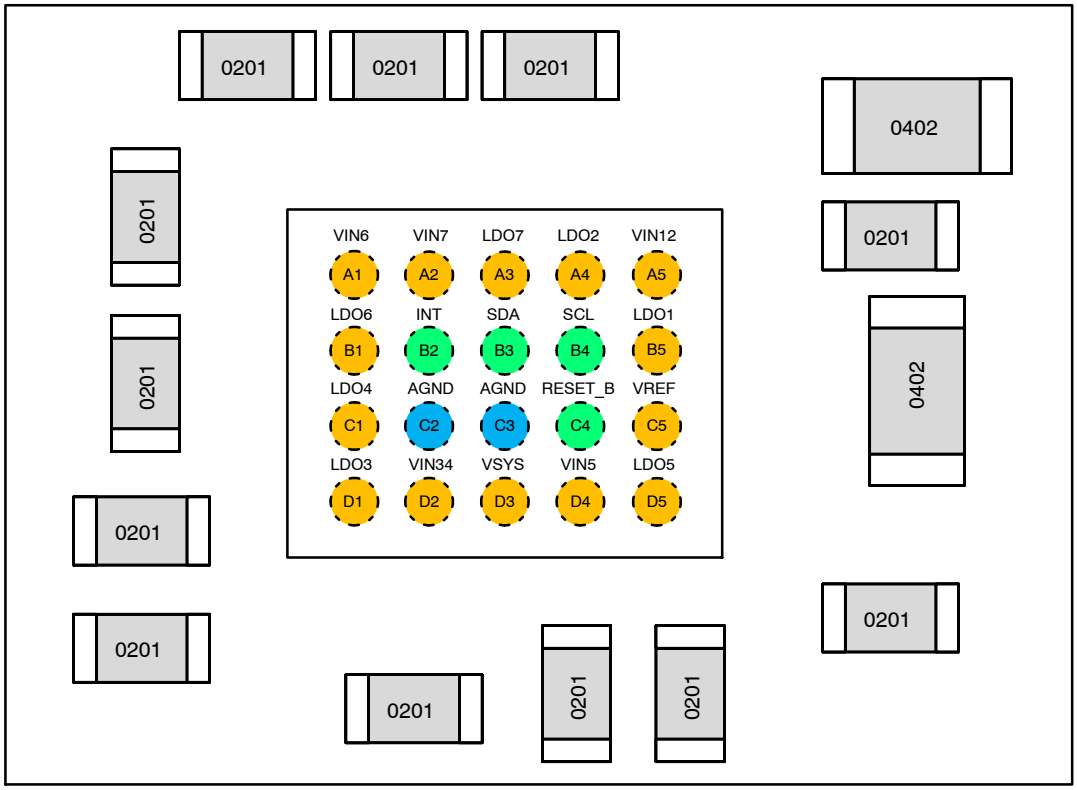


Figure 33. Recommended PCB Assembly (Top View)

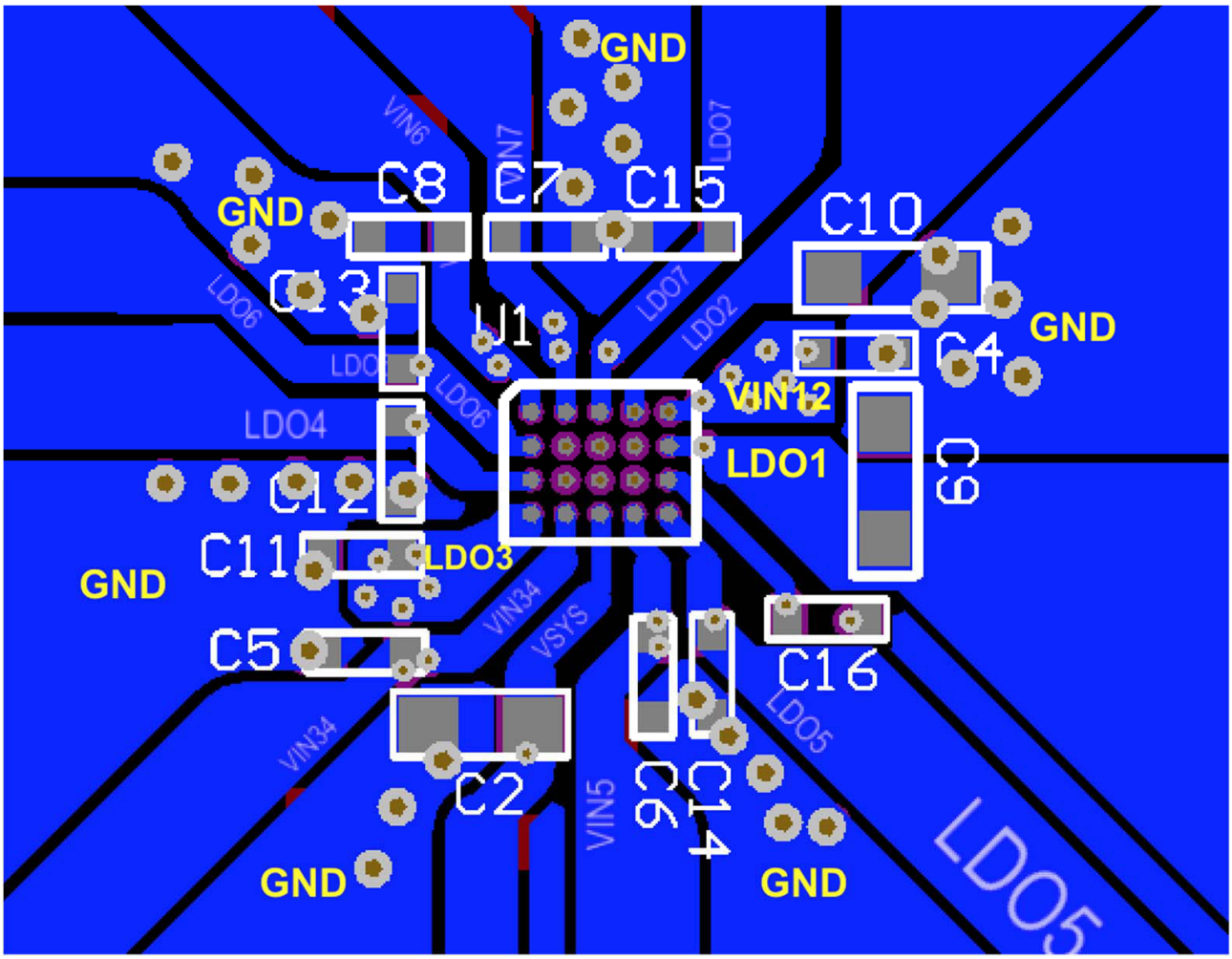
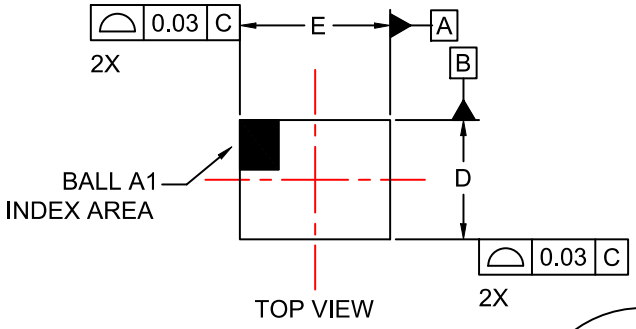
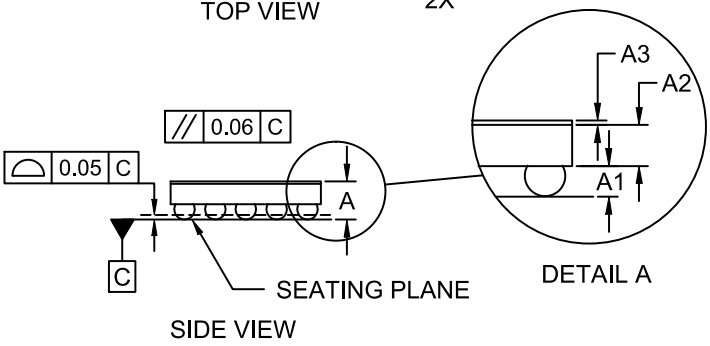


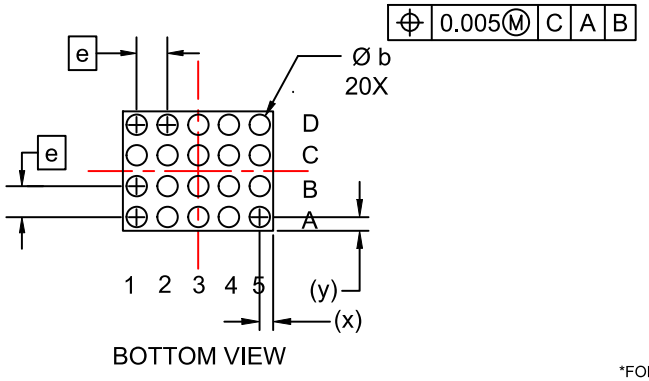
Figure 34. Recommended PCB Layout

WLCSP20 1.61x1.96x0.432
CASE 567YA
ISSUE O

DATE 02 JUL 2019



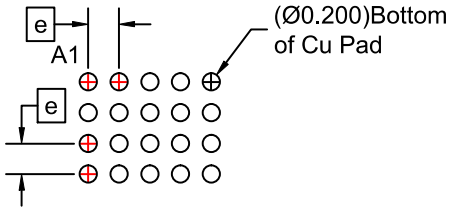




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.391	0.432	0.473
A1	0.154	0.174	0.194
A2	0.215	0.233	0.251
A3	0.022	0.025	0.028
b	0.211	0.231	0.251
D	1.58	1.61	1.64
E	1.93	1.96	1.99
e	0.35 BSC		
x	0.265	0.280	0.295
y	0.265	0.280	0.295



RECOMMENDED
MOUNTING FOOTPRINT*
(NSMD PAD TYPE)

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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DESCRIPTION:	**WLCSP20 1.61x1.96x0.432**	**PAGE 1 OF 1**

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