NCP6324GEVB

NCP6324B/C Evaluation Board User's Manual

3 MHz, 2 A, High Efficiency, Low Ripple, Adjustable Output Voltage, Synchronous Buck Converter

ON Semiconductor®

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EVAL BOARD USER'S MANUAL

Overview

This document is a manual file for a demo board of the NCP6324B/C, which includes demo board schematics, bill of materials, PCB layout, jumper setup, and test procedure.

About NCP6324B/C

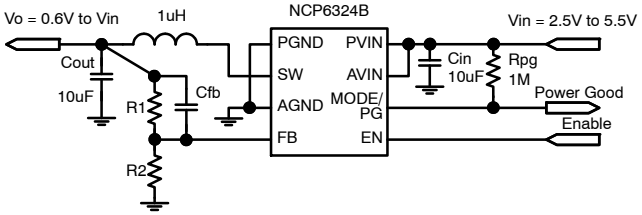
The NCP6324B/C, a family of synchronous buck converters, which is optimized to supply different sub systems of portable applications powered by one cell Li-ion or three cell Alkaline/NiCd/NiMH batteries. The devices are able to deliver up to 2 A on an external adjustable voltage range from 0.6 V to 3.3 V. Operation with 3 MHz switching frequency allows employing small size inductor and capacitors. Input supply voltage feed-forward control is employed to deal with wide input voltage range. Synchronous rectification and automatic PWM/PFM power save mode offer improved system efficiency. The NCP6324B is in a space saving, low profile $2.0 \times 2.0 \times 0.75$ mm WDFN−8 package.

Features

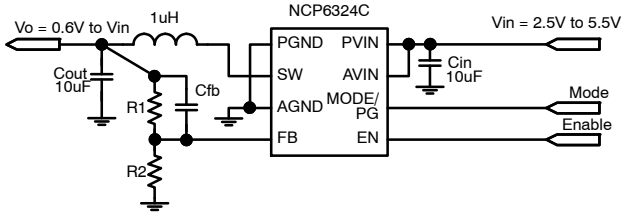
- 2.5 V to 5.5 V Input Voltage Range
- External Adjustable Voltage
- Up to 2 A Output Current
- 3 MHz Switching Frequency
- Synchronous Rectification
- Automatic Power Save or External Mode Selection
- Enable Input
- Power Good Output
- Soft Start
- Over Current Protection
- Active Discharge When Disabled. Hi−Z Version Available upon Request
- Thermal Shutdown Protection
- WDFN−8, 2×2 mm, 0.5 mm Pitch Package
- Maximum 0.8 mm Height for Super Thin Applications

Typical Applications

- Cellular Phones, Smart Phones, and PDAs
- Portable Media Players
- Digital Still Cameras
- Wireless and DSL Modems
- USB Powered Devices
- Point of Load
- Game and Entertainment System



(a) Power Good Output (NCP6324B)



(b) External Mode Selection
(NCP6324C Available upon Request)

Figure 1. Typical Application Circuits

Table 1. PIN DESCRIPTION

Pin	Name	Type	Description
1	PGND	Power Ground	Power Ground for power, analog blocks. Must be connected to the system ground.
2	SW	Power Output	Switch Power pin connects power transistors to one end of the inductor.
3	AGND	Analog Ground	Analog Ground analog and digital blocks. Must be connected to the system ground.
4	FB	Analog Input	Feedback Voltage from the buck converter output. This is the input to the error amplifier. For fixed output devices, this pin is directly connected to the output capacitor; For external adjustable output devices, this pin is connected to the resistor divider network between the output and AGND.
5	EN	Digital Input	Enable of the IC. High level at this pin enables the device. Low level at this pin disables the device.
6	PG	Digital Output	PG pin is for NCP6324B with Power Good option. It is open drain output. Low level at this pin indicates the device is not in power good, while high impedance at this pin indicates the device is in power good.
7	AVIN	Analog Input	Analog Supply. This pin is the analog and the digital supply of the device. An optional 1 μF or larger ceramic capacitor bypasses this input to the ground. This capacitor should be placed as close as possible to this input.
8	PVIN	Power Input	Power Supply Input. This pin is the power supply of the device. A 10 μF or larger ceramic capacitor must bypass this input to the ground. This capacitor should be placed as close a possible to this input.
9	PAD	Exposed Pad	Exposed Pad. Must be soldered to system ground to achieve power dissipation performances. This pin is internally unconnected

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value		Unit
		Min	Max	
Input Supply Voltage to GND	V_{PVIN}, V_{AVIN}	−0.3	7.0	V
Switch Node to GND	V_{SW}	−0.3	7.0	V
EN, PG to GND	V_{EN}, V_{PG}	−0.3	7.0	V
FB to GND	V_{FB}	−0.3	7.0	V
Human Body Model (HBM) ESD Rating are (Note 1)	ESD HBM	−	2,000	V
Machine Model (MM) ESD Rating are (Note 1)	ESD MM	−	200	V
Latch up Current: (Note 2) All pins, except digital pins Digital pins	I_{LU}	 −100 −10	 100 10	mA
Operating Junction Temperature Range	T_J	−40	125	°C
Operating Ambient Temperature Range	T_A	−40	85	°C
Storage Temperature Range	T_{STG}	−55	150	°C
Thermal Resistance Junction-to-Top Case (Note 4)	$R_{\theta JC}$	12		°C/W
Thermal Resistance Junction-to-Board (Note 4)	$R_{\theta JB}$	30		°C/W
Thermal Resistance Junction-to-Ambient (Note 4)	$R_{\theta JA}$	62		°C/W
Power Dissipation (Note 5)	P_D	1.6		W
Moisture Sensitivity Level (Note 6)	MSL	1		−

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114.
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115.
2. Latch up Current per JEDEC standard: JESD78 class II.
3. The thermal shutdown set to 150°C (typical) avoids potential irreversible damage on the device due to power dissipation.
4. The thermal resistance values are dependent of the PCB heat dissipation. Board used to drive these data was an 80 x 50 mm NCP6324EVB board. It is a multilayer board with 1 once internal power and ground planes and 2−once copper traces on top and bottom of the board. If the copper trances of top and bottom are 1 once too, $R_{\theta JC}$ = 11°C/W, $R_{\theta JB}$ = 30°C/W, and $R_{\theta JA}$ = 72°C/W.
5. .The maximum power dissipation (PD) is dependent on input voltage, maximum output current and external components selected.
6. .Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

Electrical Characteristics

For electrical characteristics, please refer to NCP6324B/C datasheet available on website: http://www.onsemi.com.

Schematic of Demo Board

A schematic of NCP6324B/C evaluation board is shown in Figure 2, which is for a typical application with 1.8 V output voltage. It is flexible to configure the board for both PG devices (NCP6324B) and Mode devices (NCP6324C). Please refer to Jumper Configuration for details.

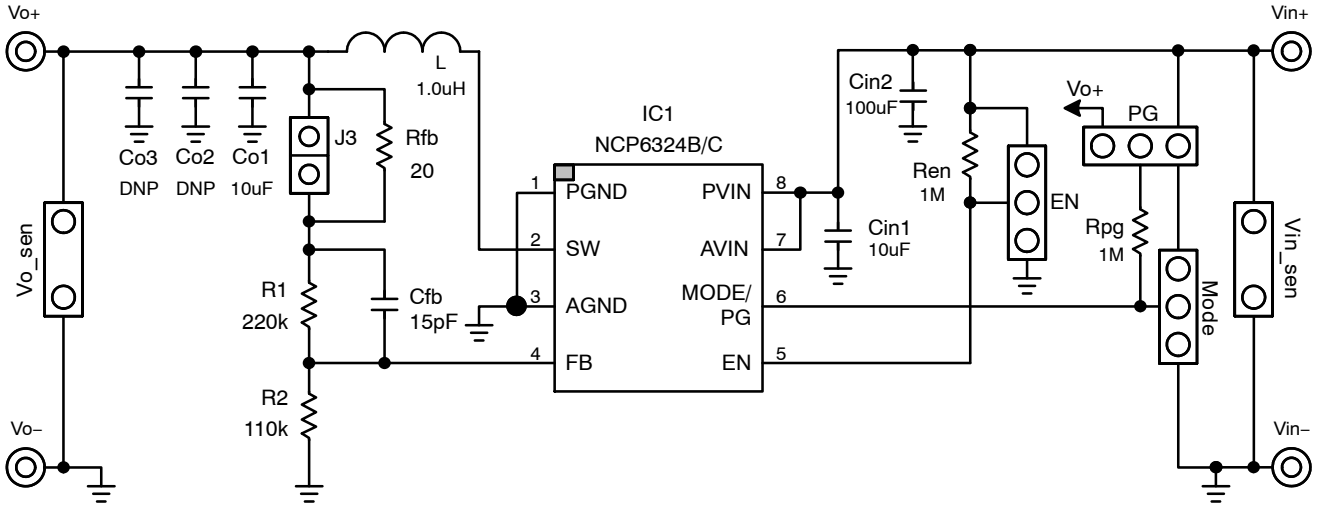


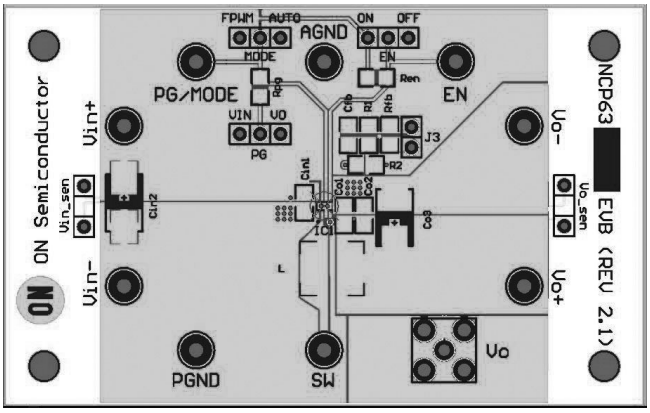
Figure 2. Schematic of NCP6324B/C Evaluation Board

Table 3. BILL OF MATERIALS OF EVALUATION BOARD

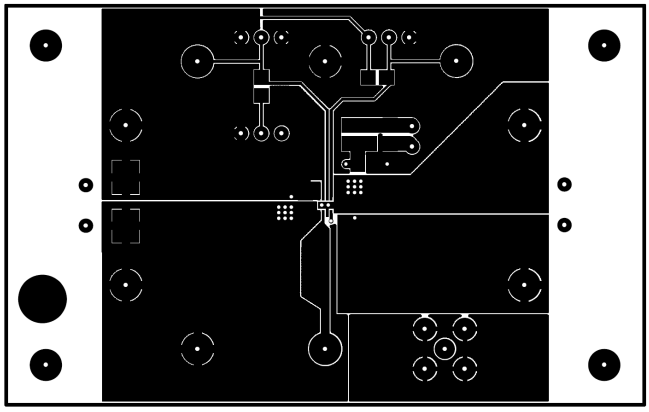
Item	Part Reference	Description	Package	Part Number	Manufacturer	Qty
1	IC1	3 MHz, 2 A, Synchronous Buck Converter	WDFN−8 2.0 × 2.0 × 0.75 mm	NCP63xyB/C	ON Semiconductor	1
2	Cin1	MLCC Cap 10 V, 10 μF, X5R, ±20%	0805	GRM21BR61A106KE19	muRata	1
3	Cin2	MLCC Cap 6.3 V, 100 μF, X5R, ±20%	1210	GRM32ER60J107ME20	muRata	1
4	Co1	MLCC Cap 6.3 V, 10 μF, X5R, ±20%	0603	GRM188R60J106ME47	muRata	1
5	L	Power Choke 1.0 μH, ±30%, 2450 mA, 30 mΩ	4.0 × 3.5 × 1.65 mm	LQH44PN1R0NP0	muRata	1
6	Ren, Rpg	Thick Film Chip Resistors, 1 MΩ, ±5%, 0.1 W	0603	ERJ3GEYJ105V	Panasonic	2
7	R1	Thick Film Chip Resistors, 220 kΩ, ±1%, 0.1 W	0603	ERA3AEB224V	Panasonic	1
8	R2	Thick Film Chip Resistors, 110 kΩ, ±1%, 0.1 W	0603	ERA3AEB114V	Panasonic	1
9	Cfb	MLCC, 15 pF, 50 V, 0603	0603	ECJ1VC1H150J	Panasonic	1
10	Rfb	Thick Film Chip Resistors, 20 Ω, ±1%, 0.1 W	0603	ERA3AEB200V	Panasonic	1

PCB Layout of Demo Board

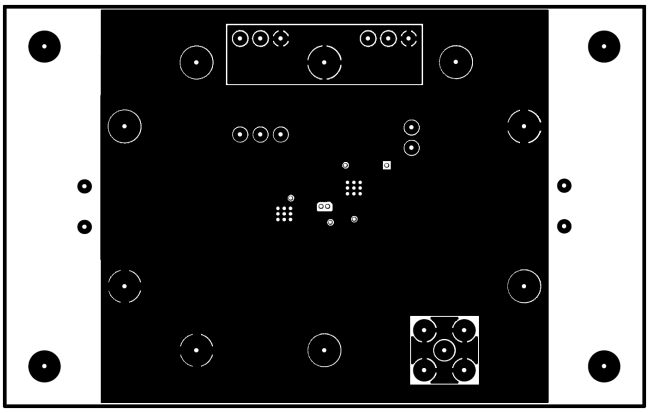
A 80×50 mm PCB is designed for NCP6324B/C evaluation board. It is a 4-layer board with 1-once internal ground planes (middle1 layer and middle2 layer) and 2-once copper traces on top layer and bottom layer of the board. Figure 3 shows layout information of the board.



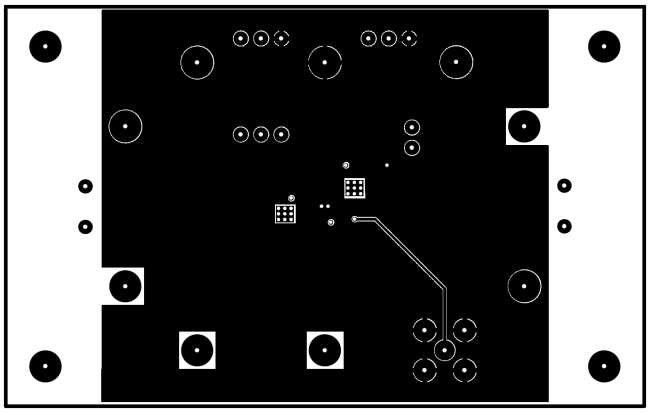
(a) TopOver Layer



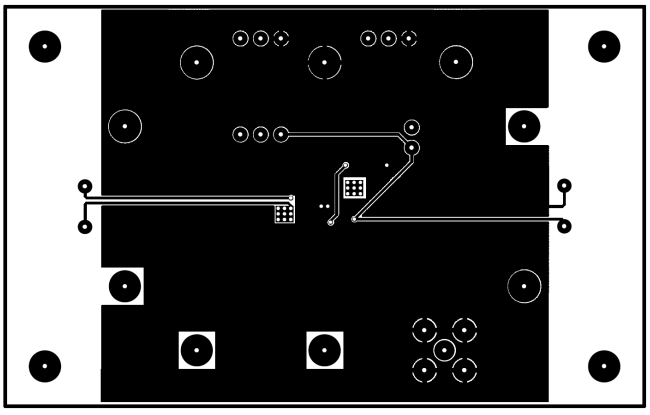
(b) Top Layer



(c) Middle 1 Layer



(d) Middle 2 Layer

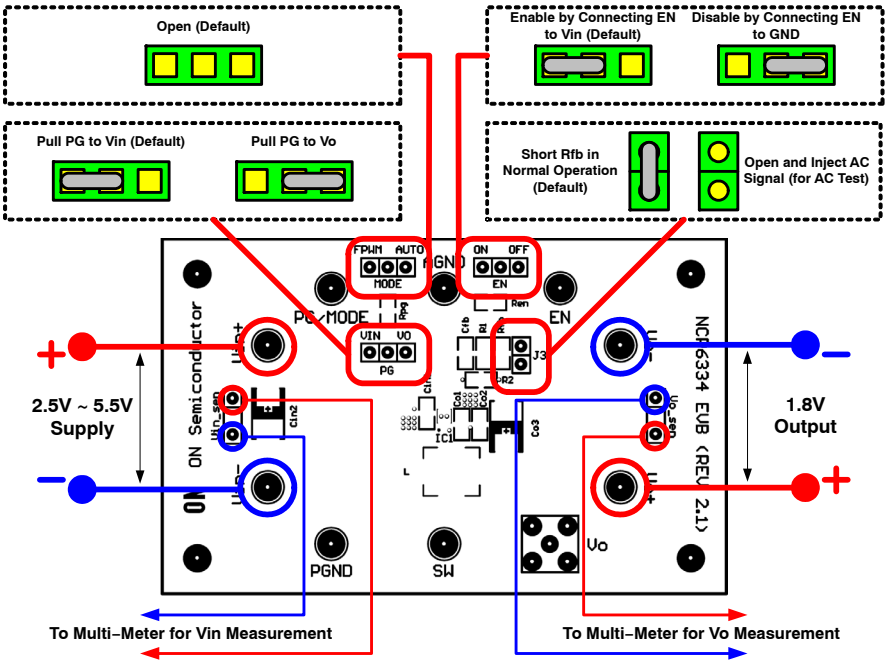


(e) Bottom Layer

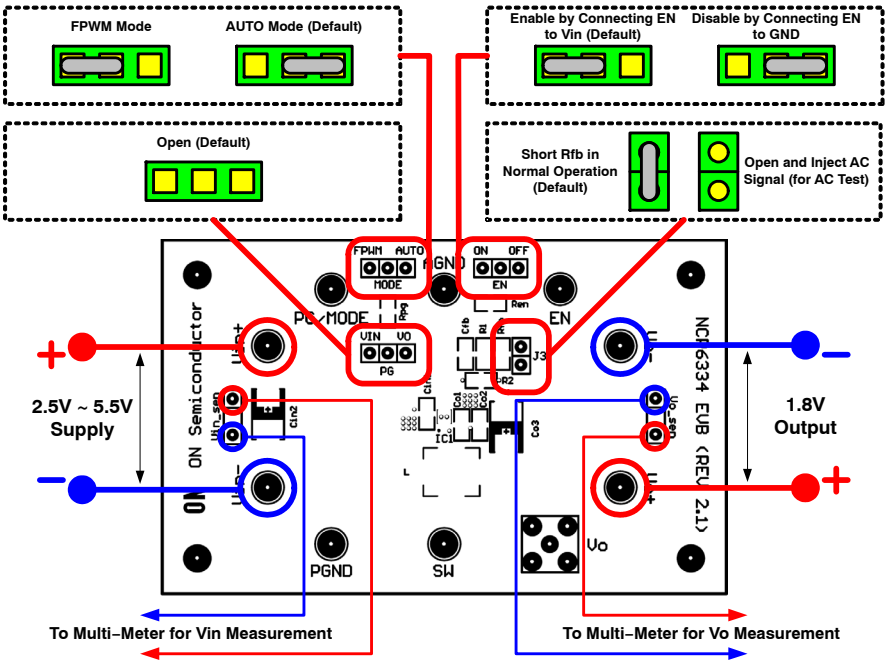
Figure 3. PCB Layout of NCP6324B/C Evaluation Board

Connections and Jumper Setup

There are two main configurations of the demo board for two different devices, which are NCP6324B (PG device) and NCP6324C (Mode device). External connections and jumper setup for both configurations are shown in Figure 4. The default configuration of NCP6324B/C evaluation board is for NCP6324B devices.



(a) NCP6324B (Default)

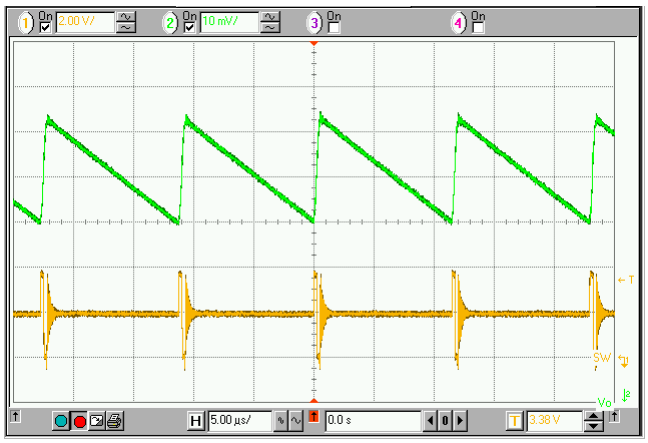


(b) NCP6324C

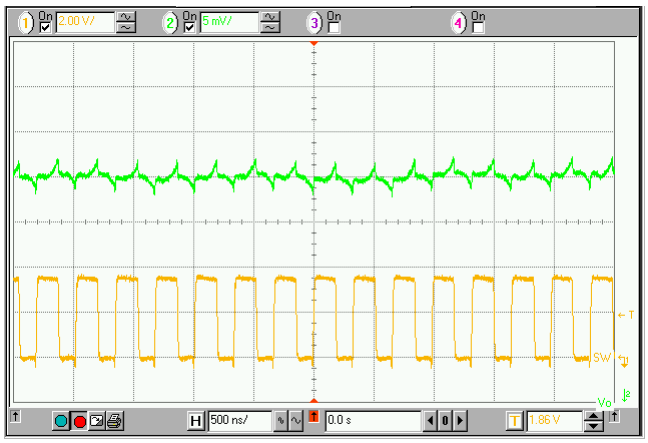
Figure 4. Connections and Jumper Setup of NCP6324B/C Evaluation Board

Test Procedure of Evaluation Board

1. Prepare equipments as below list.
   a. DC power supply
   b. Electronic load
   c. Multimeters
   d. Oscilloscope
2. Check jumper setup to make sure it is a right default configuration for the device under test.
3. Set the power supply to 3.6 V with a current limit higher than 1 A, and then disable the output of the power supply.
4. Connect the power supply to the evaluation board's connectors Vin+ and Vin−.
5. Disable output of the electronic load and connect it to the evaluation board's connectors Vo+ and Vo−.
6. Enable the output of the power supply and check the 1.8 V output voltage of the evaluation board.
7. Set the electronic load to 10 mA and enable its output. Typical input supply current is about 6 mA.
8. Monitor the output voltage and SW node signal using an oscilloscope. The converter should operate in DCM with similar waveforms as shown in Figure 5(a).
9. Increase the electronic load to 1.0 A. Typical input supply current is about 565 mA.
10. Monitor the output voltage and SW node signal using the oscilloscope. The converter should operate in CCM with similar waveforms as shown in Figure 5(b). The switching frequency is about 3 MHz.
11. After the test is done, make sure to disable the output of power supply before remove power connectors to protect the device from damage caused by possible high voltage spike in input.



(a) Io = 10 mA



(b) Io = 1000 mA

Figure 5. Typical Operation Waveforms of NCP6324B/C Evaluation Board

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
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