Design Note – DN05080/D

NCP1060, 12 Vout, 2 Watt Off-line Buck Regulator

Device	Application	Input Voltage	Output Power	Topology	I/O Isolation
NCP1060	Smart Meters, Electric Meters, White Goods	85 to 265 V	Up to 2 W at 12 Vout	Off-Line 100 kHz Buck	Non-isolated

	Output Specification
Output Voltage	12 V, max 15 V depending on selected Z1 diode value
Output Ripple	Less than 1%
Typical Current	100 to 150 mA for 12 V out
Max Current	160 mA
Min Current	0 mA

PFC (Yes/No)	No
Efficiency	See plots below
Inrush Limiting / Fuse	External fuse required
Operating Temp. Range	0 to +50°C (dependent on IC1 cooling)
Cooling Method / Supply Orientation	Convection
Signal Level Control	None

Circuit Description

This design note describes a very simple, low power, constant voltage output buck power converter intended for powering electronics for power goods, electrical meters and industrial equipment where isolation from the AC mains is not required. The switching element in the converter is **onsemi's** NCP106x series of monolithic switchers. In this reference design, the NCP1060 is utilized with a 60 kHz switching frequency and a maximum output current of 250 mA.

This buck circuit utilizes a simple charge pump or "bootstap" type of voltage sensing and regulation scheme composed of D2, C1. This simple sensing technique eliminates the use of an optocoupler in the feedback loop. Thanks an on chip voltage reference and error amplifier no external active components are necessary for regulation. Just simple resistor divider composed of R2, R5 and R6 to bring portion of external voltage to FB pin. This helps to achieve load regulation +/-5% over the loads 100% down to 1% of maximum rated load. Below 1% the output voltage will rise to the value of the overvoltage clamping zener diode D4 across the output. For a 12 V output a typical value for zener diode will be 15 V and at no load the output will be clamped at this level.

The sensed voltage produced on C5 is also used to power the NCP1060 controller through D1 once converter has started. This auxiliary Vdd to run the chip improves the overall efficiency of the circuit and prevents the controller from running in DSS mode under normal load conditions.

Although this is low power output converter, full bridge rectifier is used, to lower input peak current. C4, L2 and C5 form a conducted EMI filter.

The 1.2 mH buck output inductor is available in several surface mount or through hole configurations from multiple vendor. This inductor should be designed to handle high voltage.

Schematic

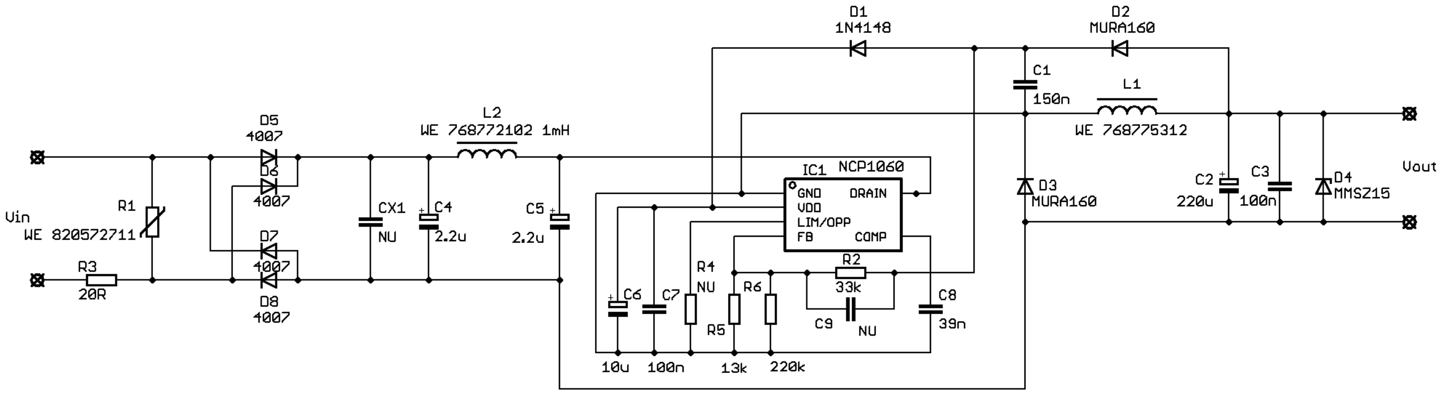

Figure 1 – Buck converter schematic

Principle description

For simplicity in schematic, current loops are colored:

Inductor current (loop A), FB current (loop B), IC supply current (loop C).

Step 1: The MOSFET (in IC1) is turned on:

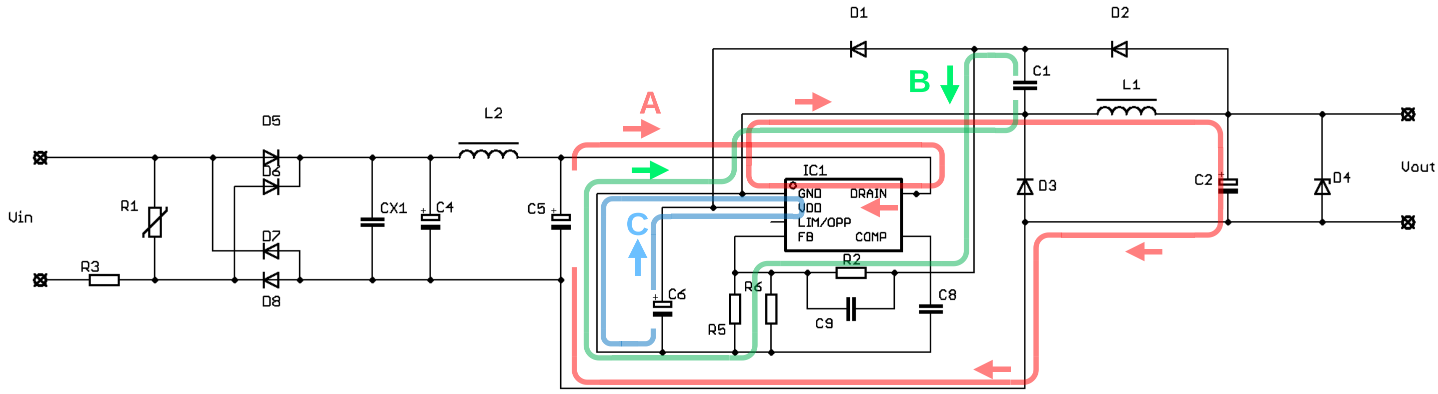

Figure 2 MOSFET is turned on

Let’s assume that the inductor L1 is fully demagnetized before MOSFET turn on, the converter has been running for a while, it is in steady state conditions and the output voltage is at target level.

The power MOSFET in IC1 is turned on, the current (loop A) starts to flow through the inductor and load, so an amount of energy charges C2 and part of the energy flows to the load. The on time and peak current is assessed by the FB loop. The information of output voltage had been stored in C1 in previous cycle. The voltage from C1 is divided by R5, R6 and R2 and it is connected to FB pin. During MOSFET conductive phase, the output voltage is not connected to FB pin, so the on time is given by voltage stored on C1 (during previous cycle), not by the actual output voltage. The C1 capacitor is slowly discharged by FB divider (FB loop (B)). It is important to select C6 value (supply capacitor for IC1) in such a way that the C1 is not discharged by IC1 consumption. Otherwise, the stability will be affected by Vdd capacitor C6. Voltage between C5 minus terminal and IC1 GND pin is almost equal to C5 (input) voltage. The fact that the IC1 GND pin is at a high voltage prevents measuring any IC1's pin voltages with respect to IC GND pin using standard oscilloscope probe, which is usually connected to main grid PE terminal. Only differential probes or battery powered oscilloscope (off the main grid) provide relevant results.

Step 2: The MOSFET (in IC1) is turned off:

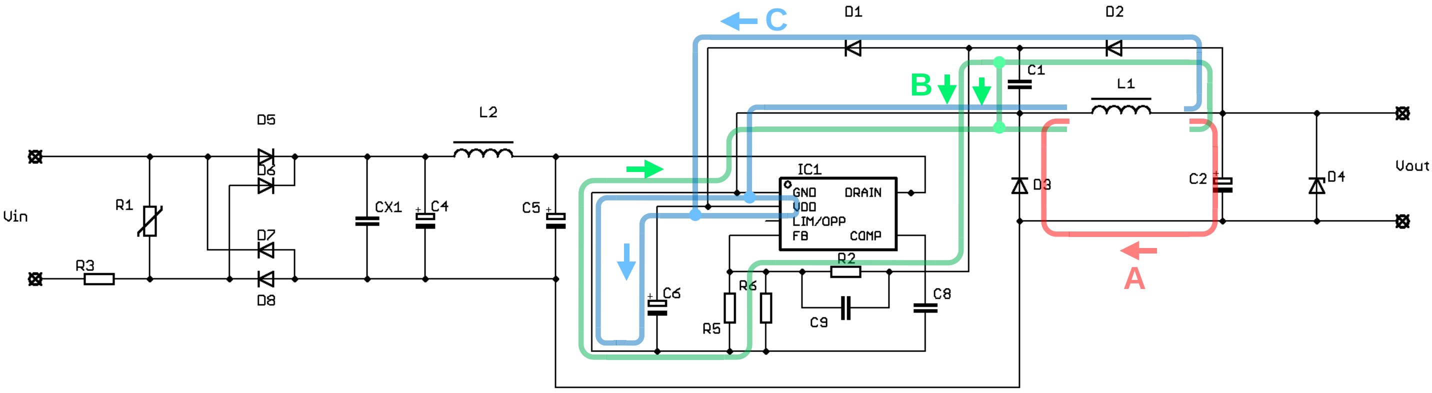

Figure 3 MOSFET is turned off

When the MOSFET is turned off, the inductor L1 will keep current flowing the same way, so the voltage on L1 is reversed and the inductor becomes the source of energy. There are several current loops, through which the current can/will flow. Which current loop will be closed first depends on several factors. If the output is at a light load or no load, the output voltage will be higher than desired by FB divider, so the current (loop A) will not start to flow to the output. We also want C6 to be discharged slower than C1, so the current (loop C) will not supply either IC1 or C6. In these light/no load conditions the current (loop B) will flow to C1 and FB divider first. Please notice the C1 is still not charged to the output voltage level (presented on C2), D3 is not conductive yet, because current (loop A) does not flow to the load. The next step depends on amount of energy stored in L1. If the energy is high enough to cover FB loop (B) and supply (loop C) capacitor demand, then the current (loop A) will start to flow through D3, and C1 capacitor is properly charged to output voltage level (C2). The voltage on C1 will be used in next cycle as the value for on time and current peak settings. In case the energy in L1 is not high enough to push a current (loop A) through D3, then the voltage on C1 will not match the output one (C2). In such case, regulation voltage on C1 will be at target level, but output voltage will be higher than desired. It is important to have enough energy in L1 to open D3 diode (allow the current (loop A) flow through D3). It is recommended not to use too small FB divider resistors as the consumed energy by divider will be missing for closing current loop (A) through D3. In case this situation occurs, Zener diode D4 can save the situation, because it clamps the voltage below critical level. During this period IC GND pin voltage is by Vf of D3 diode drop higher, than the negative terminal of C5. If the drop on D3 is higher than Vf of D3 (see DS), then it can show that there is not enough energy in L1 to open current loop (A) and C2 voltage does not correspond to the one set by FB divider.

Step 3: No energy transfer to the output:

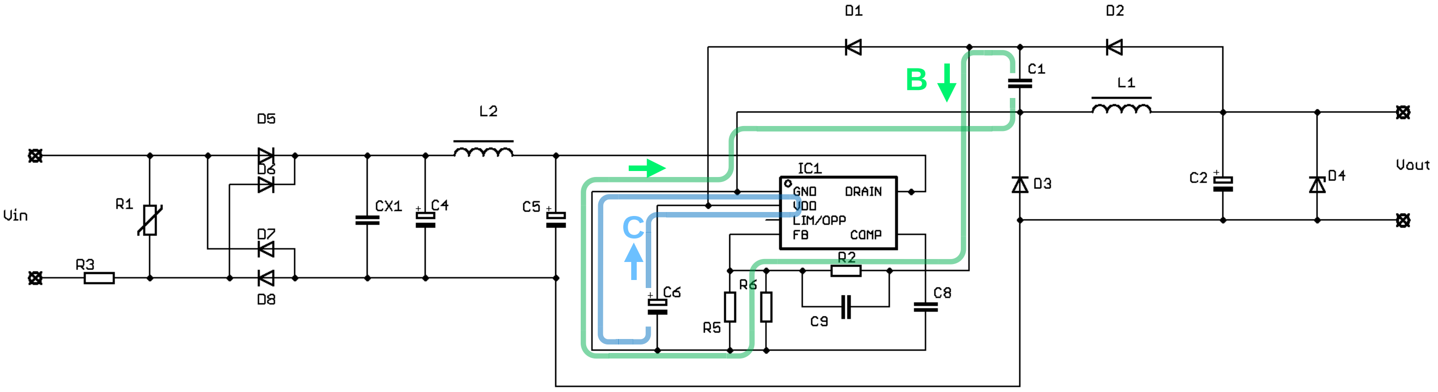

Figure 4 No energy transfer to the output

At the end of Step 2, all energy from L1 is consumed. The IC is supplied (loop C) from C6, capacitor C1 is discharged (loop B) by FB divider. The IC has no information about the real output voltage, so if a short or a step load causes voltage drop on the output, the converter will not react immediately. First, the C1 must be discharged (loop B) below FB reference level, which is done by FB divider and FB pin consumption (See DS). Then the IC clicks, which causes charging C1 capacitor to output voltage level (if the output voltage is higher than the one on C1). If the output voltage is too low, the energy transfer from input to output will start (the IC will start switching). If the output voltage is higher than desired, next switch will placed when C1 is discharged (loop B) below FB pin level. The description here shows, that the IC must switch to “check” output voltage even if the output voltage is higher than desired. Every switching transfers an amount energy to the output, which causes output voltage increase at no/light load conditions. Too keep the output voltage at a safe level, Zener diode D4 is recommended, or the output load must be always high enough to not let the output voltage become too high. During this period, IC1 GND pin voltage is equal to the output voltage (measured with respect to negative terminal of C5).

Step 4: IC1 supply for low output voltage or skip mode:

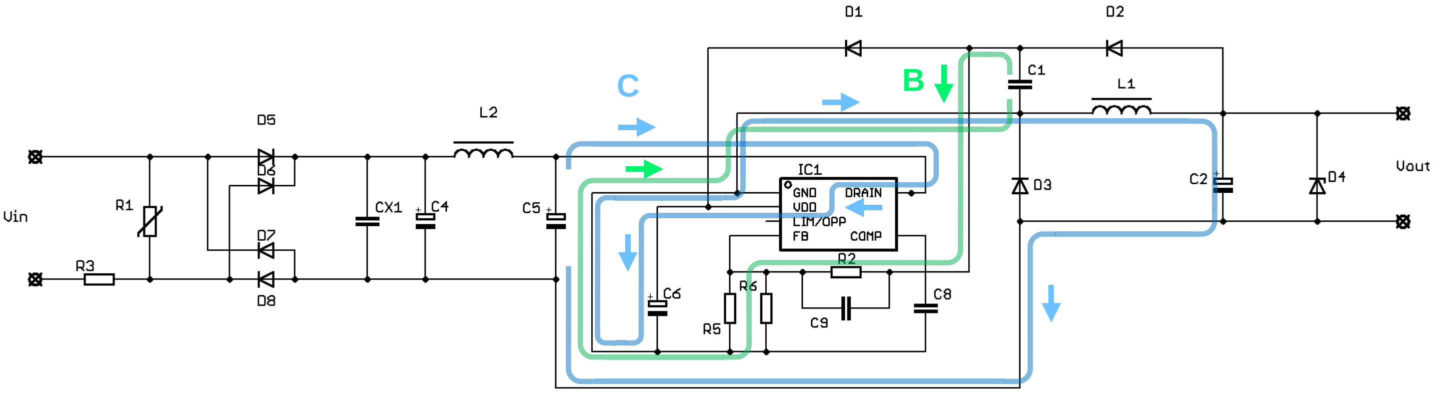

Figure 5 IC supply from DSS

The converter will enter into “self-supply” mode when DSS is activated, which is during skip mode (long off time), or if the IC1 powering is not done from the output voltage (C2). For example if the output voltage is lower than Vdd(min) voltage of the IC1 minus voltage drop on D1. If supplying from the output voltage is not possible or not used, diode D1 is not needed, it can be omitted. The DSS is composed of 8 mA supply, which charges Vdd capacitor from HV line. See IC1 DS for details. If the Vdd voltage is lower than Vdd(min) level, the DSS is activated. The charging current (loop C) 8 mA flows from Drain pin via Vdd capacitor C6 through the load back to C5. The average current is equal to IC1 consumption. The charging (loop C) current is energy transferred to the output, which is not controlled by FB loop (B). Even if the IC1 is not switching at all (i.e. TSD is activated) there is a current (loop C) which flows to the output and increases the output voltage (under no load conditions). This is another reason for using a Zener diode D4 to protect output voltage from becoming too high.

Design procedure

1. On time vs off time ratio:

$$\frac{t_{on}}{t_{off}} = \frac{V_{out} + V_{fD3}}{V_{in} - V_{out}} \qquad \text{eq. 1}$$

The result is a ratio between on time and off time, at which the converter will run in CRM mode. It means the internal MOSFET will be turned on at the moment the inductor current reaches zero. It depends on user needs if CCM or CRM mode is required.

2. Inductor value calculation:

$$L1 = \frac{V_{out}}{f_{sw} \cdot \Delta I_{L1(max)}} \cdot \frac{t_{off}}{t_{on} + t_{off}} \qquad \text{eq. 2}$$

The calculated inductor value will probably not be available, because they are manufactured only in specific values. The peak current for selected inductor is:

$$I_{L1(pk)} = I_{OUT} + \frac{V_{out}}{2 \cdot f_{sw} \cdot L1} \cdot \frac{t_{off}}{t_{on} + t_{off}} \qquad \text{eq. 3}$$

The inductor is exposed to rectified input voltage. Use the inductor with appropriate voltage range.

3. Output capacitor C2 value:

$$C2 \geq \frac{\Delta I_{L1}}{8 \cdot f_{sw} \cdot (\Delta V_{OUT} - \Delta I_{L1} \cdot ESR_{C2})} \qquad \text{eq. 4}$$

where:
ΔI_{L1} - maximum inductor current ripple
f_{SW} - switching frequency
ΔV_{OUT} - allowable output voltage drop during steady state conditions
It is recommended to use higher capacitor value than calculated, to cover energy demand during transients. It takes time to increase power delivery from the input to the output (due to limited FB loop speed). Higher capacitor value can supply the output energy demand before the power supply increases the power delivery. The overshoots will be lower as well for the same reason.

Output capacitor C2 RMS current:

$$I_{C2(RMS)} = I_{OUT} \cdot \frac{t_{off}}{\sqrt{12} \cdot \tau_{L1} \cdot \left(t_{on} + t_{off}\right)}$$ eq. 5

$$\tau_{L1} = \frac{L1}{R_{LOAD} \cdot t_{SW}}$$ eq. 6

4. FB resistor divider sets up the output voltage.
   Value of resistor R2 is determined with respect to power loss on the entire resistor divider. The R5||R6 resistor is calculated using these formulas:

$$I_{R2} = \frac{V_{OUT} - V_{FWD(D2)} + V_{FWD(D3)} - V_{REF}}{R2}$$ eq. 7

$$R5||\mathrm{R6} = \frac{V_{REF}}{I_{R2} + I_{FB}}$$ eq. 8

5. Bootstrap capacitor C1 value assessment requires to consider several aspects:
   - If the IC1 is self-supplied from the output voltage, capacitor C1 must be discharged via FB divider faster than C6 by IC consumption. This inequation must be fulfilled:

$$\frac{\mathrm{C6}}{I_{DD@VDD}} > \frac{\mathrm{C1} \cdot (\mathrm{R2} + \mathrm{R5}||\mathrm{R6})}{V_{DD1}}$$ eq. 9

   - From small signal model point of view, the C6 capacitor is connected in parallel to C1, so it will influence the FB loop control.
   - The buck converter in this arrangement has no direct FB signal from the output voltage. The C1 capacitor is charged to the output voltage during inductor's demagnetization period. The output voltage is not monitored after the demagnetization nor during the on time.
   - If too small C1 value is used, the output voltage will rise up in no load conditions. Every turn on period delivers an energy to the output, which increases the voltage. A dummy load (like Zener diode) effectively clamps the voltage at a safe level.
   - If too big C1 value is used, the output voltage will not rise so high, no load consumption is lower (fewer switching periods are needed to keep C1 at a required level), load regulation is better. On the other hand, any step load (from low to high) causes much deeper voltage drop, because the C1 is charged only from the output, not discharged to the output.

6. For the Comp pin device calculation please see:

https://www.onsemi.com/pub/Collateral/LOOP%20STABILIZATION%20FOR%20106X.PDF

7. Bulk capacitor calculation for full wave bridge rectifier:

$$C5 = \frac{\frac{P_{IN}}{f_{AC}} \cdot \left(\frac{1}{2} + \frac{arcsin \cdot \left(\frac{V_{IN(min)}}{V_{IN(pk)}} \right)}{\pi} \right)}{{V_{IN(pk)}}^2 - {V_{IN(min)}}^2} \qquad \text{eq. 10}$$

Bulk capacitor calculation for single diode rectifier (half wave):

$$C4 = \frac{\frac{P_{IN}}{f_{AC}} \cdot \left(\frac{3}{2} + \frac{arcsin \cdot \left(\frac{V_{IN(min)}}{V_{IN(pk)}} \right)}{\pi} \right)}{{V_{IN(pk)}}^2 - {V_{IN(min)}}^2} \qquad \text{eq. 11}$$

Where:

$V_{IN(min)}$ – minimum voltage on C5

$V_{IN(pk)}$ – maximum voltage on C5, usually it is $V_{IN(pk)} = V_{IN} \cdot \sqrt{2}$

P_{IN} – input power, calculated as P_{OUT} divided by expected efficiency

f_{AC} – main grid frequency

Output Regulation Curve

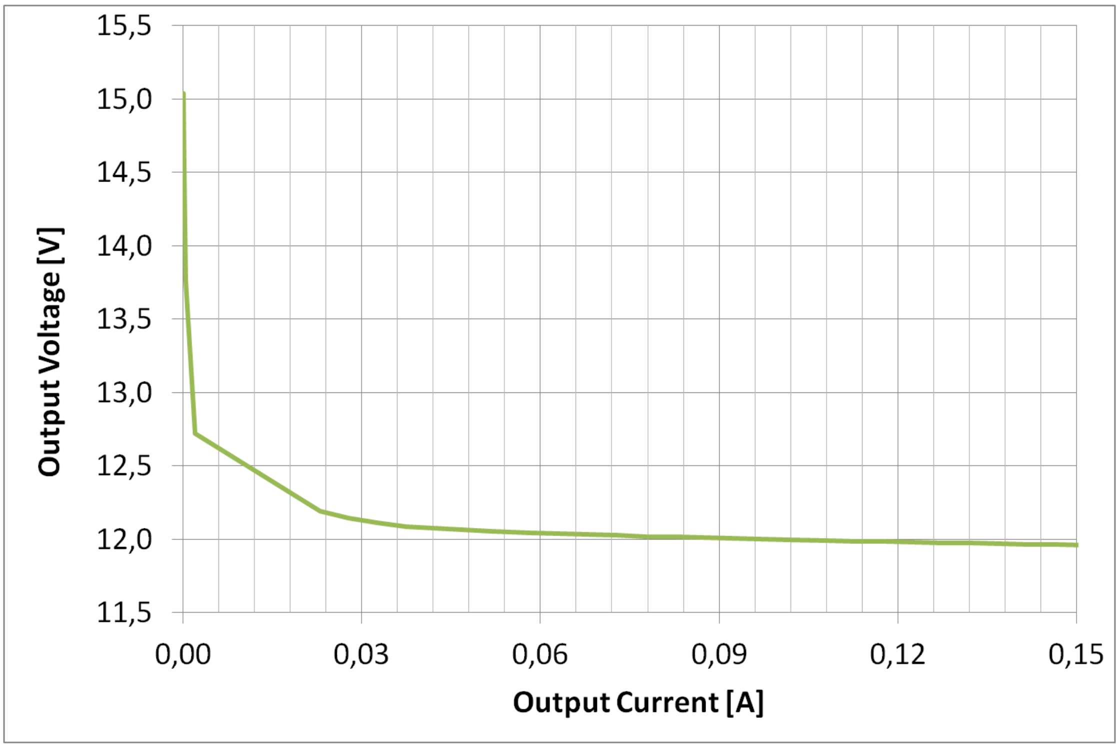

Figure 6 – Output voltage dependency on output current

Typical Efficiency versus Load for 110 V and 230 V

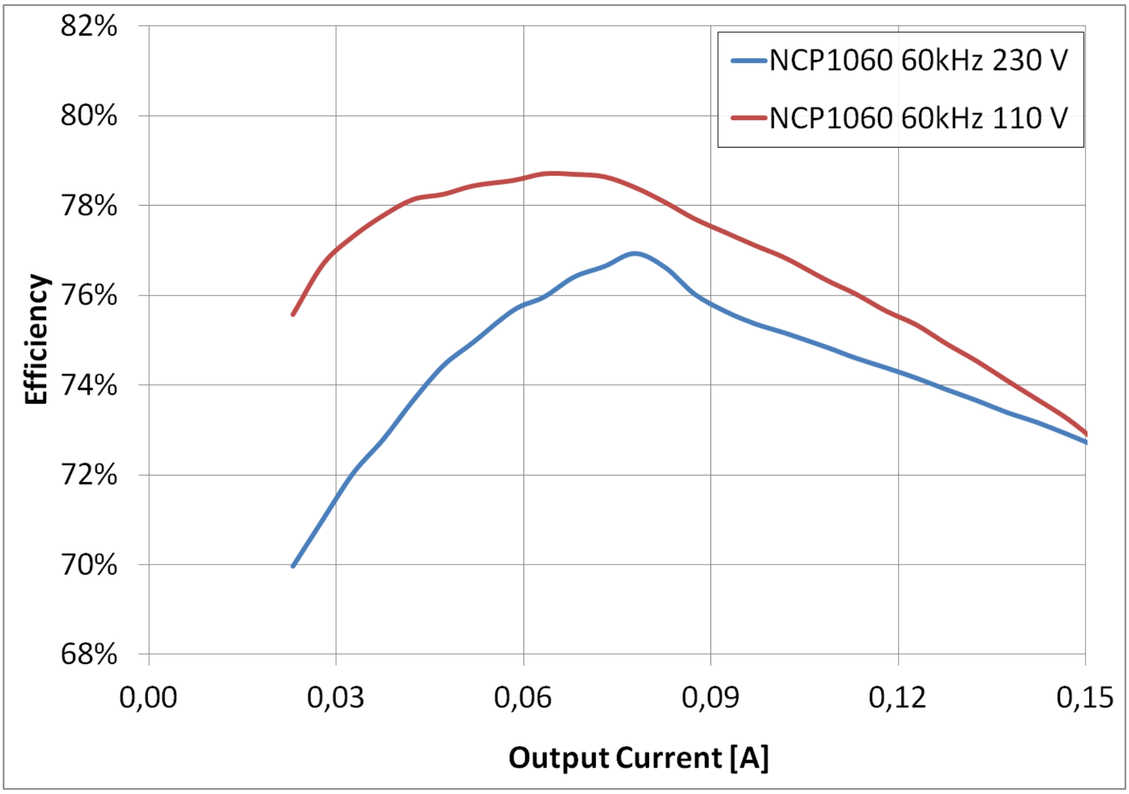

Figure 7 – Efficiency of the Buck Converter

Output Ripple – 150 mA load, 230 Vac Input

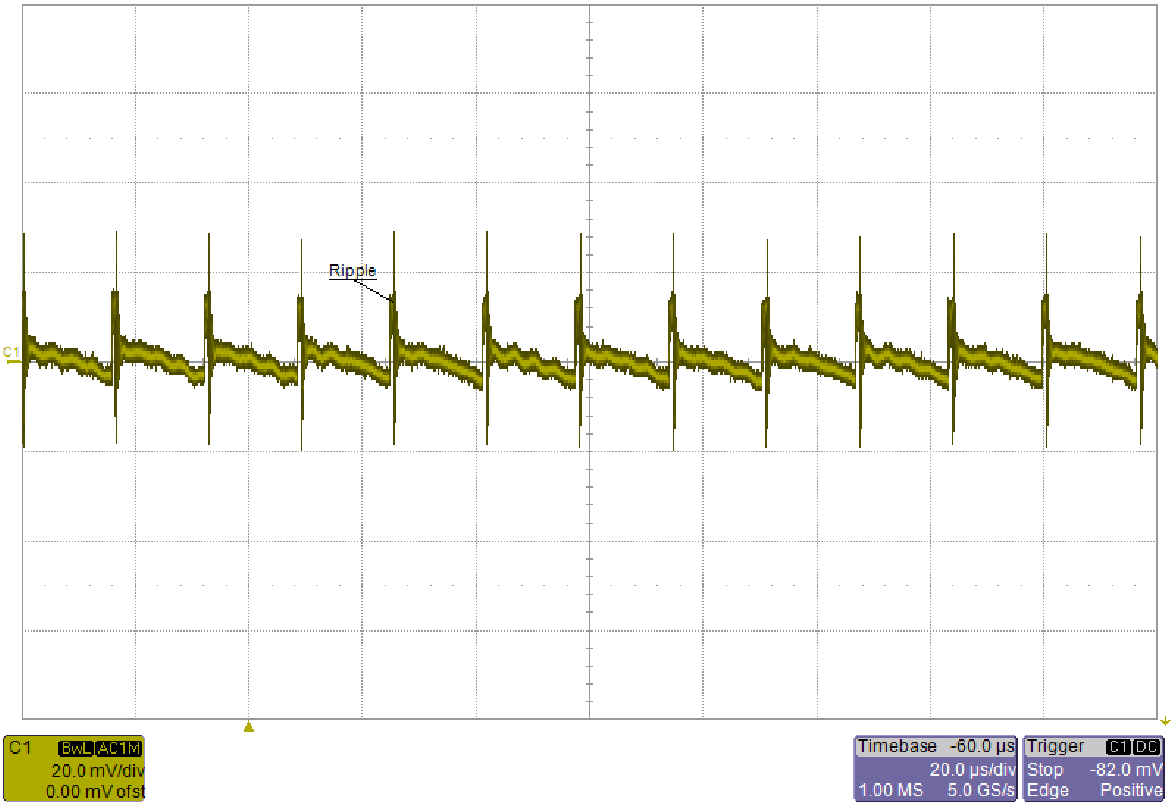

Figure 8 – Output Voltage Ripple at Full Load

References:

onsemi Application Notes: AND8318, AND8328
onsemi Design Notes: DN05014, DN06011, DN06052, DN05058
onsemi NCP1060 monolithic switcher data sheets.

PC Board:

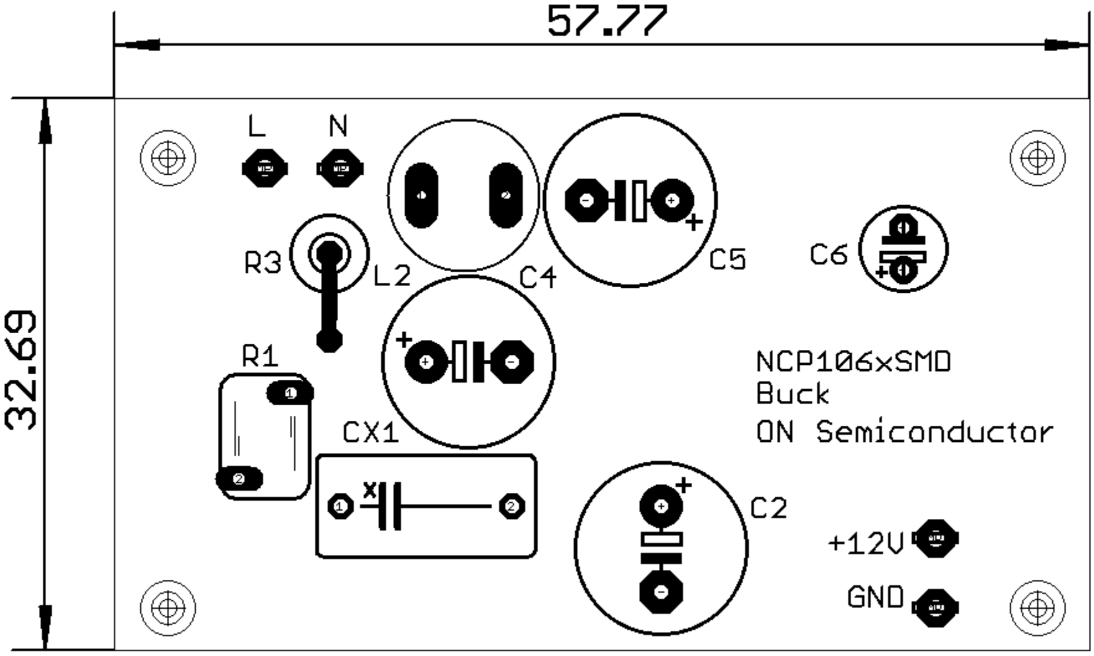

Figure 9 - components position on PCB (top side)

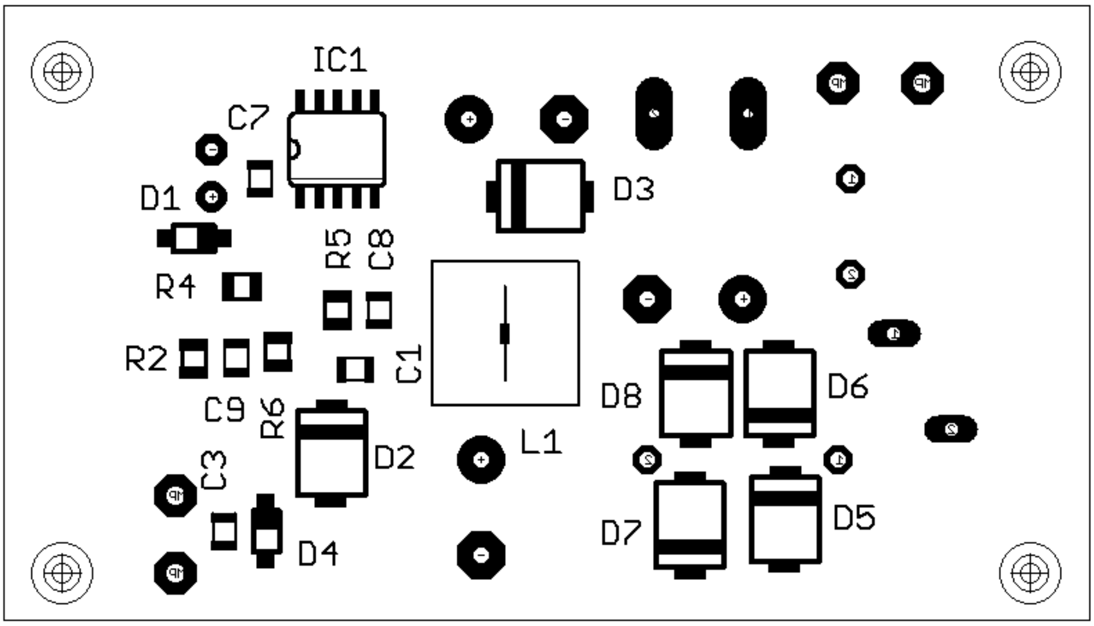

Figure 10 - components position on PCB (bottom side)

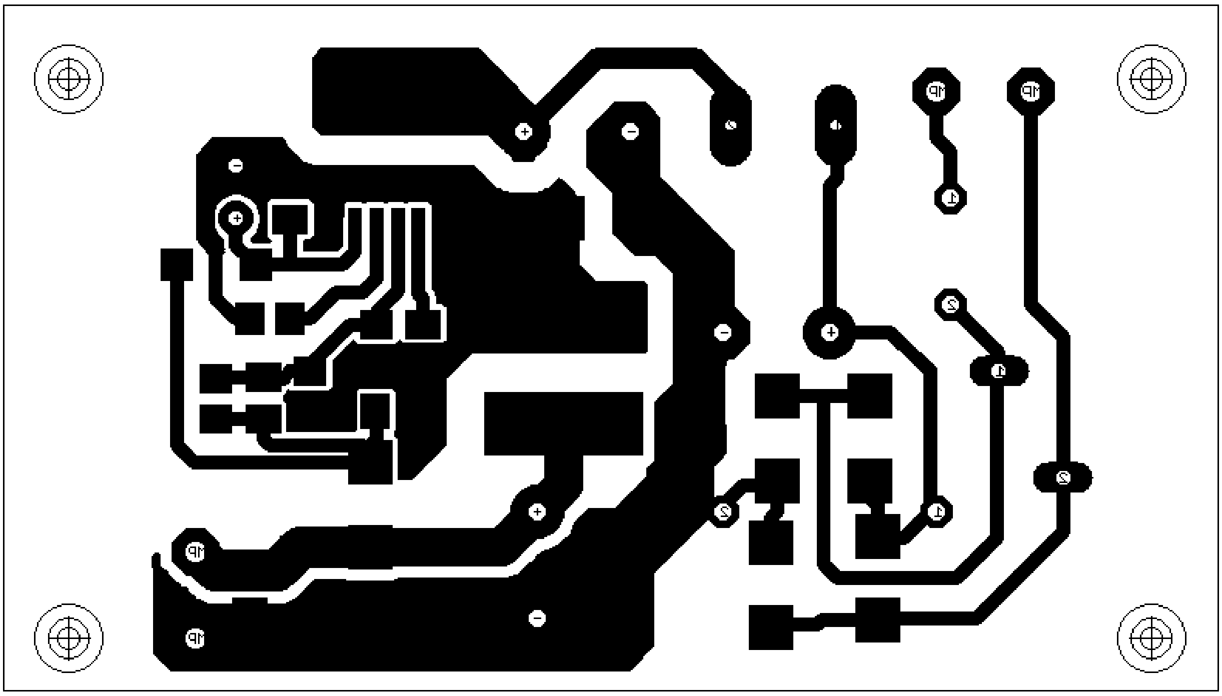

Figure 11 – PCB's bottom side

Table 1– Bill of materials

Designator	Quantity	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number
C1	1	CAPACITOR	150 nF	10%	0805	Kemet	C0805C154K5RACTU
C2	1	ELECTROLYTIC CAPACITOR	220 µF / 35 V	20%	THROUGH HOLE	Koshin	KZH-35V221MG4
C3, C7	2	CAPACITOR	100 nF	10%	0805	Kemet	C0805C104K5RACTU
C4, C5	2	ELECTROLYTIC CAPACITOR	2.2 uF / 450 V	20%	THROUGH HOLE	United Chemi-Con	EKMG451ELL2R2MJC5S
C6	1	ELECTROLYTIC CAPACITOR	10 µF / 25 V	20%	THROUGH HOLE	Koshin	KLH025V100ME3
C8, C9	2	CAPACITOR	39 nF	10%	0805	Kemet	C0805C393K5RACTU
CX1	1	CAPACITOR X2	NU	-	THROUGH HOLE	-	-
D1	1	DIODE	MMSD4148	-	SOD123	**onsemi**	MMSD4148T1G
D2, D3	2	DIODE	MURA160	-	SMA	**onsemi**	MURA160T3G
D4	1	ZENER DIODE	MMSZ15	5%	SOD123	**onsemi**	MMSZ15T1G
D5, D6, D7, D8	4	DIODE	MRA4007	-	SMA	**onsemi**	MRA4007T3G
IC1	1	SWITCHER	NCP1060	-	SOIC10	**onsemi**	NCP1060AD060R2G
L1	1	INDUCTOR	1.2 mH	10%	SMD/SMT	Würth Elektronik	768775312
L2	1	INDUCTOR	1.0 mH	10%	THROUGH HOLE	Würth Elektronik	768772102
(L,N,+12V,GND)	4	TERMINAL PIN	1.0 mm	-	THROUGH HOLE	Ettinger	13.14.119
R1	1	VARISTOR	820572711	-	THROUGH HOLE	Würth Elektronik	820572711
R2	1	RESISTOR	33 kΩ	1%	0805	Rohm Semiconductor	MCR10ERTF3302
R3	1	RESISTOR	20 Ω	5%	0613	VIshay BC Components	AC03000002009JAC00
R4	1	RESISTOR	NU	-	0805	-	-
R5	1	RESISTOR	13 kΩ	1%	0805	Rohm Semiconductor	MCR10ERTF1302
R6	1	RESISTOR	220 kΩ	1%	0805	Rohm Semiconductor	MCR10ERTF2203

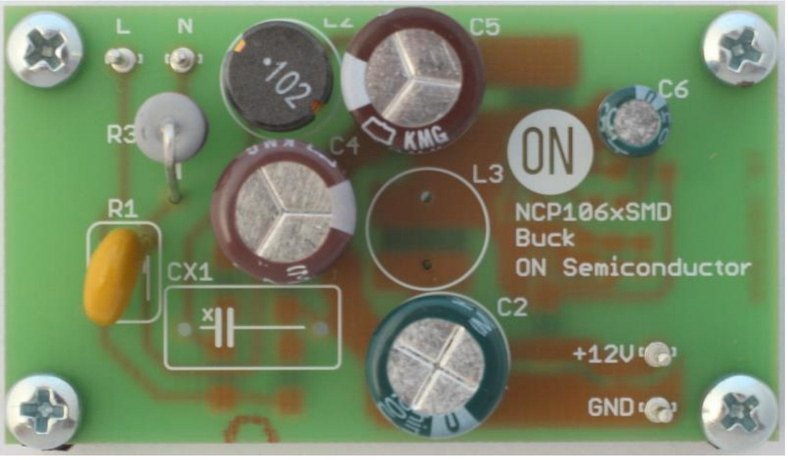

Figure 12 – PCB's top side

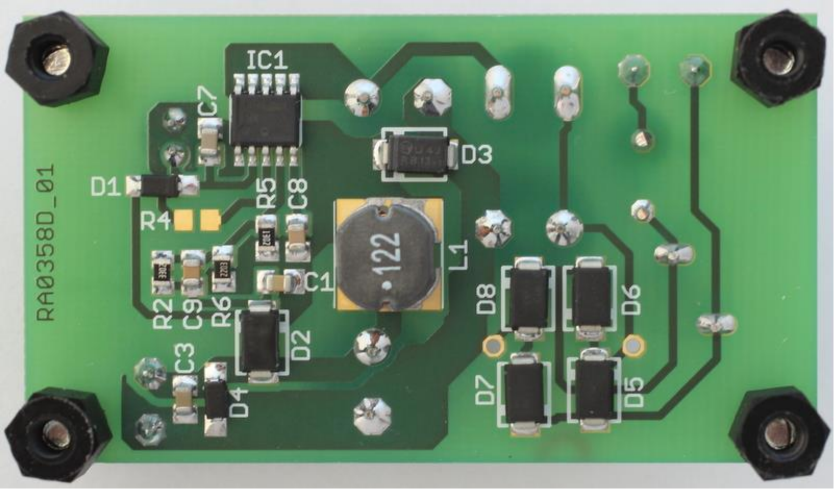

Figure 13 – PCB's bottom side