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DATA SHEET
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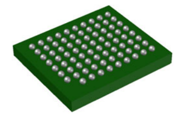
1/3.6-inch CMOS Digital Image Sensor

Product Preview

AR0341AT



IBGA79
CASE 503CS

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

General Description

The **onsemi** AR0341AT is a 1/3.6−inch CMOS digital image sensor with a 1920 H x 1536 V active−pixel array. This advanced automotive sensor captures images in high dynamic range with LED flicker mitigation (LFM) using rolling−shutter readout. The AR0341AT is able to capture both low light and extremely bright illumination in every frame with a 2.1 μm Super Exposure (SE) BSI pixel. This pixel enables 150 dB of dynamic range without the need for auto exposure adjustment. This significantly reduces latency in scene dependent critical automotive systems, enabling faster and safer data gathering and decision making. A dual output data path can be used to send both 3M and windowed images simultaneously for both ADAS systems and viewing applications, removing the need for two cameras. The sensor includes flexible functions such as smart ROI, windowing, and can achieve 60 frames per second in full−resolution. The sensor was designed following ASIL−C design processes, and the sophisticated real time safety mechanisms and fault detection features on the AR0341AT exceed ASIL−B compliance metrics.

Table 1. KEY PARAMETERS

Parameter		Typical Value
Optical Format		1/3.6 inch (5.16 mm)
Active Pixels		1920 x 1536 = 3M
Pixel Size		2.1 μm
Color Filter Array		RGGB
CRA		15°
Shutter Type		Electronic rolling shutter
Input Clock Range		10 – 50 MHz
Output	Serial	MIPI CSI−2 12, 16, 24 (22 significant bits) and 28−bit (26 significant bits)
Frame Rate	Full Resolution	Up to 60 fps in Super Exposure + T2 mode Up to 60 fps in Super Exposure mode
Responsivity (Note 1)	RGB (Green)	16 ke−/lux*sec
Maximum Dynamic Range (Note 2)		up to 150 dB in Super Exposure + T2 mode up to 120 dB in Super Exposure mode
Supply Voltage	I/O	1.8 V
	Digital	1.0 V
	Analog	2.8 V and 1.8 V
	MIPI	1.0 V
Power Consumption (Typical)		<300 mW Full resolution, SE + T2, 12−bit, 30 FPS, 25°C ambient temperature
Operating Temperature		−40°C to +105°C (ambient) −40°C to +125°C (junction)
Package Options		79 iBGA 7.5x6.5 mm

1. D65, 670 nm IRCF
2. Up to T_J = 80°C and ADACD Filter Enabled

Features

- On−chip Combined HDR RAW Output, up to 26−bit (>150 dB) with Companding Down to 16 or 12−bit
- New High−Performance 2.1 μm BSI Pixel
- Advanced HDR Image Combination with Flexible Exposure Ratio Control
- 1920 x 1536 at up to 60 fps
- Real−time Functional Safety Mechanisms and End of Frame Fault Reporting
- Designed following ASIL−C Process
- Data Interfaces: 4−lane MIPI CSI−2
- On Sensor Black Level Control
- Support for 150 dB HDR+LFM with Super Exposure (SE) + T2 Mode (Note 2)
- Support for 120 dB HDR with Super Exposure (SE) Mode (Note 2)
- Dual Output Datapath to Enable Multi−function Systems
- Spread−spectrum Input Clock Support
- Multi−Camera Synchronization Support

NOTE: PRODUCT FEATURES AND SETTINGS DESCRIBED IN THE DATA SHEET MUST BE CONFIGURED AS DEFINED IN THE PRODUCTS' DEVELOPER GUIDE AND REGISTER REFERENCE. PLEASE CONTACT YOUR **onsemi** SUPPORT CHANNEL FOR ACCESS TO THE PRODUCTS' DEVELOPER GUIDE, REGISTER REFERENCE, AND SUPPORT TO PROPERLY ENABLE THE PRODUCT'S FEATURES AND SETTINGS TO MEET YOUR SPECIFIC REQUIREMENTS.

Features (continued)

- AEC−Q100 Grade 2
- Simplified Sensor Control Command Set
- CFA Option: RGGB
- This is a Pb−Free Device

Applications

- Automotive Front Camera (ADAS)
- Mirror Replacement (CMS)
- ADAS + Viewing Fusion
- High Dynamic Range Imaging
- Surround View + Sensing

Table 2. ORDERING INFORMATION

Part Number	Description	Orderable Product Attribute Description
AR0341ATSC15XUEA0−DPBR	RGGB, 15°CRA	3 MP LFM HDR RAW sensor, Dry Pack with Protective Film, Double sided BBAR, iBGA, Engineering Sample
AR0341ATSC15XUEA0−TPBR	RGGB, 15°CRA	3 MP LFM HDR RAW sensor, Tape&Reel with Protective Film, Double sided BBAR, iBGA, Engineering Sample

NOTE: Contact the **onsemi** sales or marketing representative to discuss your specific requirements.

GENERAL DESCRIPTION

The **onsemi** AR0341AT can be operated in its default mode or programmed for frame size, exposure, gain, and other parameters. The default mode is a 1920 x 1536 resolution image at 30 frames per second (fps) dual−exposure HDR+LFM using the Super Exposure pixel. In high dynamic range mode, it outputs 12−bit, 16−bit, 20−bit, 22−bit (padded to 24−bit) companded or up to 26−bit (padded to 28−bit) linearized data using the MIPI port. The device may be operated in video (master) mode or in single frame trigger mode.

FRAME_VALID and LINE_VALID can be programmed to output by GPIO pins.

The AR0341AT includes additional features to allow application−specific tuning: windowing and offset, auto black level correction, and on−board temperature sensor. Optional register information and histogram statistic information can be embedded in the last lines of the image frame.

The sensor digital data path includes a fixed data pedestal. The data pedestal is the digital value of the pixel in the dark, which remains constant across integration time and temperature. The default value in all operating modes is 168 codes.

The sensor is designed to operate in a wide temperature range (−40°C to +125°C junction).

FUNCTIONAL OVERVIEW

The AR0341AT is a progressive−scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on−chip, phase−locked loop (PLL) that can be optionally enabled to generate all internal clocks from a single master input clock running between 10 and 50 MHz.

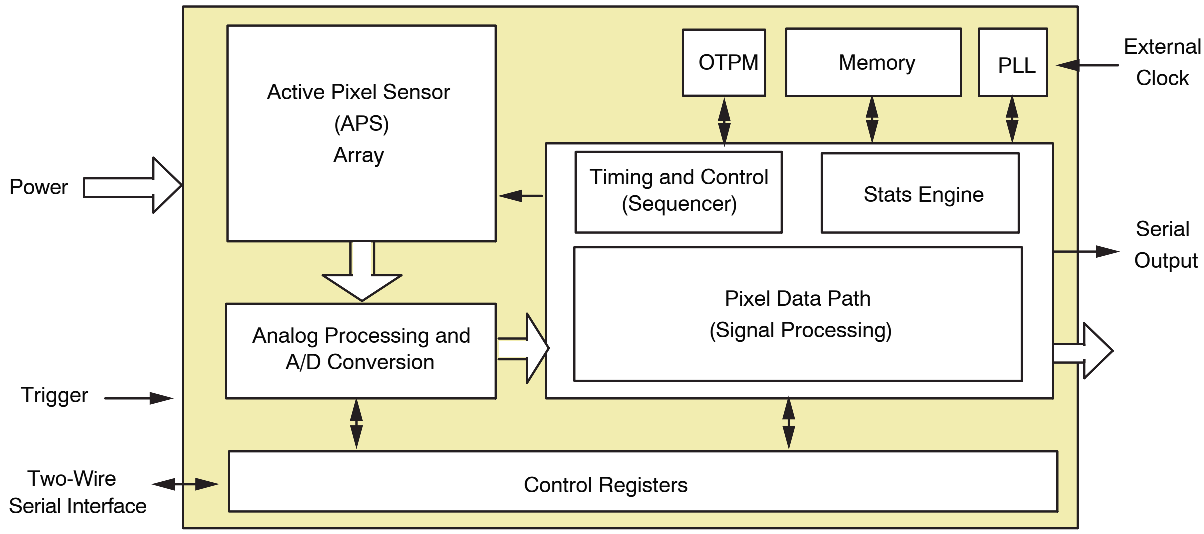


Figure 1. Block Diagram

User interaction with the sensor is through the two−wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 3 Mp BSI Active−Pixel Sensor array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row integrate incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an analog−to−digital converter (ADC). The output from the ADC is a 12−bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain). The sensor offers a high dynamic range mode of operation where multiple images are combined onchip to produce a single image at 26−bit per pixel value. A compressing mode is further offered to allow this 26−bit pixel value to be transmitted to the host system as a 12−, 16−, or 24−bit (22 significant bits) value with close to zero loss in image quality.

Features Overview

The AR0341AT has a wide array of features to enhance functionality and to increase versatility. A summary of features follows. Please refer to the AR0341AT Developer Guide for detailed feature descriptions, register settings, and tuning guidelines and recommendations.

- Operating Modes
  The AR0341AT works in master (video), trigger (single frame), or Auto Trigger modes. In master mode, the sensor generates the integration and readout timing. In trigger mode, it accepts an external trigger to start exposure, then generates the exposure and readout timing. The exposure time is programmed through the two−wire serial interface for both modes.
- Smart ROI
  Up to 8 configurable regions of interest (ROIs) can be configured to limit sensor output to key portions of the frame, reducing camera bandwidth requirements.
- Dual Output Datapath
  The dual datapath allows for the simultaneously outputting of both 3 Mp capture and cropped, windowed captured from the same exposure.
- MIPI
  The AR0341AT image sensor supports only 4−lane MIPI CSI−2 D−PHY 2.5
- PLL
  An on chip PLL provides reference clock flexibility
- Reset
  The AR0341AT may be reset by a register write, or by a dedicated input pin.
- Output Enable
  The AR0341AT output pins may be tri−stated using dedicated register bits.
- Temperature Sensor
- Black Level Correction
- Row Noise Correction
- Digital Correlated Double Sampling (DCDS)

- Test Patterns
  Several test patterns may be enabled for debug purposes. These include a solid color and a walking 1s test pattern.

ASIL / ISO26262 Support Features

The AR0341AT incorporates many features assisting the achievement of ASIL−C system compliance by a system that integrates it. Please refer to the AR0341AT Safety Manual for more information.

PIXEL DATA FORMAT

Pixel Array Structure

The AR0341AT pixel array is configured as 1936 columns by 1544 rows (see Figure 2). The dark pixels are optically black and are used internally to monitor black level. There are 1936 columns by 1544 rows of optically active pixels. While the sensor's format is 1920 x 1536, the additional active columns and active rows are included for use when horizontal or vertical mirrored readout is enabled, to allow readout to start on the same pixel. The pixel adjustment is always performed for RGGB. The active area is surrounded with optically transparent dummy pixels to improve image uniformity within the active area. Not all dummy pixels or barrier pixels can be read out. The optical center of the readable active pixels can be found between X_ADDR 967 and 968, and between Y_ADDR 771 and 772.

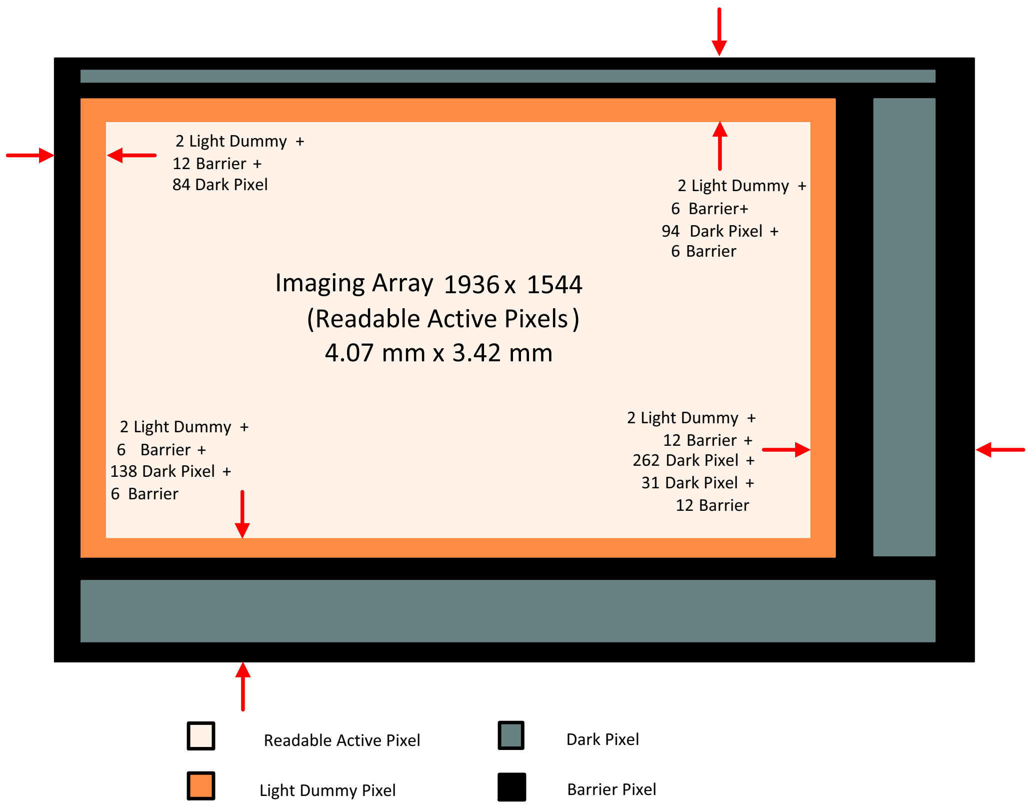


Figure 2. Pixel Array Description

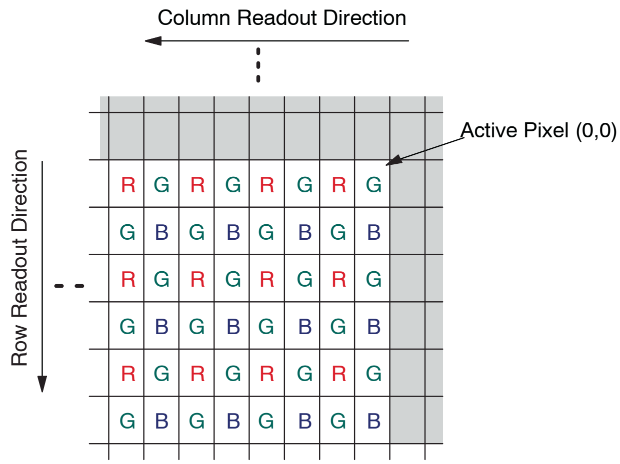


Figure 3. Pixel Color Pattern Detail (Top Right Corner) Bayer

Default Readout Order

By convention, the sensor core pixel array is shown with pixel (0,0) in the top right corner (see Figure 3). This reflects the actual layout of the array on the die.

When the sensor is imaging, the active surface of the sensor faces the scene as shown in Figure 4. When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced as shown in Figure 4.

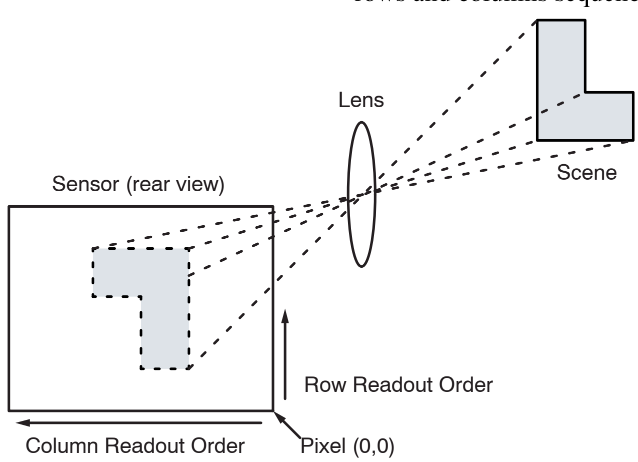
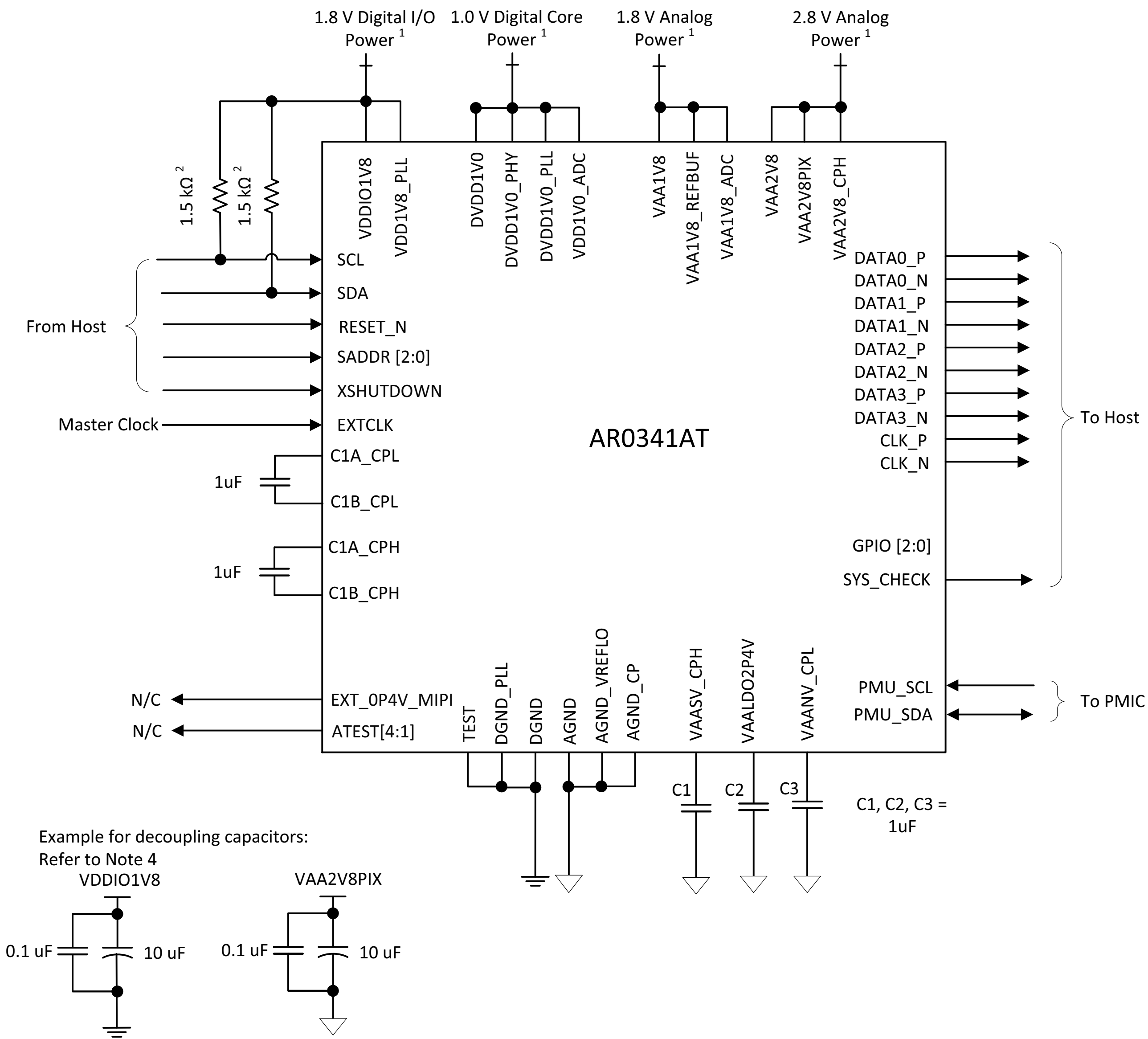


Figure 4. Imaging a Scene

CONFIGURATION AND PINOUT

The figures and tables below show a typical configuration for the AR0341AT image sensor and show the package pinout.



NOTES:
1. All power supplies must be adequately decoupled.
2. **onsemi** recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two−wire speed.
3. With default GPIO configuration setting, GPIO[2:0] can be left unconnected if not used.
4. **onsemi** recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Refer to the AR0341AT demo head-board schematics for circuit recommendations.
5. **onsemi** recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
6. I/O signals voltage must be configured to match VDDIO1V8 voltage to minimize any leakage currents.
7. Please refer to AND9640/D for board design best practices.

Figure 5. Typical Configuration, Four−Lane MIPI

Table 3. PIN DESCRIPTIONS, 7 x 6.5 mm, 79−BALL iBGA

Name	iBGA pin	Type	Description
AGND	A10, D2, D9, F10, G5, G7, G8, H3, H10	Analog Ground	Analog ground
AGND_CP	E10	Analog Ground	Analog ground
AGND_VREFLO	G6	Analog Ground	Analog ground
ATEST1	E7		Analog manufacturing test access, must be left floating for normal operation
ATEST2	F7		Analog manufacturing test access, must be left floating for normal operation
ATEST4	G4		Analog manufacturing test access, must be left floating for normal operation
ATEST_TS2	D3		Analog manufacturing test access, must be left floating for normal operation
C1A_CPH	E9	Input/Output	External bypass reference
C1A_CPL	F9	Input/Output	External bypass reference
C1B_CPH	E8	Input/Output	External bypass reference
C1B_CPL	F8	Input/Output	External bypass reference
CLKN	B6	Output	MIPI serial clock differential N
CLKP	A6	Output	MIPI serial clock differential P
DATA0N	B4	Output	MIPI serial data, lane 0, differential N
DATA0P	A4	Output	MIPI serial data, lane 0, differential P
DATA1N	B5	Output	MIPI serial data, lane 1, differential N
DATA1P	A5	Output	MIPI serial data, lane 1, differential P
DATA2N	B7	Output	MIPI serial data, lane 2, differential N
DATA2P	A7	Output	MIPI serial data, lane 2, differential P
DATA3N	B8	Output	MIPI serial data, lane 3, differential N
DATA3P	A8	Output	MIPI serial data, lane 3, differential P
DGND	B1, C6, C9, D8, E2, H1, H6	Digital Ground	Digital ground
DGND_PLL	B3	Digital Ground	Digital ground
DVDD1V0	C1, C3, C7, E1, G2, H5	Power	Core digital power, 1.0 V nominal
DVDD1V0_PHY	C5	Power	PHY power, 1.0 V nominal
DVDD1V0_PLL	C4	Power	PLL power, 1.0 V nominal
EXTCLK	B2	Input	External Input clock
EXT_0P4V_MIPI	C8	Power	Left floating for normal operation
GPIO_0	F2	Input/Output	General Purpose Input/Output
GPIO_1	F3	Input/Output	General Purpose Input/Output
GPIO_2	F4	Input/Output	General Purpose Input/Output
PMU_SCL	F5	Input	Pulled High for normal operation
PMU_SDA	F6	Input/Output	Pulled High for normal operation
RESET_N	D7	Input	Asynchronous reset (active LOW) all settings are restored to factory default
SADDR0	D5	Input	Two−Wire Serial address select (LSB)
SADDR1	C2	Input	Two−Wire Serial address select
SADDR2	D4	Input	Two−Wire Serial address select (MSB)
SCL	D6	Input	Two−Wire Serial clock input
SDA	E6	Input / Output	Two−Wire Serial data I/O
SYS_CHECK	E5	Output	Combined OR of all error flags

Table 3. PIN DESCRIPTIONS, 7 x 6.5 mm, 79−BALL iBGA (continued)

Name	iBGA pin	Type	Description
TEST	E3	Input	Manufacturing test enable pin (Tied to GND for normal operation)
VAA1V8	C10, G10	Power	Analog power, 1.8 V nominal
VAA1V8_ADC	H8	Power	ADC power, 1.8 V nominal
VAA1V8_REFBUF	F1	Power	ADC reference buffer power, 1.8 V nominal
VAA2V8	D1, D10, H2, H7	Power	Analog power, 2.8 V nominal
VAA2V8PIX	G3, G9	Power	Analog pixel array power, 2.8 V nominal
VAA2V8_CPH	B9	Power	Analog charge pump power, 2.8 V nominal
VAALDO2P4V	A9	Power	Requires 1 μF ceramic cap on board
VAANV_CPL	H9	Power	Requires 1 μF ceramic cap on board
VAASV_CPH	B10	Power	Requires 1 μF ceramic cap on board
VDD1V0_ADC	H4	Power	ADC power, 1.0 V nominal
VDD1V8_PLL	A3	Power	PLL power, 1.8 V nominal
VDDIO1V8	A2, G1	Power	Digital I/O power, 1.8 V nominal
XSHUTDOWN	E4	Input	Asynchronous active low reset de−asserted by external PMIC after all output voltage rails have been configured. It should be tied off to 1, if external PMIC is not used

	1	2	3	4	5	6	7	8	9	10
A		VDDIO1V8	VDD1V8_PLL	DATA0P	DATA1P	CLKP	DATA2P	DATA3P	VAALDO2P4V	AGND
B	DGND	EXTCLK	DGND_PLL	DATA0N	DATA1N	CLKN	DATA2N	DATA3N	VAA2V8_CPH	VAASV_CPH
C	DVDD1V0	SADDR1	DVDD1V0	DVDD1V0_PLL	DVDD1V0_PHY	DGND	DVDD1V0	EXT_0P4V_MIPI	DGND	VAA1V8
D	VAA2V8	AGND	ATEST_TS2	SADDR2	SADDR0	SCL	RESET_N	DGND	AGND	VAA2V8
E	DVDD1V0	DGND	TEST	XSHUTDOWN	SYS_CHECK	SDA	ATEST1	C1B_CPH	C1A_CPH	AGND_CP
F	VAA1V8_REFBUF	GPIO_0	GPIO_1	GPIO_2	PMU_SCL	PMU_SDA	ATEST2	C1B_CPL	C1A_CPL	AGND
G	VDDIO1V8	DVDD1V0	VAA2V8PIX	ATEST4	AGND	AGND_VREFLO	AGND	AGND	VAA2V8PIX	VAA1V8
H	DGND	VAA2V8	AGND	VDD1V0_ADC	DVDD1V0	DGND	VAA2V8	VAA1V8_ADC	VAANV_CPL	AGND

Figure 6. 7.5 x 6.5 mm 79−Ball iBGA Package (Top View)

TWO−WIRE SERIAL REGISTER INTERFACE

The two−wire serial interface bus enables read/write access to control and status registers within the AR0341AT. The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (SCLK) that is an input to the sensor and is used to synchronize transfers. Data is transferred between the master and the slave on a bidirectional signal (SDATA). SDATA is pulled up to VDD_IO off−chip by a 1.5 kΩ resistor. Either the slave or master device can drive SDATA LOW − the interface protocol determines which device is allowed to drive SDATA at any given time.

The protocols described in the two−wire serial interface specification allow the slave device to drive SCLK LOW; the AR0341AT uses SCLK as an input only and therefore never drives it LOW.

Protocol

Data transfers on the two−wire serial interface bus are performed by a sequence of low−level protocol elements:

1. A (repeated) start condition
2. A slave address/data direction byte
3. An (a no) acknowledge bit
4. A message byte
5. A stop condition

The bus is idle when both SCLK and SDATA are HIGH. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

Start Condition

A start condition is defined as a HIGH−to−LOW transition on SDATA while SCLK is HIGH. At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a "repeated start" or "restart" condition.

Stop Condition

A stop condition is defined as a LOW−to−HIGH transition on SDATA while SCLK is HIGH.

Data Transfer

Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no−acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes.

One data bit is transferred during each SCLK clock period. SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

Slave Address/Data Direction Byte

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A "0" in bit [0] indicates a WRITE, and a "1" indicates a READ. The default slave addresses used by the AR0341AT are 0x20 (write address) and 0x21 (read address) in accordance with the specification. An additional 7 alternate slave address can be selected by enabling and asserting the SADDR [2:0] inputs.

Message Byte

Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data.

Acknowledge Bit

Each 8−bit data transfer is followed by an acknowledge bit or a no−acknowledge bit in the SCLK clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases SDATA. The receiver indicates an acknowledge bit by driving SDATA LOW. As for data transfers, SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

No Acknowledge Bit

The no−acknowledge bit is generated when the receiver does not drive SDATA LOW during the SCLK clock period following a data transfer. A no−acknowledge bit is used to terminate a read sequence.

Typical Sequence

A typical READ or WRITE sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8−bit slave address/data direction byte. The last bit indicates whether the request is for a read or a write, where a "0" indicates a write and a "1" indicates a read. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

If the request was a WRITE, the master then transfers the 16−bit register address to which the WRITE should take place. This transfer takes place as two 8−bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master then transfers the data as an 8−bit sequence; the slave sends an acknowledge bit at the end of the sequence. The master stops writing by generating a (re)start or stop condition.

If the request was a READ, the master sends the 8−bit write slave address/data direction byte and 16−bit register address, the same way as with a WRITE request. The master then generates a (re)start condition and the 8−bit read slave address/data direction byte, and clocks out the register data, eight bits at a time. The master generates an acknowledge bit after each 8−bit transfer. The slave's internal register address is automatically incremented after every 8 bits are transferred. The data transfer is stopped when the master sends a no−acknowledge bit.

Single READ from Random Location

This sequence (Figure 7) starts with a dummy WRITE to the 16−bit address that is to be used for the READ. The master terminates the WRITE by generating a restart condition. The master then sends the 8−bit read slave address/data direction byte and clocks out one byte of register data. The master terminates the READ by generating a no−acknowledge bit followed by a stop condition. Figure 7 shows how the internal register address maintained by the AR0341AT is loaded and incremented as the sequence proceeds.

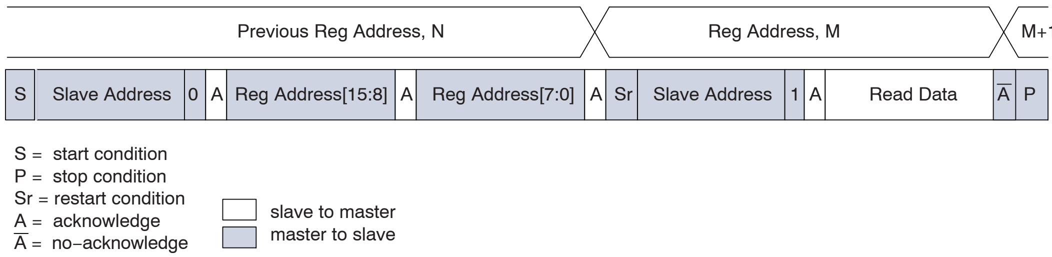


Figure 7. Single READ from Random Location

Single READ from Current Location

This sequence (Figure 8) performs a read using the current value of the AR0341AT internal register address. The master terminates the READ by generating a no−acknowledge bit followed by a stop condition. The figure shows two independent READ sequences.

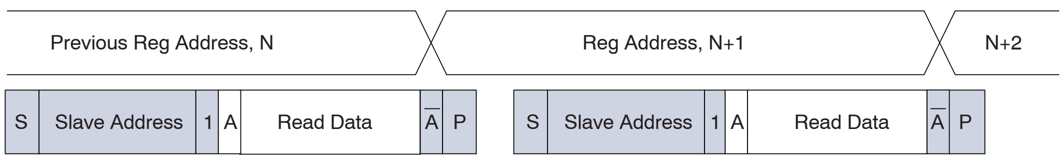


Figure 8. Single READ from Current Location

Sequential READ, Start from Random Location

This sequence (Figure 9) starts in the same way as the single READ from random location (Figure 7). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

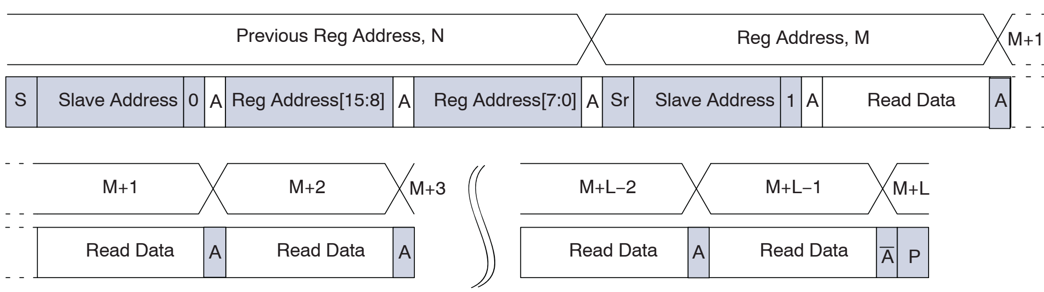


Figure 9. Sequential READ, Start from Random Location

Sequential READ, Start from Current Location

This sequence (Figure 10) starts in the same way as the single READ from current location (Figure 8). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until "L" bytes have been read.

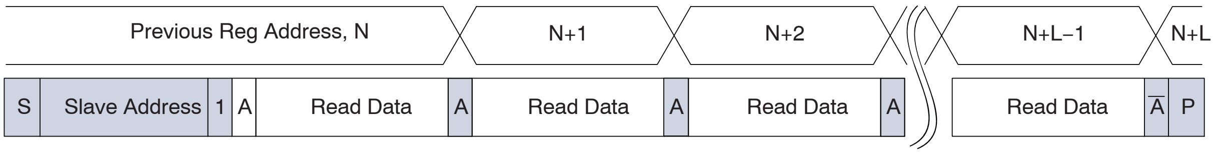


Figure 10. Sequential READ, Start from Current Location

Single WRITE to Random Location

This sequence (Figure 11) begins with the master generating a start condition. The slave address/data direction byte signals a WRITE and is followed by the HIGH then LOW bytes of the register address that is to be written. The master follows this with the byte of write data. The WRITE is terminated by the master generating a stop condition.

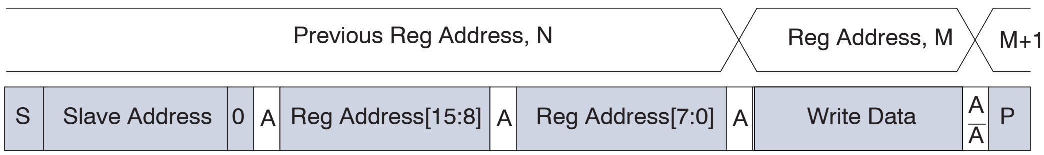


Figure 11. Single WRITE to Random Location

Sequential WRITE, Start at Random Location

This sequence (Figure 12) starts in the same way as the single WRITE to random location (Figure 11). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte WRITEs until "L" bytes have been written. The WRITE is terminated by the master generating a stop condition.

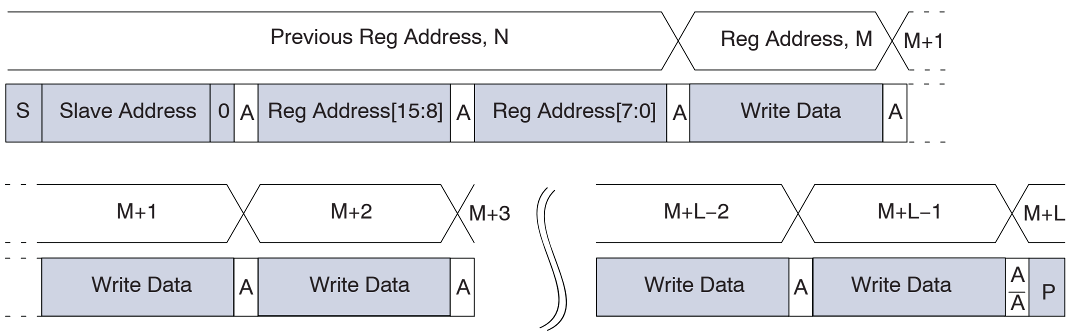
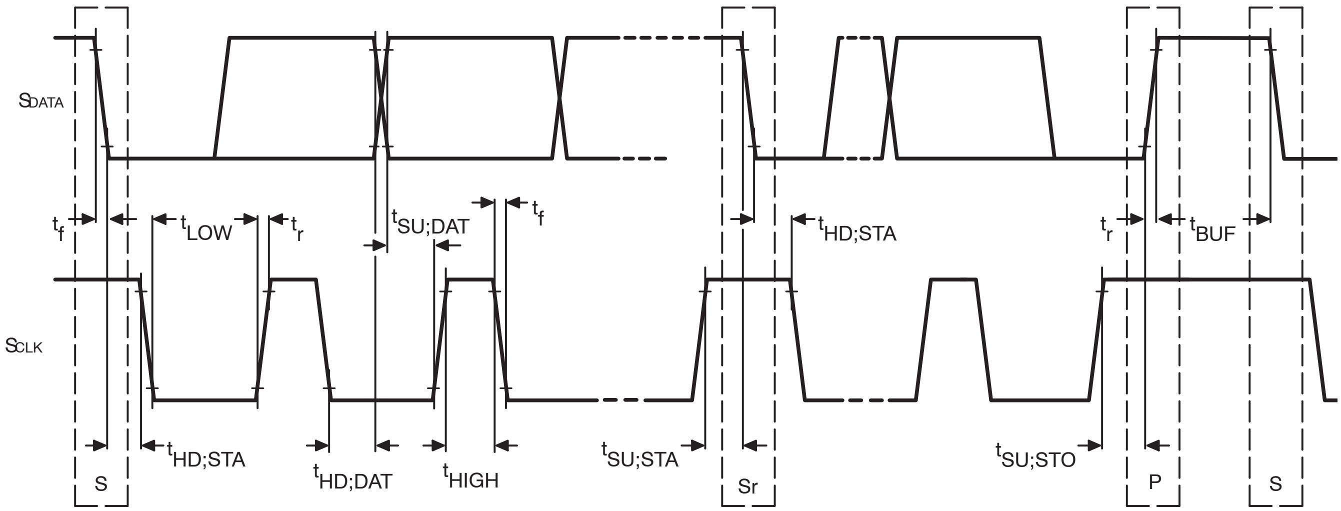


Figure 12. Sequential WRITE, Start at Random Location

ELECTRICAL SPECIFICATIONS

Two−Wire Serial Register Interface

The electrical characteristics of the two−wire serial register interface (SCLK, SDATA) are shown in Figure 13 and Table 4.



Note: Read sequence: For an 8−bit READ, read waveforms start after WRITE command and register address are issued.

Figure 13. Two−Wire Serial Bus Timing Parameters

Table 4. TWO−WIRE SERIAL BUS CHARACTERISTICS
(f_{EXTCLK} = 27 MHz; V_{DD} = 1.0 V; V_{DD}_IO = V_{AA}_1V8 = 1.8 V; V_{AA}_2V8 = V_{AA}_PIX = 2.8 V; T_A = 25°C)

Parameter	Symbol	Standard Mode		Fast Mode		Fast Mode Plus		Unit
		Min	Max	Min	Max	Min	Max	
M_S_{CLK} Clock Frequency	f_{SCL}	0	100	0	400	0	1000	kHz
S_{CLK} High		8*EXTCLK + S_{CLK} rise time		8*EXTCLK + EXTCLK rise time				μs
S_{CLK} Low		6*EXTCLK + S_{CLK} rise time		6*EXTCLK + S_{CLK} rise time				μs
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4	–	0.6	–	0.26	–	μs
LOW period of the M_S_{CLK} clock	t_{LOW}	4.7	–	1.2	–	0.5	–	μs
HIGH period of the M_S_{CLK} clock	t_{HIGH}	4	–	0.6	–	0.26	–	μs
Set−up time for a repeated START condition	$t_{SU;STA}$	4.7	–	0.6	–	0.26	–	μs
Data hold time	$t_{HD;DAT}$	0	3.453	0	0.93	0	–	μs
Data set−up time	$t_{SU;DAT}$	250	–	100	–	50	–	ns
Rise time of both M_S_{DATA} and M_S_{CLK} time (10−90%)	t_r	–	1000	20 + 0.1 Cb (Note 4)	300	20 + 0.1 Cb (Note 4)	120	ns
Fall time of both M_S_{DATA} and M_S_{CLK} time (10−90%)	t_f	–	300	20 + 0.1 Cb (Note 4)	300	20 + 0.1 Cb (Note 4)	120	ns
Set−up time for STOP condition	$t_{SU;STO}$	4	–	0.6	–	0.26	–	μs

Table 4. TWO−WIRE SERIAL BUS CHARACTERISTICS

(f_{EXTCLK} = 27 MHz; V_{DD} = 1.0 V; V_{DD}_IO = V_{AA}_1V8 = 1.8 V; V_{AA}_2V8 = V_{AA}_PIX = 2.8 V; T_A = 25°C)

Parameter	Symbol	Standard Mode		Fast Mode		Fast Mode Plus		Unit
		Min	Max	Min	Max	Min	Max	
Bus free time between a STOP and START condition	t_{BUF}	4.7	–	1.3	–	0.5	–	μs
Capacitive load for each bus line	Cb	–	400	–	400	–	500	pF
Serial interface input pin capacitance	C_{IN_SI}	–	3.3	–	3.3	–	3.3	pF
M_S_{DATA} max load capacitance	C_{LOAD_SD}	–	30	–	30	–	30	pF
M_S_{DATA} pull−up resistor	R_{SD}	1.5	4.7	1.5	4.7	1.5	4.7	kΩ

3. This table is based on I²C standard (v2.1 January 2000). Philips Semiconductor.
4. Two−wire control is I²C compatible.
5. All values referred to V_{IHmin} = 0.7 V_{DD_IO} and V_{ILmax} = 0.3 V_{DD_IO} levels. Sensor EXCLK = 27 MHz.
6. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of S_{CLK}. The two−wire standard specifies a minimum rise and fall time for Fast−Mode and Fast−Mode Plus modes of operation. This specification is not a timing requirement that is enforced on **onsemi** sensor's as a receiver, because our receivers are designed to work in mixed systems with std−mode where no such minimum rise and fall times are required/specified. However, it's the host's responsibility when using fast edge rates, especially when two−wire slew−rate driver control isn't available, to manage the generated EMI, and the potential voltage undershoot on the sensor receiver circuitry, to avoid activating sensor ESD diodes and current−clamping circuits. This is typically not an issue in most applications, but should be checked if below minimum fall times and rise times are required.
7. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the S_{CLK} signal.
8. A Fast−mode I²C−bus device can be used in a Standard−mode I²C−bus system, but the requirement $t_{SU;DAT}$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the S_{CLK} signal. If such a device does stretch the LOW period of the S_{CLK} signal, it must output the next data bit to the S_{DATA} line t_r max + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard−mode I²C−bus specification) before the S_{CLK} line is released.
9. Cb = total capacitance of one bus line in pF.

Table 5. TWO−WIRE SERIAL REGISTER INTERFACE ELECTRICAL CHARACTERISTICS

(f_{EXTCLK} = 27 MHz; V_{DD} = 1.0 V; V_{DD}_IO = V_{AA}_1V8 = 1.8 V; V_{AA}_2V8 = V_{AA}_PIX = 2.8 V; T_A = 25°C)

Parameter	Symbol	Condition	Standard Mode		Fast Mode		Fast Mode Plus		Unit
			Min	Max	Min	Max	Min	Max	
Input HIGH Voltage	V_{IH}		0.7 * V_{DDIO}	–	0.7 * V_{DDIO}	–	0.7 * V_{DDIO}	–	V
Input LOW Voltage	V_{IL}		–	0.3 * V_{DDIO}	–	0.3 * V_{DDIO}	–	0.3 * V_{DDIO}	V
Output LOW Voltage	V_{OL}	V_{DDIO} = (1.7 V − 1.9 V) I_{OL} = 3 mA	–	0.4	–	0.4	–	0.4	V

Table 6. I/O TIMING CHARACTERISTICS

Symbol	Definition	Condition	Min	Typ	Max	Unit
f_{EXTCLK}	Input Clock Frequency	PLL Enabled	10	–	50	MHz
f_{EXTCLK}	Input Clock Period	PLL Enabled	20	–	100	ns
t_R	Input Clock Rise Time		–	3	–	ns
t_F	Input Clock Fall Time		–	3	–	ns
t_{JITTER}	Input Clock Jitter		–	–	100	ps

NOTE: Under the following operating conditions:
For Min, Typ and Max voltages, refer to Table 7
Min T_J = −40°C Typ T_J = 60°C and Max T_J = 125°C
All values are taken at the 50% transition point. The loading used is 20 pF.

Table 7. DC ELECTRICAL CHARACTERISTICS

Symbol	Definition	Condition	Min	Typ	Max	Unit
V_{DD}	Core digital voltage		0.95	1.0	1.05	V
V_{DD}_IO	I/O digital voltage		1.7	1.8	1.9	V
V_{AA_2V8}	2.8 V Analog voltage		2.66	2.8	2.94	V
V_{AA_1V8}	1.8 V Analog voltage		1.7	1.8	1.9	V
V_{AA}_PIX	Pixel supply voltage		2.66	2.8	2.94	V
V_{DD}_PLL	PLL digital voltage		1.7	1.8	1.9	V
V_{IH}	Input HIGH voltage		V_{DD}_IO * 0.7	–	–	V
V_{IL}	Input LOW voltage		–	–	V_{DD}_IO * 0.3	V
I_{IN}	Input leakage current	No pull−up resistor; V_{IN} = V_{DD}_IO or D_{GND}	–	–	40	μA
V_{OH}	Output HIGH voltage		V_{DD}_IO − 0.4	–	–	V
V_{OL}	Output LOW voltage		–	–	0.4	V
I_{OH}	Output HIGH current	At specified V_{OH}	17.5	–	–	mA
I_{OL}	Output LOW current	At specified V_{OL}	–	–	17.5	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 8. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
$V_{SUPPLY\_2V8\_VAA}$	Power supply voltage 2V8	$V_{SUPPLY\_2V8\_VAAPIX}$	3.5	V
$V_{SUPPLY\_2V8\_VAA\_PIX}$	Power supply voltage 2V8	−0.3	$V_{SUPPLY\_2V8\_VAA}$	V
$V_{SUPPLY\_1V8\_VDDIO}$	Digital Power supply voltage 1V8	−0.3	2.1	V
$V_{SUPPLY\_1V8\_VAA}$	Analog Power supply voltage 1V8	−0.3	2.1	V
V_{SUPPLY_1V0}	Power supply voltage 1V0	−0.3	1.5	V
I_{SUPPLY_2V8}	Power supply current 2V8	–	560	mA
I_{SUPPLY_1V8}	Digital Power supply current 1V8	–	42	mA
$I_{SUPPLY\_1V8\_VAA}$	Analog Power supply current 1V8	–	560	mA
I_{SUPPLY_1V0}	Power supply current 1V0	–	1100	mA
I_{GND}	Total ground current	–	2000	mA
V_{IN}	DC input voltage	−0.3	V_{DD}_IO + 0.3	V
V_{OUT}	DC output voltage	−0.3	V_{DD}_IO + 0.3	V
T_{STG} (Note 10)	Storage temperature	−40	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

10. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
11. To keep dark current and shot noise artifacts from impacting image quality, keep operating temperature at a minimum.
12. Absolute maximum currents are preliminary, and will be updated for ES samples.

Table 9. REV 1.1 OPERATING CURRENTS IN 4 LANE 765 Mbps MIPI OUTPUT IN SE T1+T2 12bit 60 fps MODE

Current Definition	Symbol	Min	Typ	Max	Unit
Digital Operating Current	IDD	–	237	416	mA
I/O Digital Operating Current	IDD_IO	–	9	12	mA
Analog Operating Current	IAA	–	36	42	mA
Pixel Supply Current	IAA_PIX	–	14	18	mA
PLL Supply Current	IDD_PLL	–	1.2	1.7	mA
Analog Operating Current 1.8 V	IAA_1V8	–	26	32	mA

Table 10. REV 1.1 OPERATING CURRENTS IN 4 LANE 437 Mbps MIPI OUTPUT IN SE T1+T2 12bit 30 fps MODE

Current Definition	Symbol	Min	Typ	Max	Unit
Digital Operating Current	IDD	–	158	344	mA
I/O Digital Operating Current	IDD_IO	–	5.4	8	mA
Analog Operating Current	IAA	–	25	30	mA
Pixel Supply Current	IAA_PIX	–	6.8	9	mA
PLL Supply Current	IDD_PLL	–	1.2	1.7	mA
Analog Operating Current 1.8 V	IAA_1V8	–	15	19	mA

NOTE: Under the following operating conditions:
For Typ and Max voltage, refer to Table 7
Typ T_J = 60°C and Max 125°C
PLL Enabled and PIXCLK = 191.25 MHz

Table 11. REV 1.1 STANDBY CURRENTS

Current Definition	Symbol	Hard Standby (Clock On)		Hard Standby (Clock Off)		Soft Standby (Clock On)		Soft Standby (Clock Off)		Unit
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Digital Operating Current	IDD	29.00	183	13.00	183	28.00	205	14.00	186	mA
I/O Digital Operating Current	IDD_IO	0.60	30.00	0.30	1.30	0.50	1.30	0.45	1.30	mA
Analog Operating Current	IAA	1.10	1.60	1.30	1.60	9.50	14.00	1.10	1.60	mA
Pixel Supply Current	IAA_PIX	0.02	0.50	0.03	0.50	0.02	0.50	0.03	0.50	mA
PLL Supply Current	IDD_PLL	0.01	0.50	0.03	0.50	0.01	0.50	0.01	0.50	mA
Analog Operating Current 1.8 V	IAA_1V8	0.08	2.70	0.09	2.70	4.00	7.00	0.08	1.00	mA

NOTE: Under the following operating conditions:
For Typ and Max voltage, refer to Table 7
Typ T_J = 60°C and Max 125°C

MIPI Electrical Specifications

The **onsemi** AR0341AT sensor supports four lanes of MIPI data.

Compliant to MIPI standards:

- MIPI Alliance Standard for CSI−2 version 3.0
- MIPI Alliance Standard for D−PHY version 2.5

MIPI AC AND DC ELECTRICAL CHARACTERISTICS

Table 12. MIPI HIGH−SPEED TRANSMITTER DC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
V_{OD}	HS transmit differential voltage	140	200	270	mV
V_{CMTX}	HS transmit static common mode voltage	150	200	250	mV
ΔV_{OD}	V_{OD} mismatch when output is Differential−1 or Differential−0	–	–	14	mV
$\Delta V_{CMTX}(1,0)$	V_{CMTX} mismatch when output is Differential−1 or Differential−0	–	–	5	mV
V_{OHHS}	HS output HIGH voltage	–	–	360	mV
Z_{OS}	Single−ended output impedance	40	50	62.5	Ω
ΔZ_{OS}	Single−ended output impedance mismatch	–	–	20	%

Table 13. MIPI HIGH−SPEED TRANSMITTER AC CHARACTERISTICS 4 LANE

Symbol	Parameter	Min	Typ	Max	Unit
	Data bit rate (4 lane configuration)	–	–	1600	Mbps/lane
t_{rise}	20–80% rise time	–	–	233	ps
t_{fall}	20–80% fall time	–	–	233	ps

Table 14. MIPI LOWER−POWER TRANSMITTER DC SPECIFICATIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{OH}	Thevenin Output High Level	0.95	–	1.1	V
V_{OL}	Thevenin Output Low Level	–50	–	50	mV
Z_{OLP}	Output Impedance of LP Transmitter	110	–	–	Ω

Table 15. MIPI LOW−POWER TRANSMITTER AC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
t_{rise}	15–85% rise time	–	–	25	ns
t_{fall}	15–85% fall time	–	–	25	ns
Slew	Slew rate (C_{LOAD} 5–20 pF)	–	–	250	mV/ns
Slew	Slew rate (C_{LOAD} 20–70 pF)	–	–	150	mV/ns

Power Up/Down Timing

Power Up

The available power rails (1.0 V, 1.8 V, 2.8 V) may be powered up in any order, including all together. However the recommended power−up sequence is as follows. The init (t4) must be followed along with the RESET_N / XSHUTDOWN.

1. Turn on VDDIO1V8 and VAA1V8 (1.8 V) power supply.
2. After 0 to 100 μs, turn on VAA2V8 and VAA2V8PIX (2.8 V) power supply.
3. After 0 to 100 μs, turn on DVDD1V0 (1.0 V) power supply.
4. As the last power supply stabilizes, enable EXTCLK.
5. Assert RESET_N for at least 1 ms.
6. After de−asserting RESET_N, wait for 100 ms.
7. Configure part as desired and set streaming mode (R0x0100[8] = 1).
8. Wait for 1 ms for PLL lock to complete.

The AR0341AT is now in streaming mode.

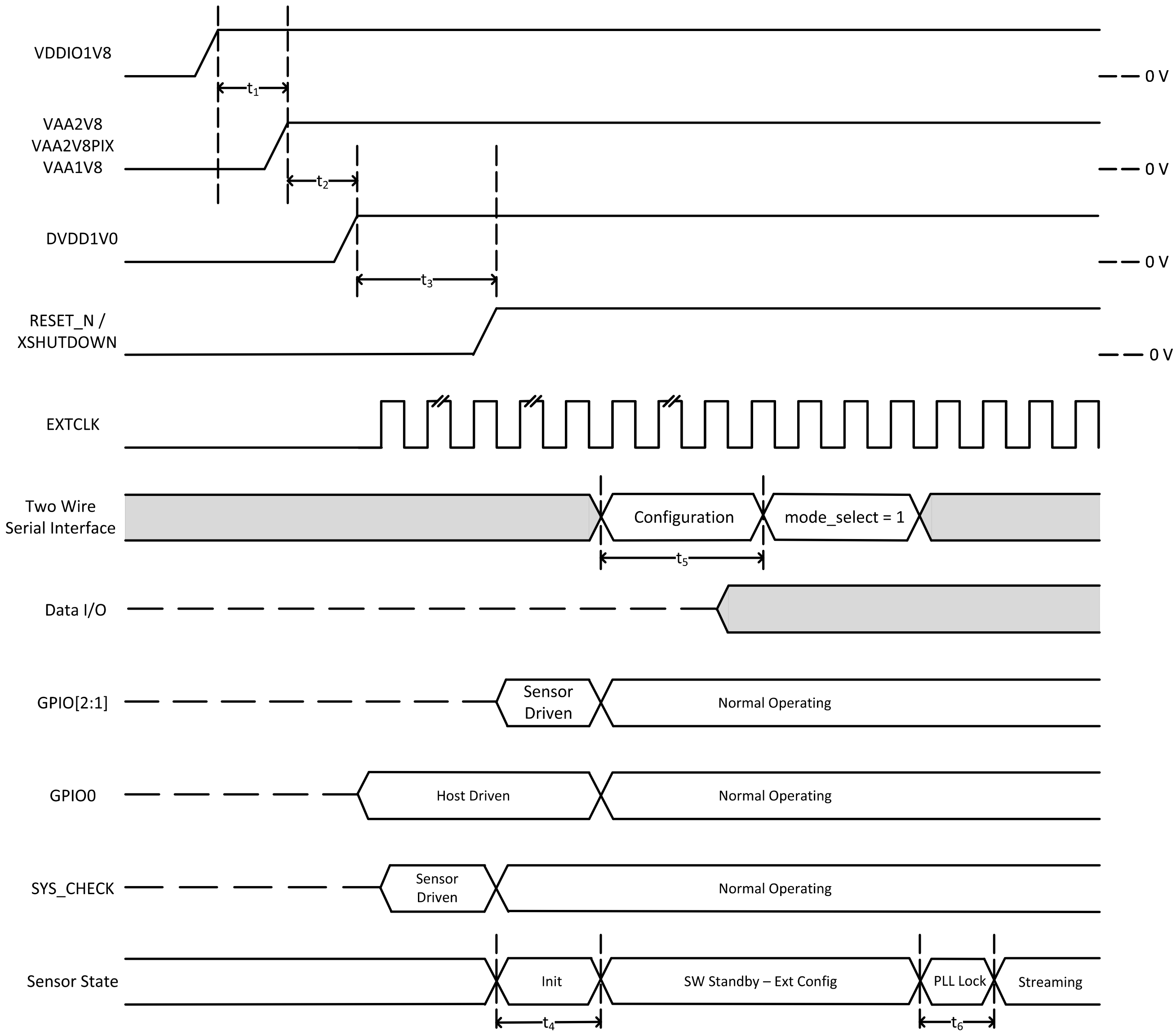


Figure 14. Initial Power Up Sequence

Table 16. POWER UP SEQUENCE

Definition	Symbol	Min	Typ	Max	Unit
VDDIO1V8 applied to VAA2V8 / VAA2V8PIX / VAA1V8 applied	t_1	0	100	–	μs
VAA2V8 / VAA2V8PIX / VAA1V8 applied to DVDD1V0 applied	t_2	0	100	–	μs
Hard Reset	t_3	1.0	–	–	ms
Minimum number of EXTCLK cycles prior to the first Two−wire serial interface transaction (includes, OTPM and ROM loading, MBIST and ASIL startup delay)	t_4	7.5	20.5		ms
Configuration (includes charge pump initialization)	t_5	150	–	–	ms
PLL lock time	t_6	1.0			ms
External power slew rate	slew rate	–	25	50	mV/μs

NOTE: VDDIO1V8 of 1.8 V can be tied together with VAA2V8/VAAPIX2V8 (t1 becomes ‘0’ in this case)
If GPIO0 is pulled up, t_4 could be 5 ms. Otherwise t4 should be 297K Ext clk cycles (11 ms at 27 MHz ext clk) plus 5 ms or longer.
If one of the available power supplies is lost or not within rated limits during power up, down or operation, there is no permanent damage to the image sensor.
t_4 is Minimum wait time before sending an I^2C command.

Power Down

The available power supplies (VAA2V8, VAA2V8PIX, VAA1V8, DVDD1V0, VDDIO1V8) may be powered down in any order. Below is an example recommended power−down sequence.

1. [Optional] Disable streaming if output is active by setting standby (R0x0100[8] = 0).
2. [Optional] Wait for soft standby state to be reached which occurs after the current row or frame, depending on configuration, has ended.
3. [Optional] Assert RESET_N.
4. Turn off DVDD1V0 (1.0 V).
5. Turn off VAA2V8, VAA2V8PIX and VAA1V8 (2.8 V, 1.8 V).
6. Turn off VDDIO1V8 (1.8 V).
7. By following the “OPTIONAL” steps 1 and 2, data output will end on a row or frame boundary.

The AR0341AT requires at least 100 ms before it can be powered on again.

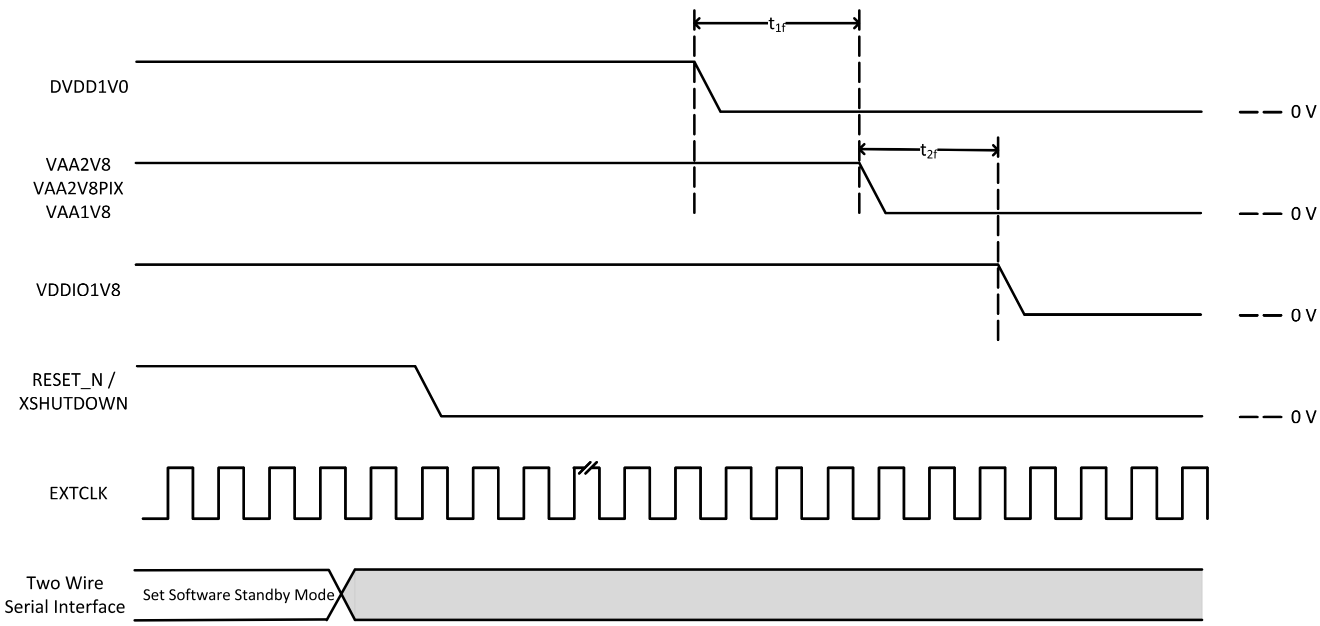


Figure 15. Power Down Sequence

Table 17. POWER DOWN SEQUENCE

Definition	Symbol	Min	Typ	Max	Unit
DVDD1V0 removal to VAA2V8 / VAA2V8PIX / VAA1V8 removal	t_{1f}	0	–	–	ms
VAA2V8 / VAA2V8PIX / VAA1V8 removal to VDDIO1V8 / VDD1V8_PLL removal	t_{2f}	0	–	–	ms

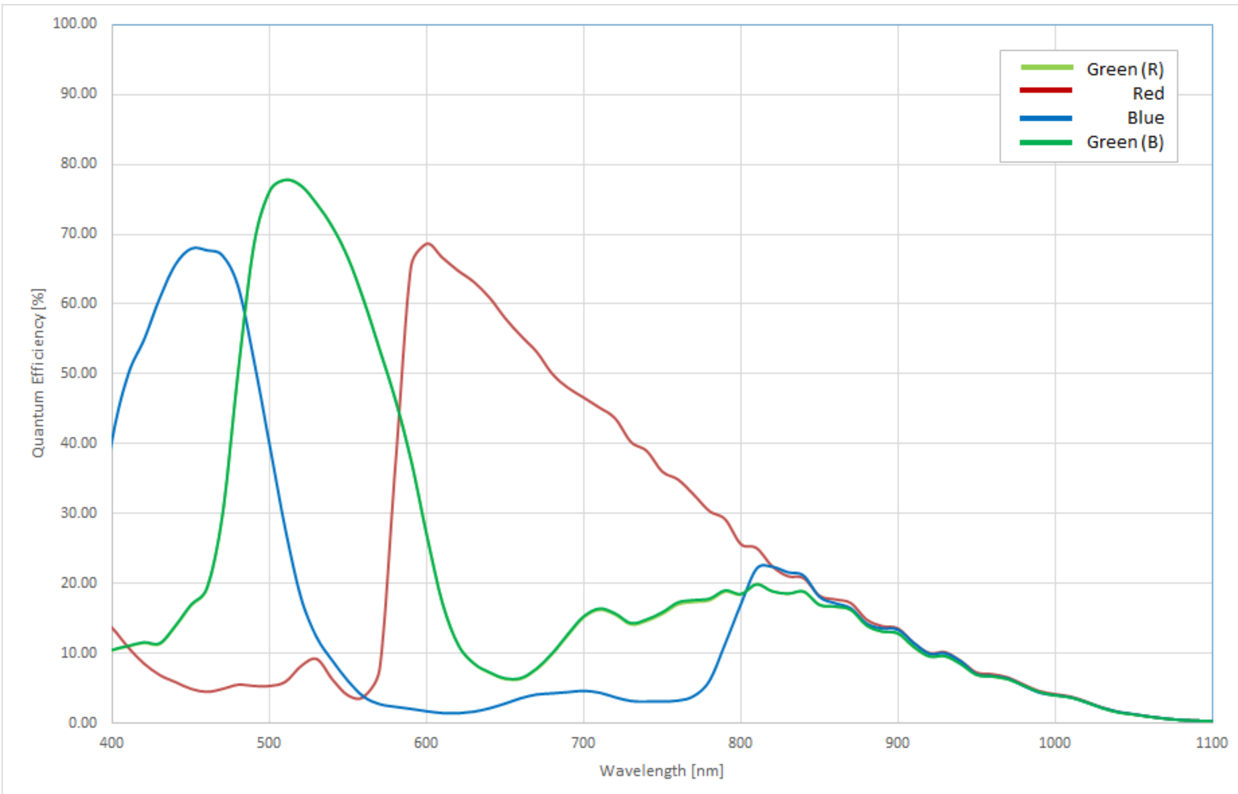


Figure 16. Estimated RGGB Pixel Quantum Efficiencies

CRA vs. Image Height Plot

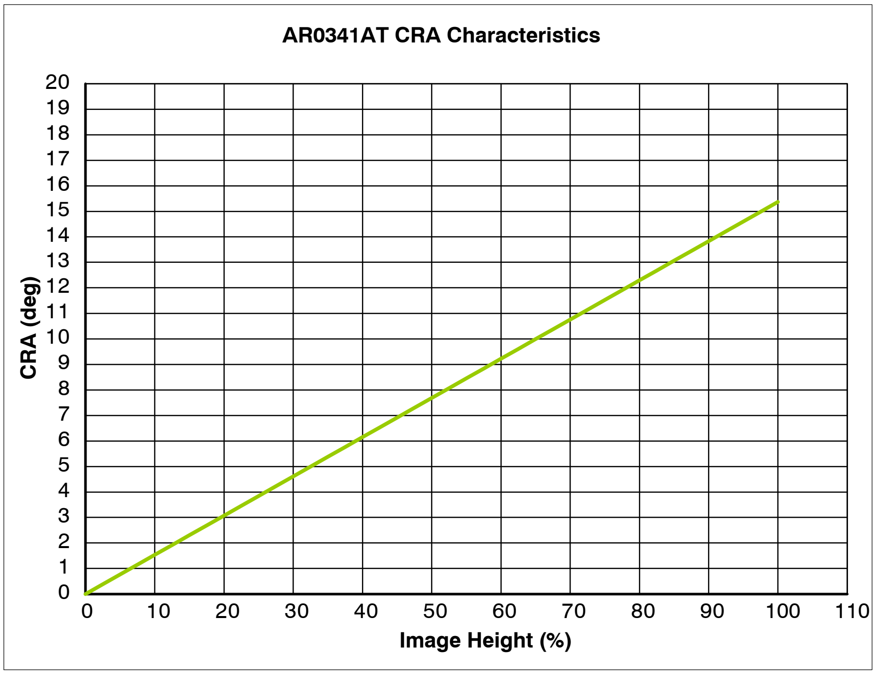
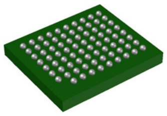


Figure 17. Chief Ray Angle – 15°

Image Height (%)	Image Height (mm)	CRA (deg)
0	0	0
5	0.129	0.77
10	0.258	1.54
15	0.387	2.31
20	0.516	3.07
25	0.645	3.84
30	0.775	4.61
35	0.904	5.38
40	1.033	6.15
45	1.162	6.92
50	1.291	7.68
55	1.420	8.45
60	1.549	9.22
65	1.678	9.99
70	1.807	10.76
75	1.936	11.53
80	2.065	12.29
85	2.194	13.06
90	2.324	13.83
95	2.453	14.60
100	2.582	15.37



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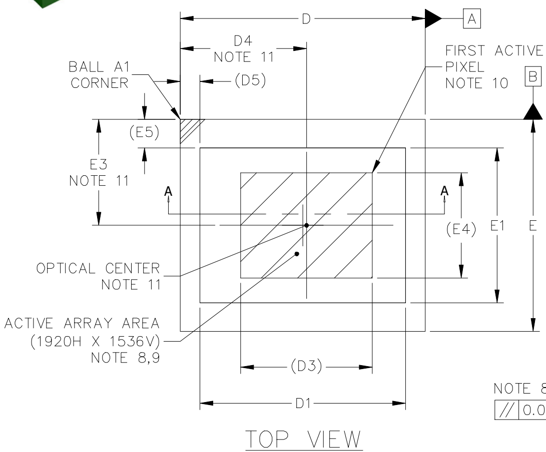
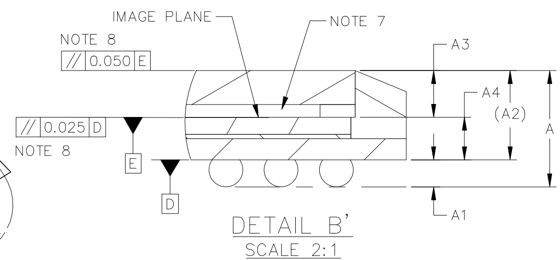
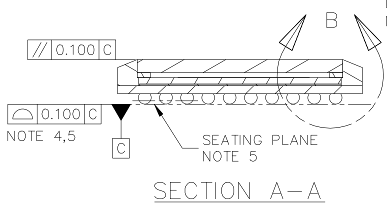


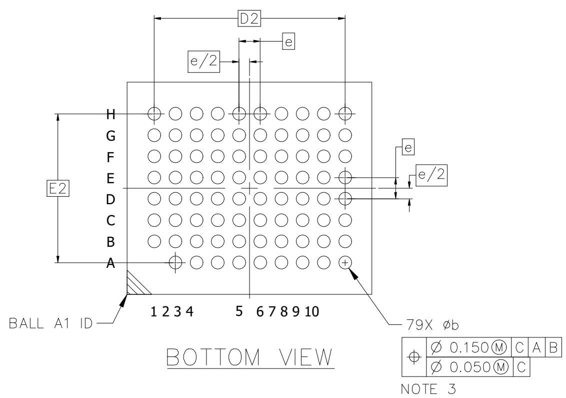
NOTES:

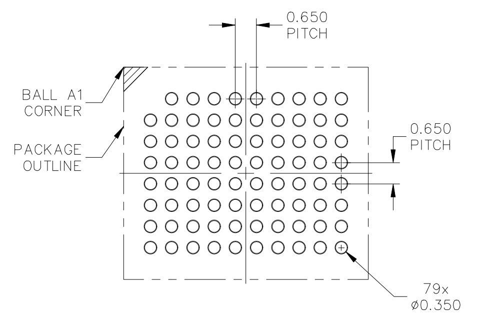
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. SOLDER BALL DIAMETER IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWN OF THE SOLDER BALLS.
5. DATUM C, THE SEATING PLANE IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. GLASS: 0.400 THICKNESS; REFRACTIVE INDEX = 1.52; AR COATING R<1% 420−850nm (EACH SIDE).
7. AIR GAP BETWEEN GLASS AND PIXEL ARRAY: 0.150 THICKNESS.
8. PARALLELISM APPLIES ONLY TO THE ACTIVE ARRAY.
9. MAXIMUM ROTATION OF ACTIVE ARRAY RELATIVE TO DATUMS A AND B IS ± 0.5°.
10. REFER TO THE DEVICE DATA SHEET FOR TOTAL PIXEL ARRAY DEFINITIONS.
11. OPTICAL CENTER RELATIVE TO PACKAGE CENTER (X, Y) = (0.115, 0.000)
12. PACKAGE CENTER (X, Y) = (0.000, 0.000).



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.550
A1	0.270	0.320	0.370
A2	1.050 REF.		
A3	0.500	0.550	0.600
A4	0.450	0.500	0.550
b	0.350	0.400	0.450
D	7.425	7.500	7.575
D1	6.200	6.300	6.400
D2	5.850 BSC		
D3	4.032 REF.		
D4	3.790	3.865	3.940
D5	0.600 REF.		
E	6.425	6.500	6.575
E1	4.660	4.760	4.860
E2	4.550 BSC		
E3	3.175	3.250	3.325
E4	3.226 REF.		
E5	0.870 REF.		
e	0.650 BSC		



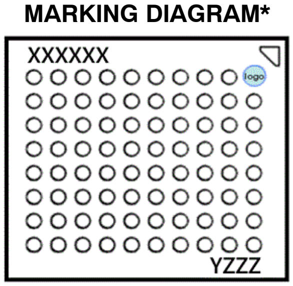




RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
Y = Year
ZZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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